CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX823
Programmable Paging Tone Decoder

D/823/3 November 2003

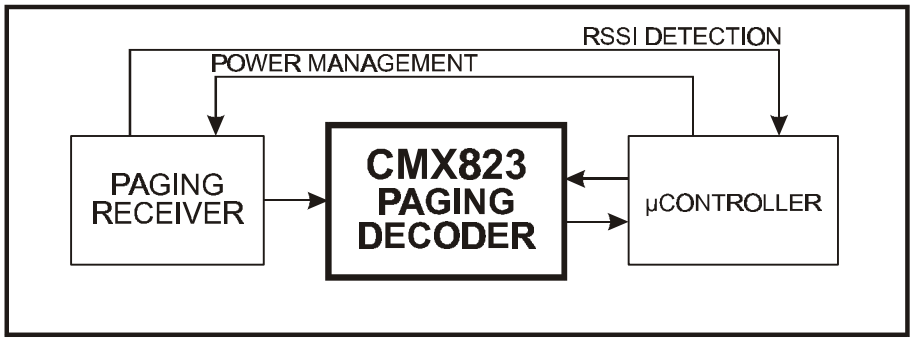
Provisional Issue

Features

- **Decodes 32 User-Programmed Tones**
- **Stores Two Lists of 32 Tones to Fast-Switch Between Tone Sets**
- **Configurable Decode Response Time and Decode Bandwidths**
- **Low Power: 0.75mA at 2.7V (typ.) and 'Zero-Power' Powersave Mode**
- **Superior Signal to Noise Performance**
- **Low Cost 3.58MHz Xtal/Clock**
- **Small 16-pin TSSOP Package**

Applications

- **Two-Tone and 5/6-Tone Pagers**
- **Selective Calling (SELCALL) Systems**
- **Voice Pager Switching and Signalling**
- **Revertive Paging Systems**
- **Wireless Local Loop Signalling**
- **Audio Tone Signalling Applications**



1.1 Brief Description

The CMX823 is a high performance, low power, audio tone decoder that can operate on low S/N signals. Each decoded tone frequency is user-defined to provide the flexibility to operate in a variety of paging, two-way radio and proprietary systems. Example systems and tones include: Motorola Quick Call series; GE groups A, B and Zetron, Reach and Plectron 2-tone radio paging; Motorola 5/6-tone paging; and the EIA, CCIR, ZVEI1 and EEA tonesets used for HSC radio paging and SELCALL. Up to 32 user-defined decode tone frequencies from 280Hz to 3500Hz are written to an internal RAM-based FIFO. (Two separate 32-tone FIFOs are provided and support fast switching between tone sets.) Each programmed tone (entry in the list) is user-assigned to one of two (or both) tone groups. 2-tone sequence decoding is simplified by dynamically enabling one or the other tone group via a mode selection.

The CMX823 asserts an interrupt on tone decoding state transitions, e.g. notone to decoded tone, decoded tone to notone, etc. STATUS and DECODED TONE PARAMETERS Registers may then be read and indicate the decoder status, the target tone decoded and its tone group. The CMX823 operates over the -40ºC to +85ºC range and is available in 16-pin TSSOP (E4) and DIL (P3) packages.

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1.2 Block Diagram

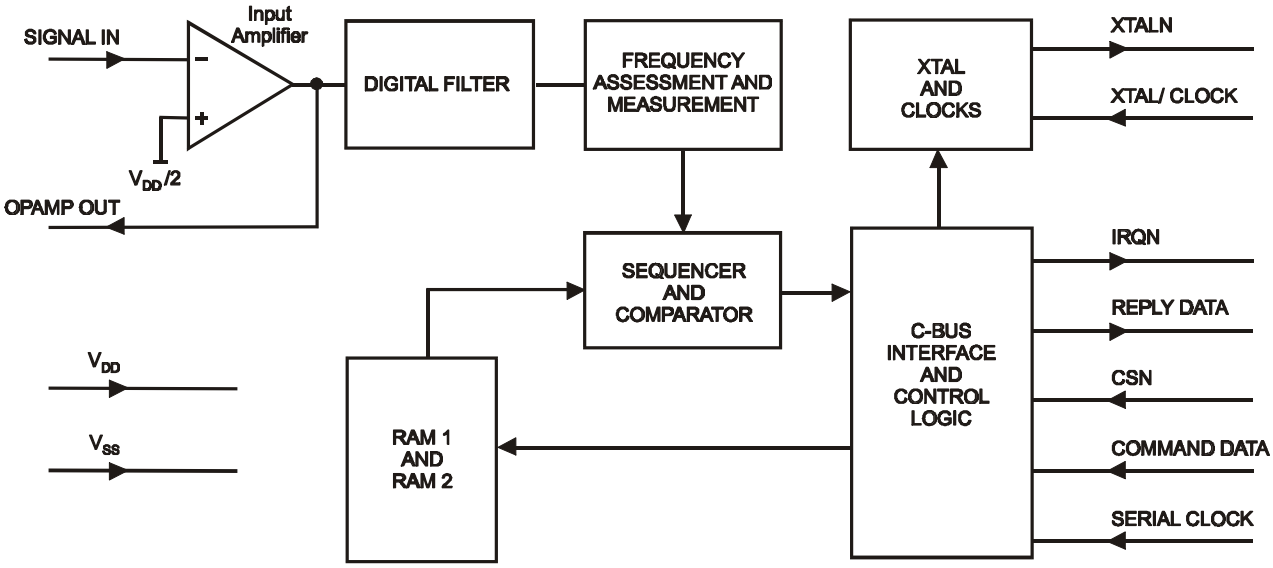


Figure 1 Block Diagram

1.3 Signal List

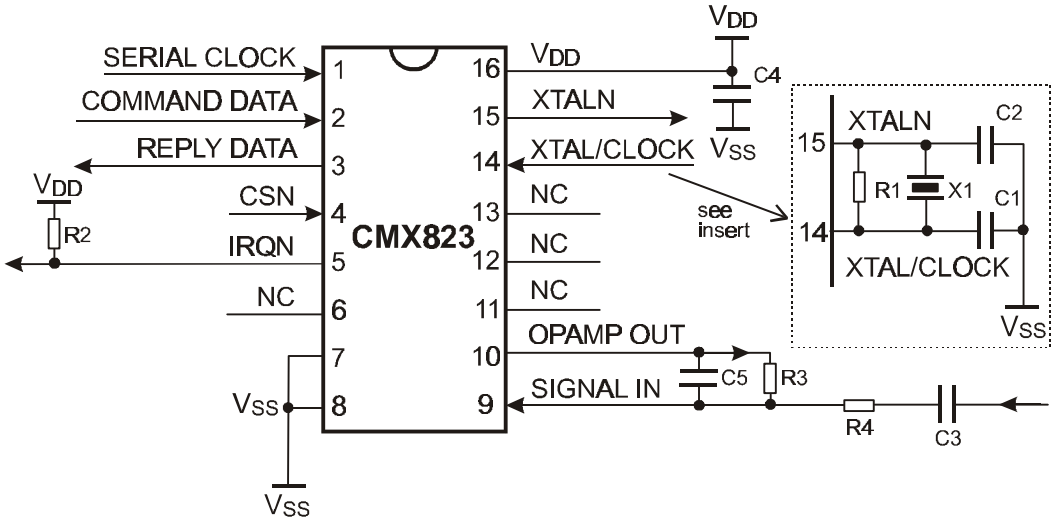
Package E4/P3	Signal		Description
Pin No.	**Name**	**Type**	
1	SERIAL CLOCK	I/P	The C-BUS serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the device. See C-BUS Timing Diagram (Figure 4).
2	COMMAND DATA	I/P	The C-BUS serial data input from the µController. Data is loaded into this device in 8-bit bytes, MSB (b7) first, and LSB (b0) last, synchronised to the SERIAL CLOCK. See C-BUS Timing Diagram (Figure 4).
3	REPLY DATA	TS	The C-BUS serial data output to the µController. The transmission of REPLY DATA bytes is synchronised to the SERIAL CLOCK under the control of the CSN input. This 3-state output is held at high impedance when not sending data to the µController. See C-BUS Timing Diagram (Figure 4).
4	CSN	I/P	The C-BUS data loading control function: this input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the CSN signal. See C-BUS Timing Diagram (Figure 4).
5	IRQN	O/P	This output indicates an interrupt condition to the µController by going to a logic "0". This is a "wire-ORable" output, enabling the connection of several peripherals to 1 interrupt port on the µController. This pin has a low impedance pulldown to logic "0" when active and a high-impedance when inactive. An external pullup resistor is required.

1.3 Signal List (continued)

Package E4/P3	Signal		Description
Pin No.	**Name**	**Type**	
6	NC		Reserved for future use. Do not make any connection to this pin.
7	NC		For manufacturer's use only. Connect to V_{SS}.
8	V_{SS}	Power	The negative supply rail (ground).
9	SIGNAL IN	I/P	The inverting input to the input amplifier.
10	OPAMP OUT	O/P	The output of the input amplifier and the input to the digital filter section.
11	NC		) Reserved for future use. Do not make
12	NC		) any connection to these pins.
13	NC		)
14	XTAL/CLOCK	I/P	The input of the on-chip oscillator.
15	XTALN	O/P	The inverted output of the on-chip oscillator.
16	V_{DD}	Power	The positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor.

Notes: I/P = Input
O/P = Output
TS = 3-state Output
NC = No Connection

1.4 External Components



C1	18pF	±20%	R1	1MΩ	±5%
C2	18pF	±20%	R2	22kΩ	±10%
C3	68nF	±20%	R3	1MΩ	±10%
C4	0.1µF	±20%	R4	51kΩ	±10%
C5	22pF	±20%	X1	3.5795450MHz	±100ppm

Figure 2 Recommended External Components

1.5 General Description

When the CMX823 detects the start of a valid tone it generates an interrupt and reports which tone was detected. At the end of the tone it produces another interrupt and reports NOTONE detected. The host µC should measure and interpret the tone lengths and gap lengths according to calling code requirements. The CMX823 can decode any combination of up to 32 different tones from a list, received in any order. This device is not designed for the decoding of multiple tones that are present simultaneously.

The parameters for decoding each tone in the tone list are stored in a decoding RAM. Two RAMs are available and selectable via CONTROL Register $30. Each RAM is intended for use with a single RF channel and the RAM contents are preserved each time the RF channel is changed or when the device is taken out of Zero-Power mode, so the host µC does not need to reload the tone definitions. Each RAM has the ability to store up to 32 tones. Tone decode parameters can belong to either or both of 2 tone groups, which may be used to represent the first and second tones in a tone sequence. The tone decode parameters for the selected group are sequentially retrieved from RAM and matched with those of the received signal to find a tone decode. If a match is found, the CMX823 generates an interrupt and reports the decoded tone parameters. Further tone definitions in the RAM are not checked as the decoding process is then restarted and a new tone decode match is reported. Tone decode status changes are flagged in the STATUS Register. To ensure data validity, interrupts should be serviced within 4.3ms or 8.6ms, depending on the setting of the FAST/SLOW bit of the CONTROL register.

RAM Location	**RAM FIFO 1**			
	Tone Group		Tone Frequency	
	1	2	N	R
0	1	0	N1	R1
1	1	0	N2	R2
2	1	1	N3	R3
:	:	:	:	:
:	:	:	:	:
:	:	:	:	:
29	1	0	N30	R30
30	0	1	N31	R31
31	1	1	N32	R32

RAM FIFO 2			
Tone Group		Tone Frequency	
1	2	N	R
1	0	N1	R1
1	0	N2	R2
1	1	N3	R3
:	:	:	:
:	:	:	:
:	:	:	:
1	0	N30	R30
0	1	N31	R31
1	1	N32	R32

- Each of the two RAM FIFOs holds an independent list of up to 32 user-defined tones.
- Each defined tone has a user-configured Tone Group assignment.
- One RAM FIFO can be activated at a time. Configuration of CONTROL Register $30 determines which of the RAM FIFOs is currently active.
- Configuration of the TONE DECODE MODE bits (bits 6 and 7) of GENERAL Register $33 determines whether Tone Group 1 or Tone Group 2 assigned tones of the currently active FIFO are decoded.
- RAM location 0 is reserved for programming the 1st tone of a 2-tone or 5/6 tone sequence. It should not be used for programming later tones in the sequence.

Fast and Slow measurement modes are selectable via the CONTROL Register. The Fast mode is intended for 5/6-tone pager tonesets, which require a faster response and the Slow mode is intended for 2-tone pager tonesets, where slower response times are acceptable.

The input amplifier, with suitable external components, is used to adjust the received signal to the correct amplitude for the decoder. All functions are controlled over the C-BUS serial µC interface.

1.5.1 Software Description

Address/Commands
Instructions and data are transferred, via C-BUS, in accordance with the timing information given in Figure 4.

Instruction and data transactions to and from the CMX823 consist of an Address/Command (A/C) byte that may be followed by either:

(i) a further instruction or data bytes or
(ii) a status byte or Rx data reply bytes

8-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	GENERAL RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$30	CONTROL	RAM SELECT	FAST/ SLOW SELECT	DECODER BANDWIDTH				OPERATION MODE	
		BIT 7	BIT 6	MSB BIT 5	BIT 4	BIT 3	LSB BIT 2	MSB BIT 1	LSB BIT 0
$32	AUXILIARY CONTROL		Reserved						I/P SIGNAL FLOW
		BIT 7						BIT 1	BIT 0
$33	GENERAL	1^{ST} TONE DECODE	2^{ND} TONE DECODE	Reserved	Not used				
		BIT 7	BIT6	BIT 5	MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0

Write Only Register Descriptions

GENERAL RESET (Hex address $01)

The reset command has no data attached to it. It resets the device (write) registers to zero (including the OPERATION MODE bits of the CONTROL Register) and therefore enters Zero-Power mode. The RAM FULL bit of the STATUS Register is reset to "0" but the contents of the two RAMs are retained. The OPERATION MODE bits are used to clear the RAMs before writing to them, once the CMX823 has been powered up.

CONTROL Register (Hex address $30)

This register is used to control the functions of the device as described below:

RAM SELECT (Bit 7) This bit selects one of the two RAMs for programming or decoding.

Bit 7	
0	RAM 1 selected
1	RAM 2 selected

In order to change the selected RAM, it is necessary to first disable tone detection, by placing the CMX823 into NoTone state. The suggested procedure is:

i) Enter NoTone state by setting GENERAL Rgister $33 bits 7 and 6 to '0'.
ii) Select the other RAM by setting CONTROL Register $30 bit 7 as required.
iii) Re-enable tone detection by setting GENERAL Register $33 bits 7 and 6 to their previously held values.

FAST/SLOW SELECT (Bit 6) This bit selects the measurement mode used for decoding.

Bit 6	
0	SLOW measurement mode
1	FAST measurement mode

DECODER BANDWIDTH (Bits 5, 4, 3 and 2) These four bits set the nominal bandwidth of the tone decoder according to the table below:

Bit 5	Bit 4	Bit 3	Bit 2	BANDWIDTH Nominal Decode
0	0	0	0	±0.1%
0	0	0	1	±0.3%
0	0	1	0	±0.5%
0	0	1	1	±0.7%
0	1	0	0	±0.9%
0	1	0	1	±1.1%
0	1	1	0	±1.3%
0	1	1	1	±1.5%
1	0	0	0	±1.7%
1	0	0	1	±1.9%
1	0	1	0	±2.1%
1	0	1	1	±2.3%
1	1	0	0	±2.5%
1	1	0	1	±2.7%
1	1	1	0	±2.9%
1	1	1	1	±3.1%

OPERATION MODE (Bits 1 and 0) These two bits select the mode of operation of the device.

Bit 1	Bit 0	OPERATION MODE
0	0	Zero-Power state.
0	1	CLEAR RAM: Clears all of the contents of the selected RAM. The RAM FULL bit of the STATUS Register is reset to 0. Wait 100ns after setting this mode, so that the clear operation can complete.
1	0	Normal operation, tone decoding enabled.
1	1	Reserved for future use.

AUXILIARY CONTROL Register (Hex address $32)

(Bit 7 to Bit 1) Reserved for future use. These bits should be reset to "0".

(Bit 0) This bit controls the input signal flow. In normal use it should be set to “0”, but during the loading of RAM values it should be set to “1”, to prevent a spurious input from disrupting the loading process.

GENERAL Register (Hex address $33)
This register is used to enable either the 1st tone or 2nd tone decode mode and interrupt.

TONE DECODE MODE (Bits 7 and 6) These two bits select the decode mode and interrupt action of the device.

Bit 7	Bit 6	TONE DECODE MODE
0	0	Tone decode interrupt is disabled. Device goes to NOTONE state.
0	1	2nd tone group decode mode: any 2nd tone programmed in the RAM list will be matched with the received signal. Tone decode interrupt is enabled.
1	0	1st tone group decode mode: any 1st tone programmed in the RAM list will be matched with the received signal. Tone decode interrupt is enabled.
1	1	Not allowed. It is not possible to search for 1st and 2nd tone groups at the same time, even though a programmed tone can belong to both groups.

The CMX823 will ignore a similar frequency tone which is in a different tone group. i.e. If the device is in 1st tone group decode mode it will ignore a 2nd tone group signal (not also configured to be in the 1st tone group) which is on the same tone list.

(Bit 5) Reserved for future use. This bit should be reset to "0".

(Bit 4 to Bit 0) Not used. Reserved for future use. These bits should all be reset to "0".

16-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 15 (D15)	BIT 14 (D14)	BIT 13 - BIT 7 (D13 - D7)	BIT 6 - BIT 0 (D6 - D0)
$34	TONE PARAMETERS	1ST TONE GROUP	2ND TONE GROUP	N (binary representation of the decimal number n)	R (the nearest 7-bit binary representation of r)

TONE PARAMETERS Register (Hex address $34)
This register is used to load the list of up to 32 tone centre frequencies (N and R values) and their associated tone groups into the selected RAM. A CLEAR RAM command should precede any new list to be loaded. When cleared, every RAM location will hold N and R values of zero, which indicates an unused memory location. A FIFO system is used for loading each RAM. If more than 32 tones are loaded into a RAM, only the last 32 entries will be stored. All desired tone entries (up to 32) must be loaded into a RAM before enabling it for decoding: incremental changes to a configured list are not allowed. Note that the list is programmed into the selected RAM by repeating the C-BUS routine in Figure 4 up to 32 times:
(take CSN low, load COMMAND byte [$34], wait, load DATA [high] byte, wait, load DATA [low] byte, take CSN high, wait) - This routine is to be repeated for each tone definition that is loaded into the RAM.

TONE GROUP (Bits 15 and 14) These two bits indicate that the tone parameters belong to either a 1st tone or a 2nd tone of a 2-tone scheme, or that they belong to another scheme (e.g. 5/6-tone) where the parameters are matched in both groups.

Bit 15	Bit 14	TONE GROUP
0	0	No decode.
0	1	2nd tone group.
1	0	1st tone group.
1	1	Both tone groups.

Before an interrupt can be issued on the detection of a valid tone match, the 1st tone decode mode or 2nd tone decode mode must have been set (Bit 7 or Bit 6 of the GENERAL Register - $33). This tone decode mode must match the corresponding tone group programmed into Bit 15 or Bit 14 above.

N and R (Bit 13 to Bit 0) Each tone to be decoded is identified by 14 bits of data, representing the tone frequency, according to the formula below:

For SLOW mode:

$$n = INT\ (118920 \times f_{TONE} / f_{XTAL})$$

$$r = ((29730 / f_{XTAL}) - (n / (4 \times f_{TONE}))) \times 119318.1667$$

$$f_{TONE} = n \times f_{XTAL} / (240 \times (495.5 - (r / 2)))$$

Example: To decode 1000Hz when using the recommended 3.579545MHz Xtal.

n = INT (118920 x 1000 / 3.579545 x 10^6)
= INT (33.222) = 33 (truncated)
∴ N = 0100001 (binary)

r = ((29730 / 3.579545 x 10^6) - (33 / (4 x 1000))) x 119318.1667
= 6.625
= 6 (truncated)
∴ R = 0000110 (binary)

For FAST mode:

$$n = INT\ (59460 \times f_{TONE} / f_{XTAL})$$

$$r = ((14865 / f_{XTAL}) - (n / (4 \times f_{TONE}))) \times 119318.1667$$

$$f_{TONE} = n \times f_{XTAL} / (120 \times (495.5 - r))$$

Example: To decode 1000Hz when using the recommended 3.579545MHz Xtal.

n = INT (59460 x 1000 / 3.579545 x 10^6)
= INT (16.611) = 16 (truncated)
∴ N = 0010000 (binary)

r = ((14865 / 3.579545 x 10^6) - (16 / (4 x 1000))) x 119318.1667
= 18.227
= 18 (truncated)
∴ R = 0010010 (binary)

Read Only Register Descriptions

8-bit Read Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$38	DECODED TONE RAM LOCATION	Reserved: set to 0	0	0	DECODED TONE RAM LOCATION MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$3F	STATUS	Reserved: set to 0	0	TONE CHANGE	RAM FULL	DECODE STATUS CHANGE	TONE DECODE	UNLISTED TONE	RAM1 or RAM2

DECODED TONE RAM LOCATION Register (Hex address $38)

This register is used to indicate the location in the selected RAM of the decoded tone, as follows:

(Bits 7, 6 and 5) Reserved for future use. These are set to "000" and should be ignored by the user.

DECODED TONE RAM LOCATION (Bit 4 to Bit 0) After a valid detection, the location in the selected RAM of the decoded tone is presented as a 5-bit number. A value of "00000" represents the location first written to and a value of "11111" represents the last location in RAM, whether written to or not. This register is updated at the same time as the 16-bit DECODED TONE PARAMETERS Register $3C and may be read instead of the latter when the tone decode N and R values are already known by the host µC.

STATUS Register (Hex address $3F)

This register is used to indicate the status of the device, as described below and subsequently in Figure 3:

(Bits 7 and 6) Reserved for future use. These are set to "00" and should be ignored by the user.

TONE CHANGE (Bit 5) After a valid detection, the device is at the listed TONE DECODE state. If the decoder then detects another listed tone, the TONE CHANGE bit is set to "1".

RAM FULL (Bit 4) After 32 tone addresses are loaded to the selected RAM, this bit is set to "1". This RAM FULL bit, together with the contents of both RAMs, is not altered by putting the CMX823 into the Zero Power state, unless this was by means of a GENERAL RESET command.
A CLEAR RAM or GENERAL RESET command will reset the RAM FULL bit to "0", but will leave the RAM contents undisturbed.

DECODE STATUS CHANGE (Bit 3) When in TONE DECODE state and leaving that state or
when the decoded 16-bit data in DECODED TONE PARAMETERS Register $3C changes state and the selected tone decode mode also matches the corresponding tone group programmed, this bit will be set to "1".
A “0” indicates no change in the decode status.

TONE DECODE (Bit 2)

This bit indicates the status of the tone decoder. A "1" indicates a tone has been detected (TONE DECODE) and a "0" indicates the loss of the tone (NOTONE) or the identification of a valid tone which is in the pre-programmed list of the selected RAM but not in the tone group programmed to be detected, when in NOTONE state.

From NOTONE state, TONE DECODE set to "1" means that a tone has been decoded and its characteristics are as defined by the bandwidth (see CONTROL Register $30, Bits 5, 4, 3 and 2), the centre frequency and the tone group (see TONE PARAMETERS Register $34, Bit 15 to Bit 0). An interrupt will be generated.

From NOTONE state, the identification of a valid tone which is not in the pre-programmed list of the selected RAM (up to 32 tones) will cause the decoder to move to the TONE DECODE state with the UNLISTED TONE (Bit 1) set to "1", indicating a valid but unrecognised tone. No interrupt is generated.

From NOTONE state, the identification of a valid tone which is in the pre-programmed list of the selected RAM but not in the tone group programmed to be detected, will not cause the decoder to move to the TONE DECODE state and the UNLISTED TONE (Bit 1) will remain at "0". No interrupt is generated.

From TONE DECODE state, if the decoder detects another tone, either listed or unlisted, either in the same or in a different tone group, the TONE DECODE bit will remain at "1". An interrupt will be generated.

Loss of tone will cause the NOTONE timer to be started. If loss of tone continues for the duration of the time-out period, then the decoder will move to the NOTONE state and the identification of pre-programmed tones will start again. The time-out period is not user adjustable. After the CMX823 has deresponded into the NOTONE state, the internal decoded data history should be cleared by resetting the GENERAL Register $33 bits 6 and 7 to “0” for a short period (> 10µs). These bits should then be returned to their previous values. This will ensure that the decoding of a new tone is not influenced by assessments made on the previous tone. See Figure 3.

UNLISTED TONE (Bit 1)

This bit, if set to "1", indicates that an UNLISTED tone has been decoded. This bit is reset to "0" if a listed tone (of any kind) is decoded.

RAM 1 or RAM 2 (Bit 0)

This bit indicates the RAM that was selected when a match is found for the decoded tone. A "1" indicates RAM 2, a "0" indicates RAM 1. This bit is undefined if there is no decoded tone or if the tone is unlisted. No interrupt is generated.

If the DECODE STATUS CHANGE **(**Bit 3) of the STATUS Register is "1" or the RAM FULL (Bit 4) of the STATUS Register changes from "0" to "1" or the TONE CHANGE **(**Bit 5) of the STATUS Register is "1" then an interrupt will be generated and the IRQN output will be pulled low.

Reading the STATUS Register clears the interrupt (IRQN output goes high) and also clears Bit 3 and Bit 5 of the STATUS Register, if set. A CLEAR RAM command clears Bit 4 of the STATUS Register, if set. Bits 2, 1 and 0 are set and reset by the action of the tone decoder algorithm, shown in Figure 3. These are updated every 4.3ms in FAST mode or every 8.6ms in SLOW mode, depending on the setting of the FAST/SLOW bit of the CONTROL register, after the IRQN pin is pulled low.

In Zero-Power mode, STATUS Register Bits 7 to 0 are preset to “000x0000” respectively.

When Bit 7 and Bit 6 in the GENERAL Register $33 are reset to "0" (disabling the tone decoder), RAM 1 or RAM 2 (Bit 0), UNLISTED TONE (Bit 1), TONE DECODE (Bit 2), DECODE STATUS CHANGE (Bit 3) and TONE CHANGE (Bit 5) will also be reset to "0".

16-bit Read Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 15 (D15)	BIT 14 (D14)	BIT 13 - BIT 7 (D13 - D7)	BIT 6 - BIT 0 (D6 - D0)
$3C	DECODED TONE PARAMETERS	1ST TONE GROUP	2ND TONE GROUP	N (binary representation of the decimal number n)	R (the nearest 7 bit binary representation of r)

DECODED TONE PARAMETERS Register (Hex address $3C)

This register is used to send the decoded tone parameters to the host µC as described below. It is updated every 4.3ms or 8.6ms, depending on the setting of the FAST/SLOW bit of the CONTROL Register $30. The value is valid from the falling edge of IRQN for a period of either 4.3ms or 8.6ms, depending on the setting of the FAST/SLOW bit. Note that the STATUS Register only changes when there is a change of decode status (see Figure 3).

DECODED TONE GROUP (Bits 15 and 14)

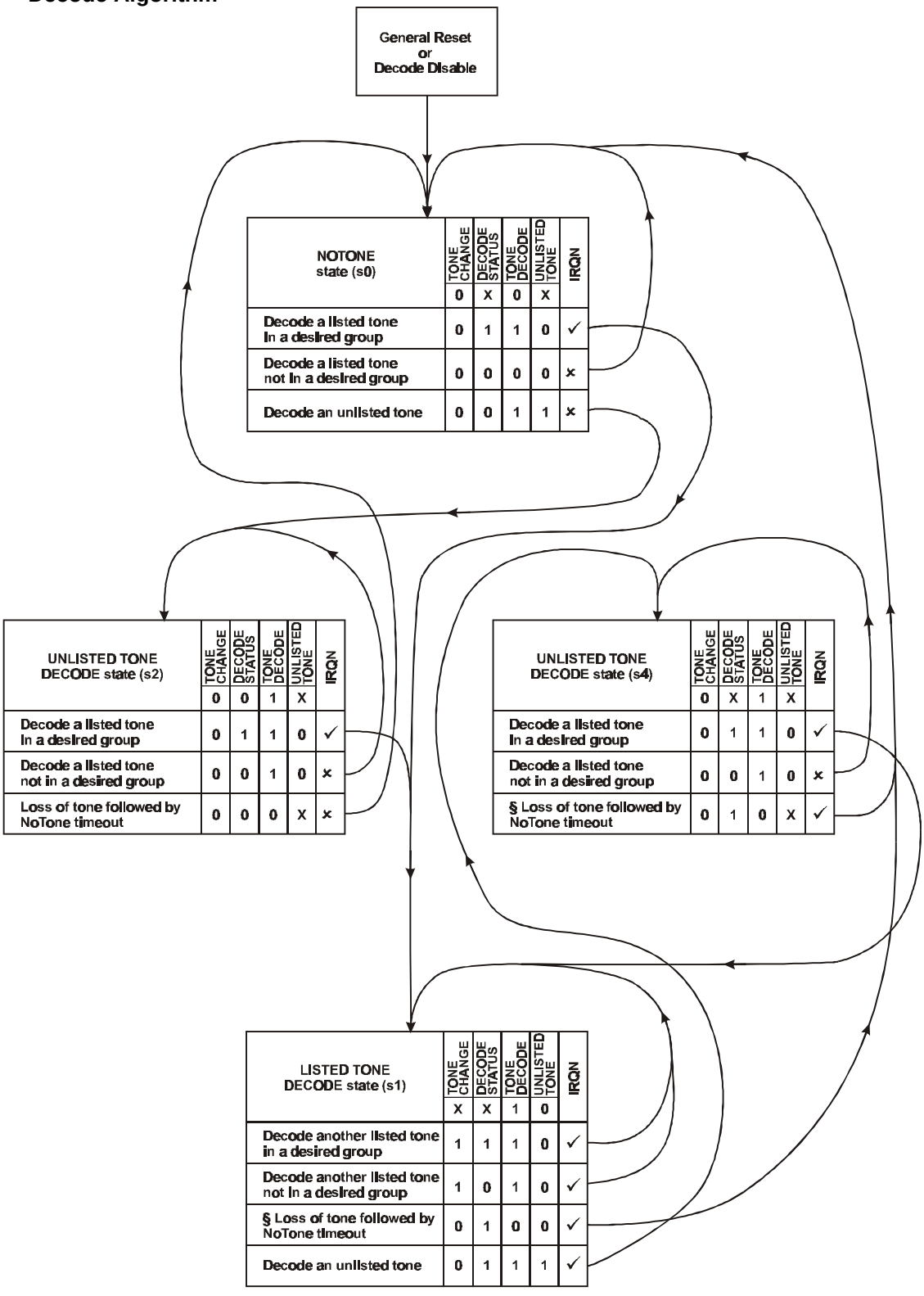
These two bits indicate the tone group set in the decoded tone's parameters: (1st tone or 2nd tone of a 2-tone scheme, or both tones, for a 5/6-tone scheme).

Bit 15	Bit 14	DECODED TONE GROUP
0	0	No decode.
0	1	2nd tone group decoded.
1	0	1st tone group decoded.
1	1	Either tone group decoded.

DECODED TONE PARAMETERS (Bit 13 to Bit 0)

When a tone is decoded and a match found, the CMX823 reports the decoded tone parameters (N and R values) which were originally programmed via the TONE PARAMETERS Register $34. It does not report the actual N and R values of the decoded tone. The contents of each RAM location are compared with the N and R values derived from the incoming signal, after making allowance for the bandwidth programmed into CONTROL Register $30. The first RAM location which produces a valid match with the decoded tone will return its programmed N and R values as the decoded tone parameters in bits 13-0 of the DECODED TONE PARAMETERS Register $3C. The comparison process starts at RAM location 0 and finishes when a tone is matched, or when RAM location 31 is reached. An interrupt may also be generated (see Figure 3).

1.5.2 Decode Algorithm



§ See detailed description of $3F STATUS Register, TONE DECODE (bit 2) for the procedure associated with this transition.

Figure 3 Decode Algorithm State Diagram

1.6 Application Notes

1.6.1 General

The device should be reset first by the command GENERAL RESET $01. This will put the device into Zero-Power mode and will clear all of the registers, but will retain the contents of the two RAMs.

Setting the OPERATION MODE bits of the CONTROL Register $30 will take the CMX823 out of Zero-Power mode. Approximately 30ms should be allowed for the crystal oscillator to start-up and the internal amplifier bias point to stabilize before attempting to use the CMX823.

Clear the contents of both RAMs before programming the tone parameters to be decoded:

Select RAM 1 (Bit 7) and set to CLEAR RAM mode (Bits 1 and 0) in CONTROL Register $30.
Wait 100µs.
Select RAM 2 (Bit 7) and set to CLEAR RAM mode (Bits 1 and 0) in CONTROL Register $30.
Wait 100µs.
Select RAM 1 (Bit 7) and set to normal operation mode (Bits 1 and 0) in CONTROL Register $30.
Program the desired RAM 1 tone parameters (i.e. the tone groups and centre frequencies of the desired tones) into TONE PARAMETERS Register $34. Up to 32 tones can be programmed. RAM 1 location 0 is loaded first, then incrementally loaded up to location 31. Bit 0 of the AUXILIARY CONTROL Register $32 should be set to "1" during this process, then reset to "0" when it is required to decode an input signal. This bit enables the input when it is at "0". Allow at least 1µs between each RAM write.
Select RAM 2 and program tones into the TONE PARAMETERS Register, as required.

The desired decoder characteristics should now be set up. This entails setting the normal operation mode, decoder bandwidth, measurement period and decoding RAM to be used in CONTROL Register $30.

Select 1st tone or 2nd tone decode in TONE DECODE MODE (Bits 7 and 6) of GENERAL Register $33. This enables the decoding process.

During the decoding process the tones are scanned in the sequence of their location: once a tone is detected the remaining tones in the selected RAM list are not checked.

When the decoder detects a change in its present state an interrupt may be generated (see Figure 3). The change of decode status that occurred can be read from Bit 3 of STATUS Register $3F. Bit 2 of the same register indicates TONE DECODE or NOTONE. A detectable, but unlisted, tone is indicated by the setting of Bit 1. The selected RAM which contains a match for the decoded tone can be read from Bit 0. The decoding of another listed tone, following the first detection, is indicated by Bit 5. Reading the STATUS Register clears the interrupt.

The decoded tone parameters can be read from DECODED TONE PARAMETERS Register $3C and the location in the selected RAM at which the tone parameters were programmed can be read from DECODED TONE RAM LOCATION Register $38.

When decoding a 2-tone sequence, the TONE DECODE MODE (Bits 7 and 6) of GENERAL Register $33 should be set to 1st tone decode initially. When a tone interrupt occurs, these bits should then be set to 2nd tone decode, in order to reject any continuation of the 1st tone. The next interrupt will indicate the presence (or otherwise) of the 2nd tone.

For a 5/6-tone sequence, the TONE DECODE MODE (Bits 7 and 6) of GENERAL Register $33 should be set to either 1st tone or 2nd tone decode and both tone groups set in the TONE PARAMETERS Register $34. A TONE DECODE interrupt will occur on detection of the start of the sequence and a NOTONE interrupt will occur when the timeout period expires, at the end of the 5/6-tone sequence.

1.7 Performance Specification

1.7.1 Electrical Performance

1.7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA

E4 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		300	mW
... Derating		5	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

P3 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

1.7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Operating Temperature		-40	+85	°C
Xtal Frequency		3.579187	3.579903	MHz

1.7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 3.579545MHz. V_{DD} = 2.7V to 5.5V, Tamb = -40°C to +85°C.
Noise Bandwidth = 5kHz Band Limited Gaussian, 0dB reference = 775mVrms

		Notes	Min.	Typ.	Max.	Units
DC Parameters						
At V_{DD} = 2.7V						
I_{DD} (Zero Power)		1	–	1.0	2.0	µA
I_{DD} (Operating)		1	–	0.75	1.5	mA
At V_{DD} = 5.0V						
I_{DD} (Zero Power)		1	–	1.0	2.0	µA
I_{DD} (Operating)		1	–	1.5	3.0	mA
C-BUS Interface						
Input Logic "1"			70%	–	–	V_{DD}
Input Logic "0"			–	–	30%	V_{DD}
Input Leakage Current (Logic "1" or "0")			-1.0	–	1.0	µA
Input Capacitance			–	–	7.5	pF
Output Logic "1" (I_{OH} = 360µA)			90%	–	–	V_{DD}
Output Logic "0" (I_{OL} = 360µA)			–	–	10%	V_{DD}
IRQN O/P "Off" State Leakage Current (Vout = V_{DD})			–	–	1.0	µA
AC Parameters						
Decoder						
Sensitivity		2	–	-65.0	–	dB
Tone Measurement Resolution						
	Slow measurement Mode		-	±0.1	-	%
	Fast measurement Mode			±0.2		%
Tone Measurement Accuracy			–	±0.5	–	%
Response Time	Slow measurement Mode		–	33.0	49.0	ms
De-Response Time	Slow measurement Mode	3	–	79.0	85.0	ms
Response Time	Fast measurement Mode		–	28.0	37.0	ms
De-Response Time	Fast measurement Mode	3	–	46.0	65.0	ms
Frequency Range			280	–	3500	Hz
Signal/Noise			–	-4	–	dB
Input Amplifier						
Open Loop Gain	(I/P = 1mV at 100Hz)		–	70.0	–	dB
Unity Gain Bandwidth			–	5.0	–	MHz
Input Impedance	(at 100Hz)		10.0	–	–	MΩ
Output Impedance	(Open Loop)		–	6.0	–	kΩ
Xtal/Clock Input						
Pulse Width ('High' or 'Low')		4	40.0	–	–	ns
Input Impedance (at 100Hz)			10.0	–	–	MΩ
Gain (I/P = 1mVrms at 100Hz)			20.0	–	–	dB

Notes:
1. Not including any current drawn from the device pins by external circuitry.
2. Sensitivity is independent of V_{DD}.
3. De-response times are for 95% probability.
4. Timing for an external input to the XTAL/CLOCK pin.

1.7.1 Electrical Performance (continued)

C-BUS Timings (See Figure 4 and Note 9)		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN-Enable to Clock-High time		100	–	–	ns
t_{CSH}	Last Clock-High to CSN-High time		100	–	–	ns
t_{LOZ}	Clock-Low to Reply Output enable time		0.0	–	–	ns
t_{HIZ}	CSN-High to Reply Output 3-state time		–	–	1.0	µs
t_{CSOFF}	CSN-High Time between transactions		1.0	–	–	µs
t_{NXT}	Inter-Byte Time		500	–	–	ns
t_{CK}	Clock-Cycle time		500	–	–	ns
t_{CH}	Serial Clock-High time		200	–	–	ns
t_{CL}	Serial Clock-Low time		200	–	–	ns
t_{CDS}	Command Data Set-Up time		75	–	–	ns
t_{CDH}	Command Data Hold time		25	–	–	ns
t_{RDS}	Reply Data Set-Up time		75	–	–	ns
t_{RDH}	Reply Data Hold time		0	–	–	ns

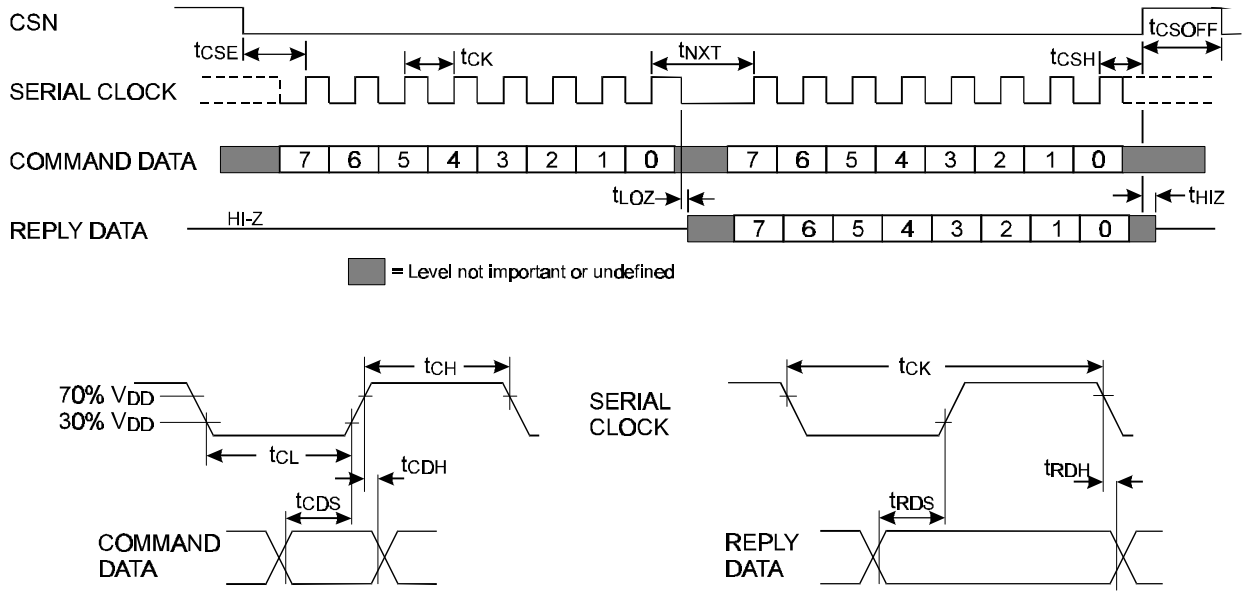
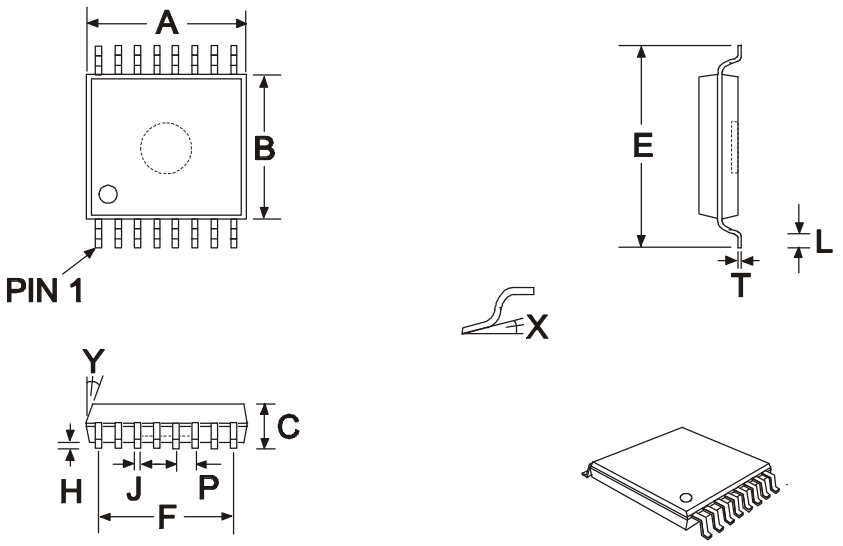


Figure 4 C-BUS Timing

Notes:
5. Depending on the command, 1, 2 or 3 bytes of COMMAND DATA are transmitted to the CMX823 MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA (1 or 2 bytes) is read from the CMX823 MSB (Bit 7) first, LSB (Bit 0) last.
6. Data is clocked into and out of the peripheral on the rising edge of the SERIAL CLOCK.
7. Loaded commands are acted upon at the end of each command (i.e. when CSN goes high).
8. To allow for differing µController serial interface formats, C-BUS compatible ICs are able to work with either polarity SERIAL CLOCK pulses.
9. These timings are for the latest version of the C-BUS, as embodied in the CMX823, and allow faster transfers than the original C-BUS specification.

1.7.2 Packaging



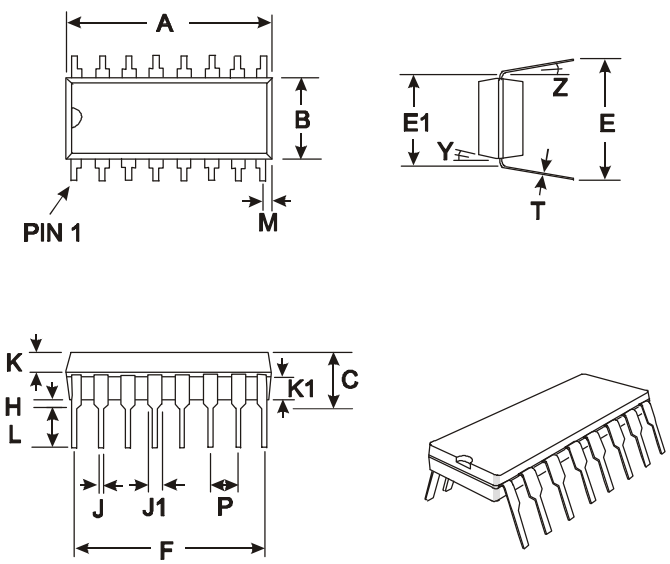
DIM.	MIN.	TYP.	MAX.
* A	4.90		5.10
* B	4.30		4.50
C	--------		1.20
E	6.30		6.50
F		4.55	
H	0.05		0.15
J	0.17		0.30
L	0.45		0.75
P		0.65	
T	0.08		0.20
X	0°		8°
Y		12°	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Figure 5 Mechanical Outline: ***Order as part no. CMX823E4***



DIM.	MIN.	TYP.	MAX.
* A	0.740 (18.80)		0.810 (20.57)
* B	0.240 (6.10)		0.262 (6.65)
C	0.127 (3.23)		0.200 (5.08)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
F		0.70 (17.78)	
H	0.015 (0.38)		0.040 (1.02)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
K1	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
M		0.028 (0.71)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		5°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 6 Mechanical Outline: ***Order as part no CMX823P3***

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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For detailed application notes: www.cmlmicro.com/products/applications/

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