11C83

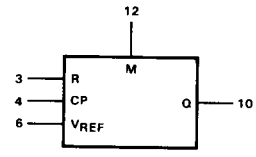
1 GHz DIVIDE-BY-248/256 PRESCALER

11C00 SERIES

GENERAL DESCRIPTION – The 11C83 Prescaler is guaranteed to operate above 950 MHz over the 0°C to +75°C temperature range and with a V_{CC} variation from +4.75 to +5.5 V. The circuit requires only one supply voltage and the clock input signal can be either dc or ac coupled. The prescaler divides by either 248 or 256, as determined by the signal applied to the Mode Control (M) input. This feature makes it possible to use the 11C83 in conjunction with other logic to achieve a broad range of overall divide ratios, either fixed or programmable. For example, a divide ratio of 1000 can be achieved by one 11C83 and one 9LS161 modulo-16 counter.

- **DC TO 950 MHz OPERATION – GUARANTEED OVER 0°C TO +75°C**
- **DC OR AC COUPLED INPUT**
- **USES STANDARD TTL OR CMOS POWER SUPPLY**
- **OUTPUT DRIVES TTL OR CMOS**
- **DIVIDE BY 248/256 MODE CONTROL**

LOGIC SYMBOL



V_{CC} = Pin 1
V_{CCA} = Pin 14
GND = Pin 7

FUNCTIONS

CP = Clock pulse input

M = Mode Control input
LOW = ÷ 248
HIGH = ÷ 256

Q = Output w/2K pull-up

R = 10 kΩ to GND, for optional CP offset

V_{REF} = Internal reference voltage, for ac coupled clocking

FUNCTIONAL BLOCK DIAGRAM

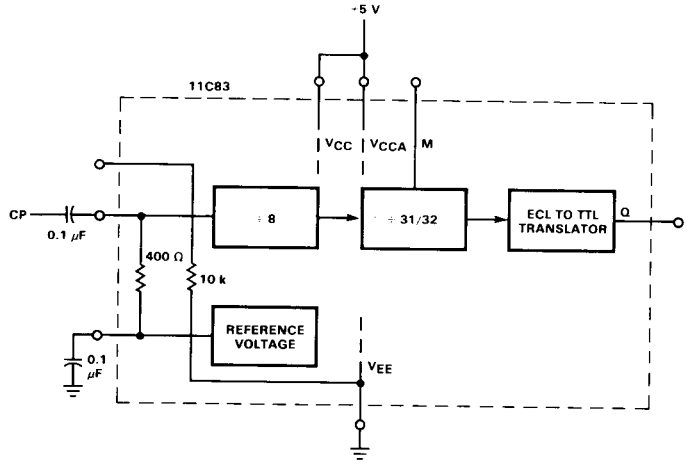
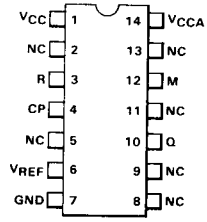


Fig. 1.

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)



FUNCTIONAL DESCRIPTION — The 11C83 contains a 3-stage modulo-8 divider whose output drives a 5-stage modulo-31/32 divider. The 5-stage circuit has a natural divide ratio of 32, but a LOW signal on the Mode Control input causes it to skip one state and thus divide by 31. Referred to the CP input, this changes the overall divide ratio from 256 to 248. Both dividers are designed with ECL circuitry and the divide-by-31/32 drives an ECL-to-TTL translator. The translator has a 2 kΩ pull-up resistor returned to V_{CC} through a diode and thus will pull up high enough to drive CMOS as well as TTL inputs. In the LOW state, the output can sink 10 mA at a V_{OL} level of 0.5 V or less.

The relationship between the output waveform, the divide ratio and the Mode Control input signal are outlined in *Figure 2*. The trigger pulses shown are those which operate the divide-by-31/32 circuit. Although these pulses cannot be monitored, they are convenient to use as timing references in discussing delay time, setup time and, by extension, timing constraints on any external logic used to generate Mode Control signals. As shown, the output is LOW for 16 pulse periods regardless of the state of M. The duration of the output HIGH state, however, can be either 15 or 16 pulse periods. The pulse edge that makes Q go HIGH is identified as t_0. The 15th following pulse edge causes Q to go LOW if M is LOW at least 3 ns before t_{15}. If M is HIGH at this time, Q will go low after the 16th pulse edge following t_0.

The mutual constraints between the maximum operating frequency and the total delay in generating the M input signal can be deduced by considering an example. *Figure 3* shows an 11C83 driving the clock input of a 9LS161 Modulo-16 Counter. The table shows that the 9LS161 counts up from 5 to 8 and then presets back to 5 to repeat the sequence. Its Q_2 and Q_3 outputs drive the Preset Enable of the 9LS161 and the M input of the 11C83. The clock input of the 9LS161 responds to the positive-going edge of the 11C83 output and, thus, it is appropriate to evaluate delays from t_0 of *Figure 2*. The indicated t_{PLH} consists of a worst-case delay of 25 ns, plus the time to rise to the 1.3 V level at the 9LS161 input. For a stray capacitance of 10 pF, this rise will not exceed 10 ns. Thus the t_{PLH} in *Figure 2* will be 35 ns or less.

The worst-case t_{PLH} of the 9LS161, from CP to Q, is 20 ns with a 15 pF load and is measured to the 1.3 V level on the rising output. The Q_3 output must rise further, however, to reach the V_{IH} level of the M input, which is approximately 1.5 V below V_{CC}. This extra rise takes about 8 ns. Note that an external 2 kΩ pull-up resistor is shown in *Figure 3*. This provides additional HIGH state noise margin and also helps the Q_3 rise rate. This resistor also tends to increase the t_{PHL} of the 9LS161, as measured at the 1.3 V level, but this is not a critical timing factor because the falling Q_2 output is effectively in the LOW state as soon as it passes through the V_{IL} level of the 11C83 M input, at about 2.6 V.

For this example, the cumulative delays from t_0 of *Figure 2* are 35 ns t_{PLH} to the 9LS161 CP input plus 28 ns to the 11C83 M input. Adding 3 ns setup time for M preceding t_{15} gives a minimum time of 66 ns for the period of 15 pulses into the divide-by-31/32 circuit. But at a frequency of 1 GHz into the divide-by-8 circuit, the pulse frequency into the divide-by-31/32 is 125 MHz and 15 pulse periods constitute 120 ns. Thus the frequency limit for *Figure 3* is that of the 11C83 input, rather than the delays in the Mode Control feedback loop. A different result is obtained by replacing the 9LS161 with the F40161 CMOS equivalent. CMOS delays are measured between the 50% points, or 2.5 V with a 5 V supply. Thus the 11C83 output rise time is measured to the 2.5 V level rather than 1.3 V, which takes approximately 25 ns rather than 10 ns. The worst-case t_{PLH} of the F40161 is 185 ns to the 2.5 V level and the output rise from 2.5 V to 3.5 V takes another 5 ns. Substituting these numbers in the previous example gives 243 ns minimum for the period of 120 pulses into the divide-by-8. This gives an upper frequency limit of about 495 MHz. The frequency limit can be extended by using a logic inverter between the 11C83 output and the clock input of the F40161. This makes the F40161 trigger when the 11C83 output goes negative, rather than positive, which precedes t_0 by the period of 128 pulses into the divide-by-8. Since the 11C83 output falls to 2.5 V much faster than it rises, a CMOS inverter increases the total delay to only about 260 ns. This is the minimum period for 248 pulses into the divide-by-8, which translates to a maximum frequency of 955 MHz. Note that the 2 kΩ pull-up resistor of *Figure 3* is not required with the CMOS counter, nor is it desirable from the standpoint of loading the Q_2 output in the LOW state.

If an application requires a prescaler output HIGH signal level more positive than +5 V, it will be necessary to use a discrete transistor or some other type of interface circuit. The use of an external pull-up resistor returned to a higher voltage is not recommended, due to the possibility of causing latch-up in the output transistor. This voltage limitation is one of the trade-offs necessary to achieve transistors with the bandwidth required for 1 GHz counting.

The 11C83 clock input is one side of a differential switch whose other side is connected to an internally generated reference voltage. A 400 Ω internal resistor is connected between the clock input and reference voltage, as shown in *Figure 1*. This biases the input in the middle of the threshold region, which maximizes the input sensitivity and eliminates the need for external biasing resistors with capacitively coupled clocking. Also provided is a 10 kΩ resistor returned to V_{EE}. For ac coupled applications in which a clock signal is not always present, this resistor (pin 3) should be connected to the clock pin. This offsets the input sufficiently to avoid extreme sensitivity to noise when no signal is present. Otherwise, noise triggering can lead to oscillation at about 300 MHz. For dc coupled clocking the input signal levels should be designed to provide the specified V_{IH} and V_{IL} levels, which are nominally 2.5 V and 3.3 V below V_{CC}, respectively.

For a sinusoidal input waveform the minimum frequency of operation is about 50 MHz, due to edge rate limitations. Operation down to dc is possible provided that the input pulse edges have a slew rate of 50 V/μs or better. Minimum peak-to-peak trigger amplitude as a function of frequency is shown in *Figure 4*. Maximum recommended trigger amplitude is 1200 mV pk-pk. An rf bypass capacitor should be connected between V_{REF} (pin 6) and ground to maintain input sensitivity and to make the input impedance independent of internal switching. Input impedance is 54 Ω resistive at 1 GHz and has a capacitive component at lower frequencies, as shown in *Figure 5*. The 11C83 uses separate V_{CC} pins for the faster and slower parts of the circuit to prevent any interaction through the medium of lead inductance. The two V_{CC} pins should be connected together as close to the package as possible. Low impedance V_{CC} and V_{EE} (GND) distribution and rf bypass capacitors are recommended to prevent crosstalk with other circuits.

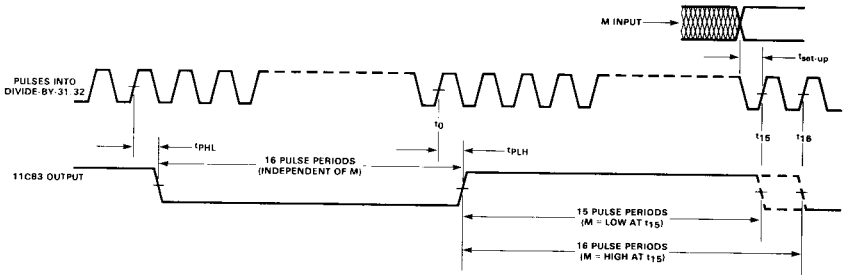


Fig. 2 Effect of M on Output Duty Cycle

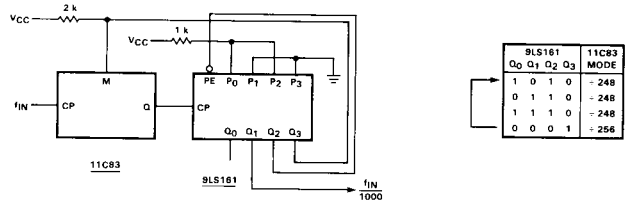


Fig. 3 Divide-by-1000 Obtained by Pulse-Swallowing

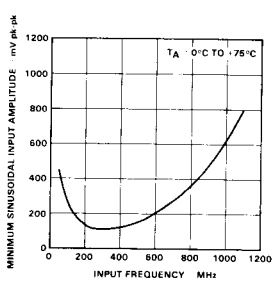


Fig. 4 AC Coupled Triggering Characteristics

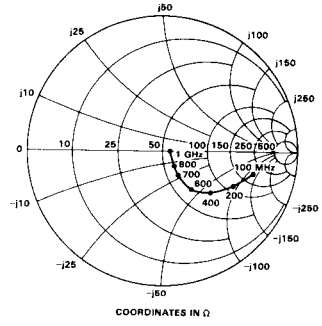


Fig. 5 High Frequency Input Characteristics

DC CHARACTERISTICS: Over operating temperature and voltage range unless otherwise specified: Pins 1 and 14 = V_{CC}, Pin 7 = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
V_{OH}	Output HIGH Voltage	2.7	3.6		V	V_{CC} = 4.75 V, I_{OH} = 240 μA
		3.5	4.2		V	V_{CC} = 4.75 V, I_{OH} = 10 μA
V_{OL}	Output LOW Voltage		0.4	0.5	V	V_{CC} = 4.75 V, I_{OL} = 10 mA
			0.33	0.4	V	V_{CC} = 4.75 V, I_{OL} = 5.0 mA
V_{IH}	Input HIGH Voltage at CP Input		2.40		V	T_A = 75°C
	(Note 3)		2.50		V	T_A = 25°C
			2.55		V	T_A = 0°C
V_{IL}	Input LOW Voltage at CP Input		1.60		V	T_A = 75°C
	(Note 3)		1.70		V	T_A = 25°C
			1.75		V	T_A = 0°C
V_{IH}	Input HIGH Voltage at M Input	3.58		V_{CC}	V	V_{CC} = 5.0 V, T_A = 75°C
	(Note 3)	3.40		V_{CC}	V	V_{CC} = 5.0 V, T_A = 25°C
		3.34		V_{CC}	V	V_{CC} = 5.0 V, T_A = 0°C
V_{IL}	Input LOW Voltage at M Input	GND		2.78	V	V_{CC} = 5.0 V, T_A = 75°C
	(Note 3)	GND		2.60	V	V_{CC} = 5.0 V, T_A = 25°C
		GND		2.54	V	V_{CC} = 5.0 V, T_A = 0°C
I_{IH}	Input HIGH Current at M			250	μA	V_{IN} = 3.4 V, T_A = 25°C
I_{IL}	Input LOW Current at M	0.5			μA	V_{IN} = 2.6 V, T_A = 25°C
I_{OS}	Output Short-Circuit Current	1.6		2.9	mA	V_{CC} = 5.0 V, T_A = 25°C
I_{CC}	Power Supply Current		100	130	mA	V_{CC} = 5.0 V, T_A = 25°C
V_{CC}	Operating Supply Voltage	4.75	5.0	5.5	V	T_A = 0°C to +75°C

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification, a copy of which may be obtained from Fairchild ECL Product Marketing, Mountain View, Ca.
2. Typical values are at V_{CC} = 5.0 V and T_A = 25°C.
3. The M and CP input thresholds are referenced to V_{CC}, and vary directly with V_{CC}. For example, raising V_{CC} by 0.2 V also raises the thresholds by 0.2 V.

AC CHARACTERISTICS: T_A = 0°C to +75°C, Pins 1 and 14 = +5.0 V, Pin 7 = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
f_{COUNT}	Maximum Sinusoidal Input Frequency	950	1100		MHz	ac coupled input, 800 mV pk-pk
f_{COUNT}	Minimum Sinusoidal Input Frequency		50		MHz	Note 1
SR_{MIN}	Minimum Slew Rate, Squarewave Input		50		V/μs	Note 2

NOTES:
1. Input drive shall not exceed 1.2 V pk-pk.
2. Operation at very low frequency is possible, provided that sufficient slew rate of the input pulse edge is maintained.

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