XRT8010

350MHZ CLOCK & CRYSTAL MULTIPLIER WITH LVDS OUTPUTS

DECEMBER 2002 *REV. P1.0.0*

DESCRIPTION

The XRT8010 is a monolithic analog phase locked loop that provides a high frequency LVDS clock output, using a low frequency crystal or reference clock. It is designed for SONET/SDH and other low jitter applications.The high performance of the IC provides a very low jitter LVDS clock output up to 350 MHz, while operating at 3.3 volts. The XRT8010 has a selectable 8x or 16x internal multiplier for an external crystal or signal source. The Output Enable pin provides a true disconnect for the LVDS output. The very compact (4 x 4 mm) low inductance package is ideal for high frequency operation.

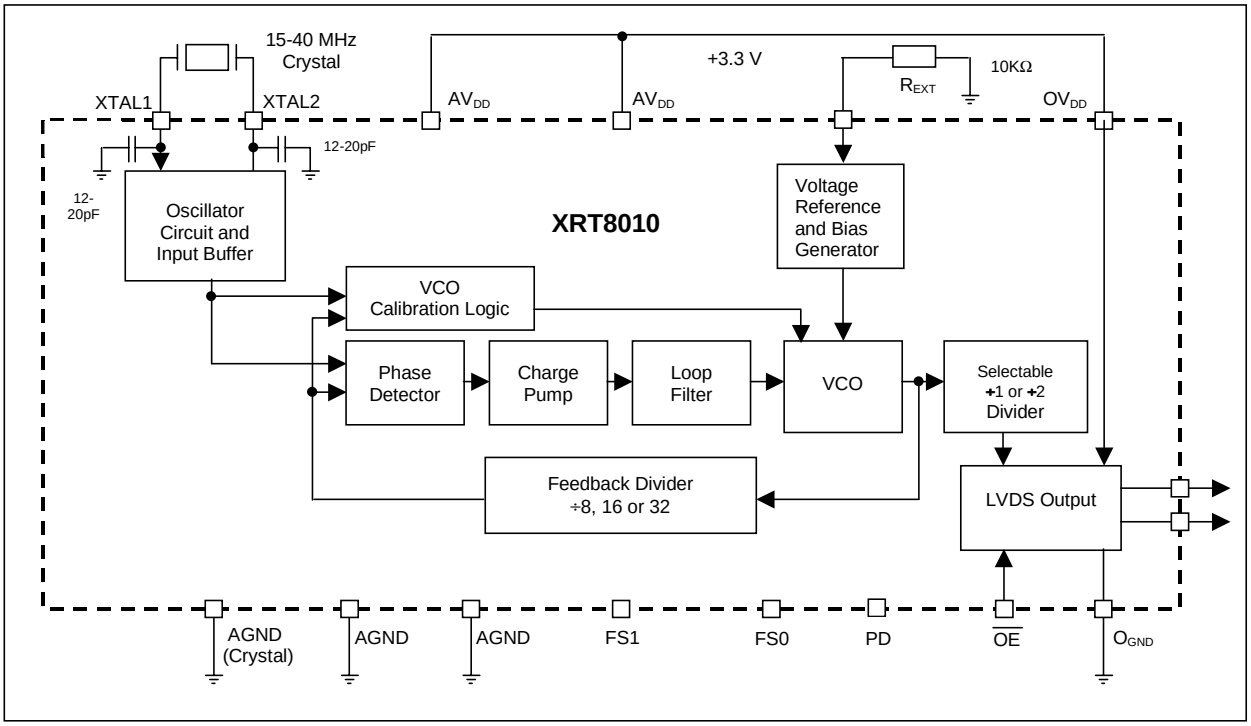
APPLICATIONS

- Gigabit Ethernet
- SONET/SDH
- SPI-4 Phase 2
- Voltage Controlled Crystal Oscillator (VCXO)
- 8x or 16x Clock Multiplier
  - Computer Systems
  - Telecommunication systems

FEATURES

- Up to 350 MHz operation
- Low Output Jitter:
  - 6 ps rms at 312 MHz, input referred
- On Chip Crystal Oscillator Circuit
  - Optimized for 15 to 40 MHz crystals
  - Uses parallel fundamental mode
- Selectable 8x or 16x multiplier
- Selectable ÷1 or ÷2 LVDS output
- LVDS output meets TIA/EIA 644A Specification (2001)
- 3.3V Low power CMOS: <80 mW typical
- -40°C to +85°C operating temperature
- Extremely small 16-lead QFN package

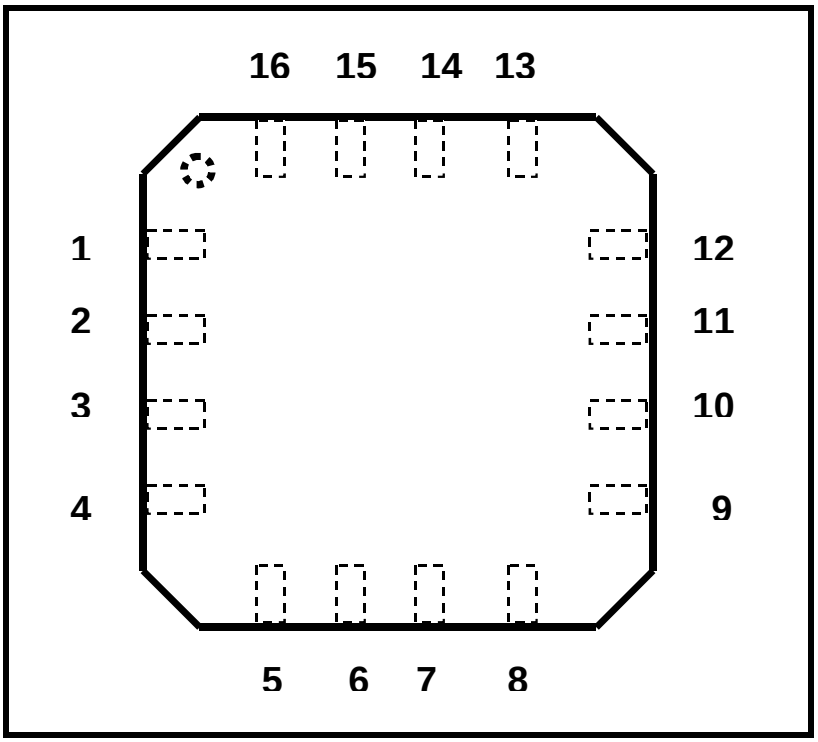
FIGURE 1. XRT8010 BLOCK DIAGRAM



XRT8010 PIN DESCRIPTION

PIN #	NAME	TYPE	DESCRIPTION
1	AVDD		+ 3.3V Analog Supply for Crystal Oscillator
2	AGND		Analog Ground for Crystal Oscillator
3	XTAL1	I	Crystal pin 1 or external clock input
4	XTAL2	O	Crystal pin 2 (output drive for crystal)
5	AGND		Analog Ground
6	REXT	I	External Bias Resistor (10KΩ to ground)
7	OE	I	Output Enable, Active low (Internal 50KΩ pull-down to ground)
8	PD	I	Power Down, Active High (Internal 50KΩ pull-down to ground)
9	FS1	I	Frequency select “1” (Internal 50KΩ pull-down to ground)
10	FS0	I	Frequency select “0” (Internal 50KΩ pull-up to VDD)
11	AGND		Analog Ground
12	OGND		Output Ground for LVDS outputs
13	OUTN	O	LVDS negative output for 50Ω line
14	OUTP	O	LVDS positive output for 50Ω line
15	OVDD		+ 3.3V Digital Supply for LVDS Output buffer
16	AVDD		+ 3.3V Analog Supply

FIGURE 2. PIN-OUT OF THE XRT8010 (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

Supply voltage	-0.5 to 6.0 V
VIN	-0.5 to 6.0 V
Storage Temperature	-65°C to + 150°C
Operating Temperature	-40°C to + 85°C
ESD	2,000 volts

ELECTRICAL SPECIFICATIONS:

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	VDD	3.0	3.3	3.6	V	
Supply current	IDD		20	25	mA	
Input Digital High	VINH	2.0			V	
Input Digital Low	VINL			0.8	V	
Crystal Frequency		15		40	MHz	Crystal Jitter < 1 ps p-p
Power on Calibration time				5	ms	After VDD reaches 2.8VNote: calibration time = 16,000 clock cycles
Max Frequency	FOUT	250		325	MHz	312 MHz nominal FOUT
Rise time	TR			300	ps	CL = 5pF, RL = 100Ω
Fall Time	TF			300	ps	CL = 5pF, RL = 100Ω
Duty cycle		45		55	%	LVDS output
Output skew				10	ps	Differential
Output Loading			100		Ω	
Output voltage		-400		400	mV	Differential (OUTP-OUTN)
Common Mode Voltage	VCM		1.2		V	
Output short circuit current			-5.7	-8	mA	Current limit to ground, VDD or Vp to Vn
Output Jitter, Cycle-to-cycle			6	10	ps	rms, at 312 MHz, Input referred
Output Jitter, Accumulated			16	20	ps	rms, over 1,000 cycles, at 312 MHz
Crystal Frequency Range		15		40	MHz	Fundamental Mode Crystal

FIGURE 3. LVDS OUTPUT WAVEFORMS AND TEST CIRCUITS

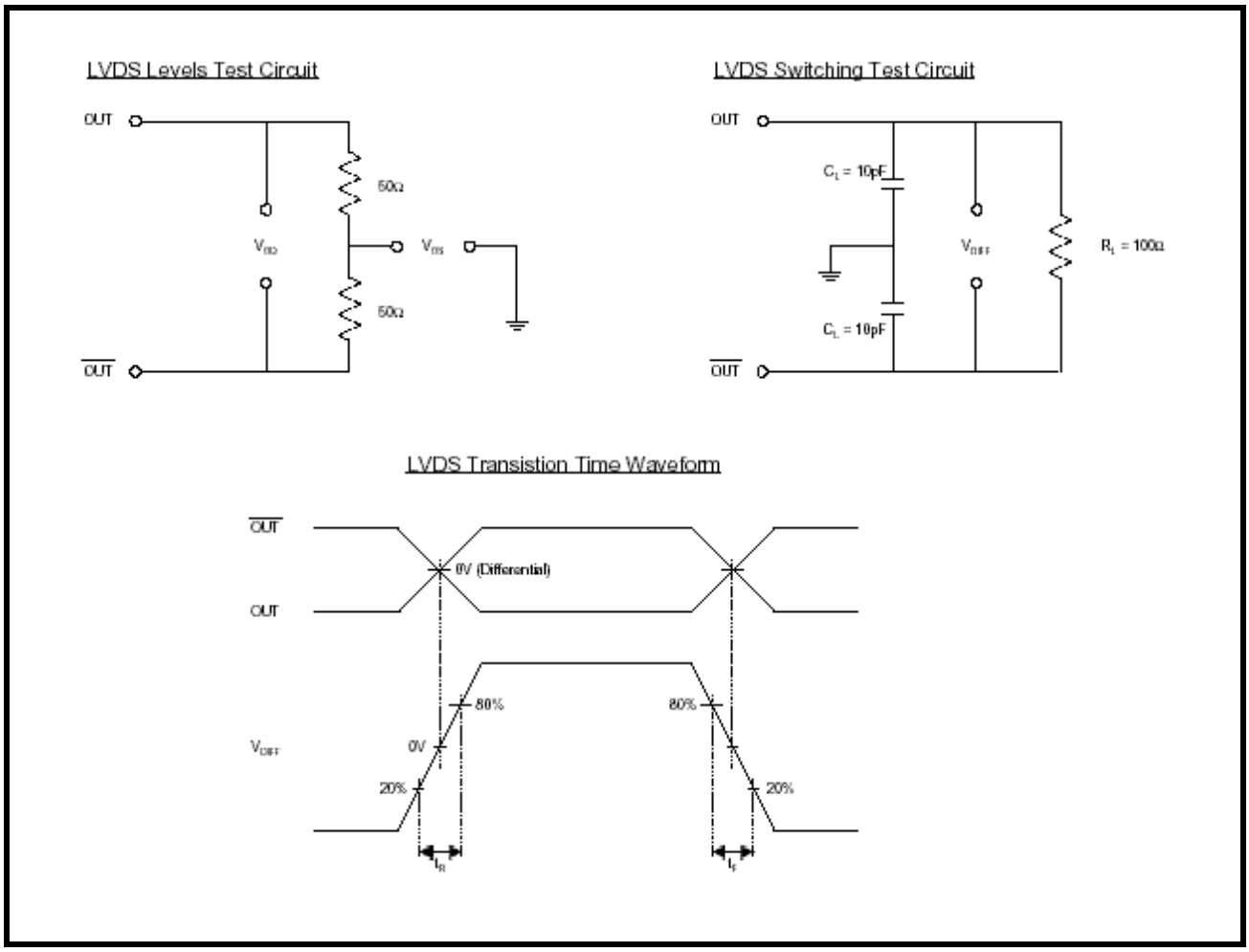


TABLE 1: FREQUENCY SELECTION TABLE

FS0PIN 10	FS1PIN 9	CRYSTAL FREQUENCY	INTERNAL CAPACITOR	MULTIPLY RATIO	OUTPUT DIVIDE	FREQUENCY OUTPUT
1	1	39.0 MHz	12 pF	8x	1	312 MHz
0	1	39.0 MHz	12 pF	8x	2	156 MHz
1	0	19.5 MHz	20 pF	16x	1	312 MHz
0	0	19.5 MHz	20 pF	16x	2	156 MHz

NOTES:

1. *Use Parallel Fundamental mode crystal*
2. *FS0 has a 50KΩ pull-up resistor to VDD on chip*
3. *FS1 has a 50KΩ pull-down resistor to ground on chip*

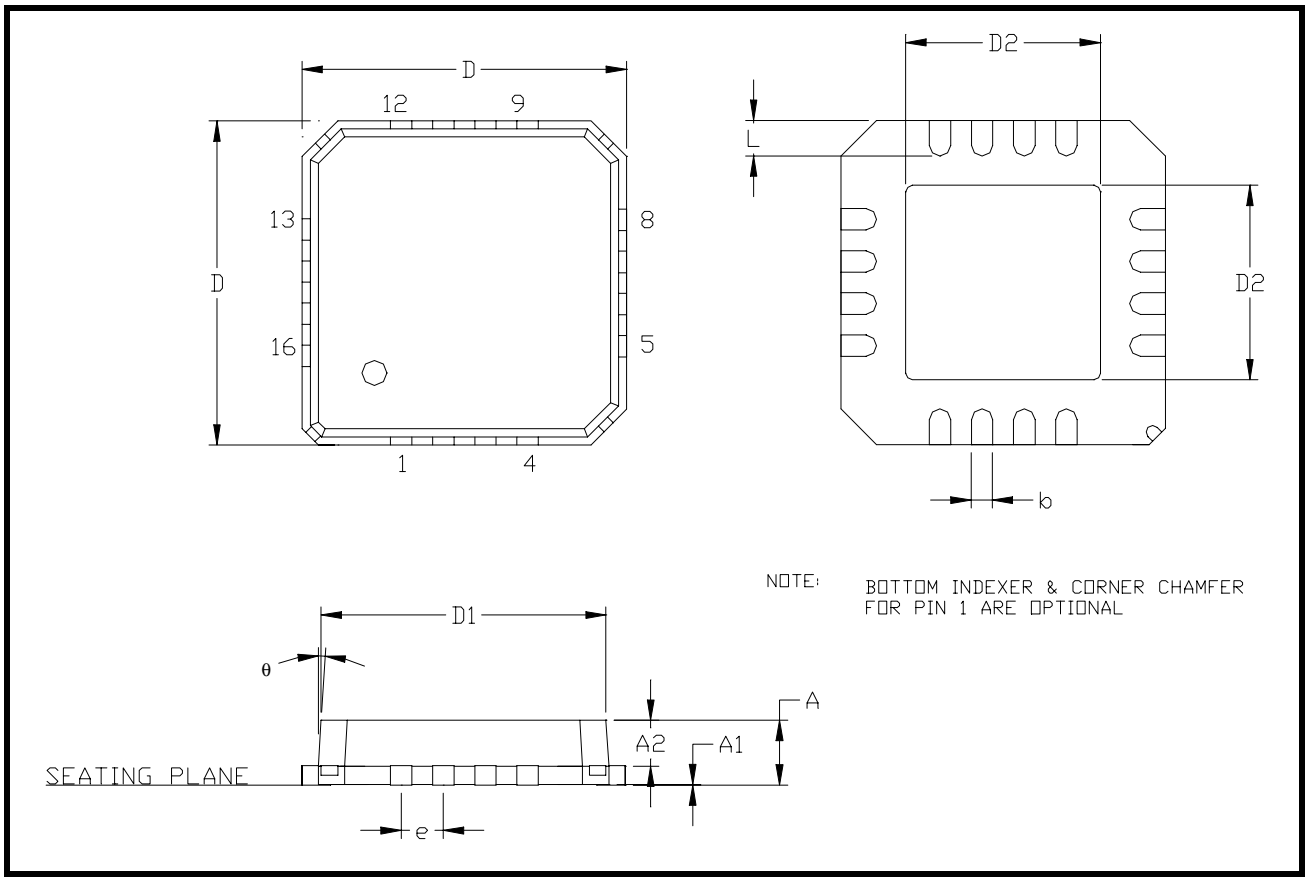
TABLE 2: POWER-DOWN AND OUTPUT TRI-STATE SELECTION TABLE

PD PIN 8	OE PIN 7	STATUS	NOTES
1	X	Outputs tri-stated and chip Powered-down	"X" = don't care
0	1	Output tri-stated	PD and OE have a 50KΩ pull-down resistor to ground on chip

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT8010IL	16 LEAD QUAD FLAT NO LEAD (4 mm x 4 mm, QFN)	-40°C to +85°C

FIGURE 4. 16-PIN QFN PACKAGE OUTLINE DRAWING AND DIMENSIONS



Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.039	0.80	1.00
A1	0.000	0.002	0.00	0.05
A2	0.000	0.039	0.00	1.00
D	0.154	0.161	3.90	4.10
D1	0.144	0.152	3.65	3.85
D2	0.030	0.089	0.75	2.25
b	0.009	0.015	0.23	0.38
e	0.0256 BSC		0.65 BSC	
L	0.014	0.030	0.35	0.75
θ	0°	12°	0°	12°

NOTES

NOTICE

Datasheet December 2002.