PRELIMINARY

16-CHARACTER 2-LINE DOT MATRIX LCD CONTROLLER DRIVER with Icon Display

■ GENERAL DESCRIPTION

The **NJU6636** is a Dot Matrix LCD controller driver for 16-character 2-line display with icon display in single chip. It contains voltage converter and regulator, bleeder resistor, CR oscillator, microprocessor Interface circuits, Instruction decoder controller, character generator ROM/RAM and common and segment drivers.

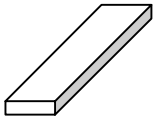
The external power supply circuit is simplified by using the bleeder resistance to generate the bias level of LCD driving voltage internally.

The microprocessor Interface circuits which operate 2MHz frequency, can be connected directly to serial or 8bit microprocessor.

The character generator consists of 9,600 bits ROM and 64 x 5 bits RAM. The standard version ROM is coded with 240 characters including capital and small letter fonts.

The 17-common (16 for character, 2 for icon) and 80-segment drive up to 16-character 2-line with 80 Icon LCD panel which divided two common electrode blocks.

■ PACKAGE OUTLINE



NJU6636CJ

■ FEATURES

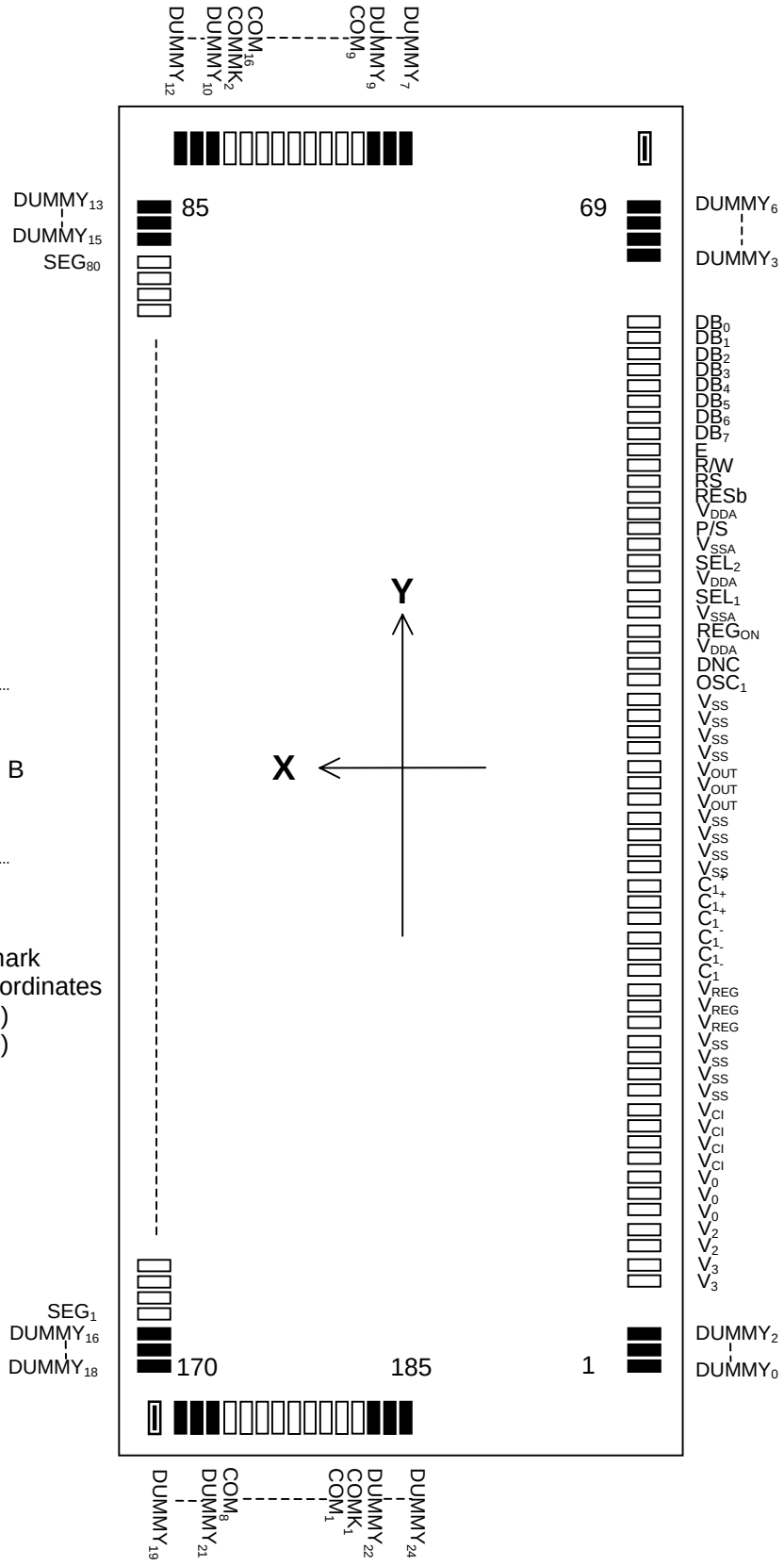
- 16-character 2-line Dot Matrix LCD Controller Driver
- Maximum 80 Icon Display
- Serial, 8 Bi t Microprocessor direct Interface
- Display Data RAM :32 x 8 bits : Maximum 16-character 2line Display
- Character Generator ROM :9,600 bits ; 240 characters for 5 x 8 dots
- Character Generator RAM :64 x 5 bits ; 8 Patterns(5 x 8 dots)
- Icon Display RAM :16 x 5 bits ; Maximum 80 icon
- Microprocessor direst accessing to Display Data RAM and Character Generator RAM
- High Voltage LCD Driver :17-common / 80-segment
- Duty Ratio :1/9, 1/17 Duty (Programmable) and 1/5 bias
- Useful Instruction Set :Clear Display, Returns Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift
- Power On Reset / Hardware Reset Function
- Voltage regulator on chip (software contrast control : 8 Step)
- Oscillation Circuit on chip
- Bleeder Resistor on chip (Mask Option)

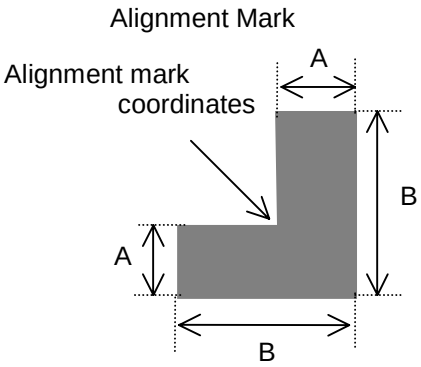
Version	Bleeder Resistor(V_0 to V_{SS})
NJU6636A	40kΩ (Typ.) : 1/5 Bias
NJU6636B	20kΩ (Typ.) : 1/5 Bias

- Low Power Consumption (Power down function)
- Common and Segment driver Location order Select Function (SEL1 & SEL2 Terminal)
- Operating Voltage --- +2.4 to 5.5V (Except LCD Driving Voltage)
- LCD Driving Voltage --- 6.0V Max.
- Package Outline --- Bumped Chip
- C-MOS Technology (P-sub)

■ PAD LOCATION

Mode A (TOP VIEW) SEL_1=0, SEL_2=0





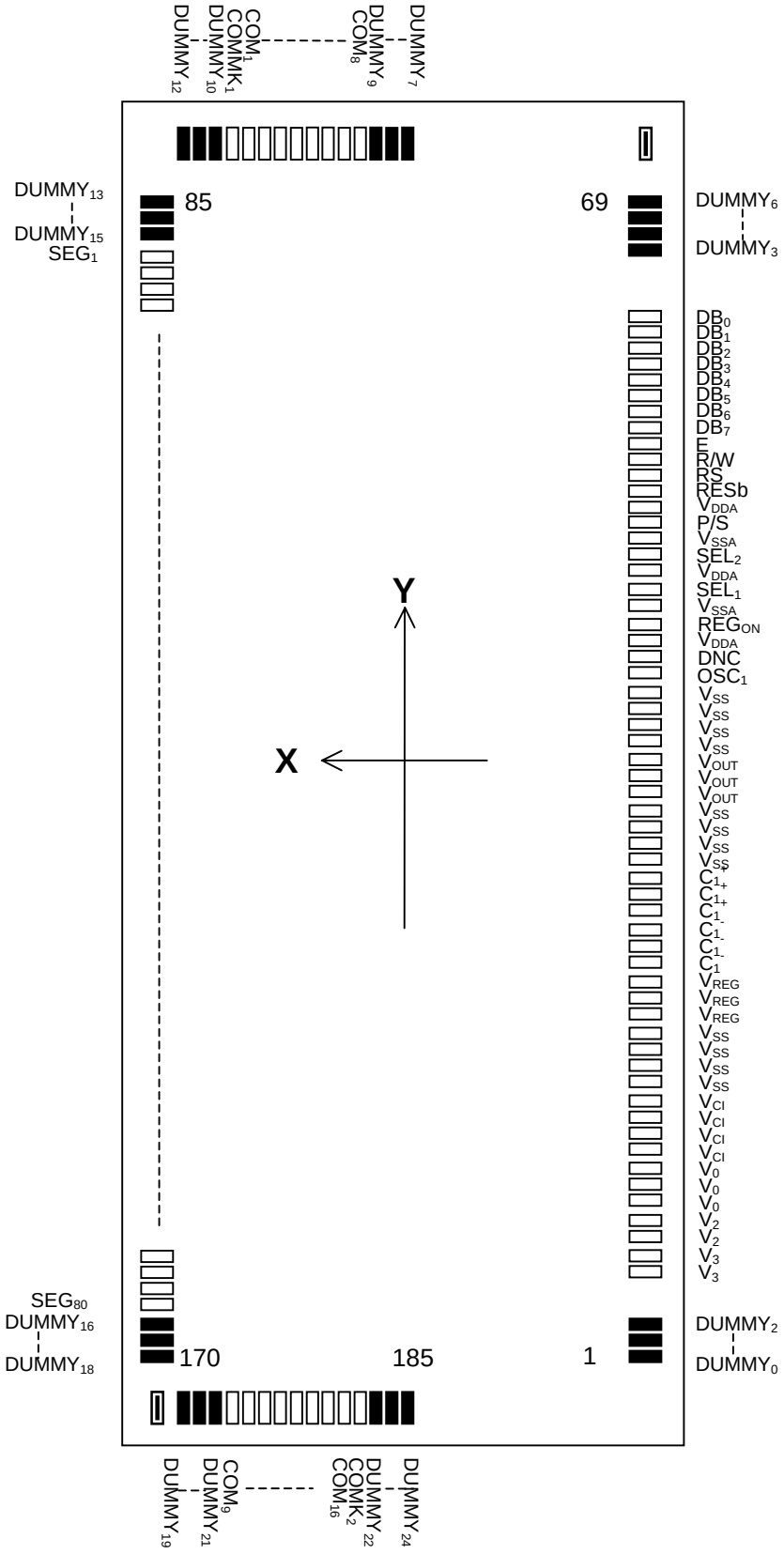
A : 25um
B : 50um

Alignment mark coordinates
(-2495, 878)
(2495, -878)

Chip Size : 5.33 x 2.08mm
Chip Center : X=0μm, Y=0μm
Bump Size : 35 x 104μm
Bump Height : 17.5um (Typ.)
Bump Material : Au

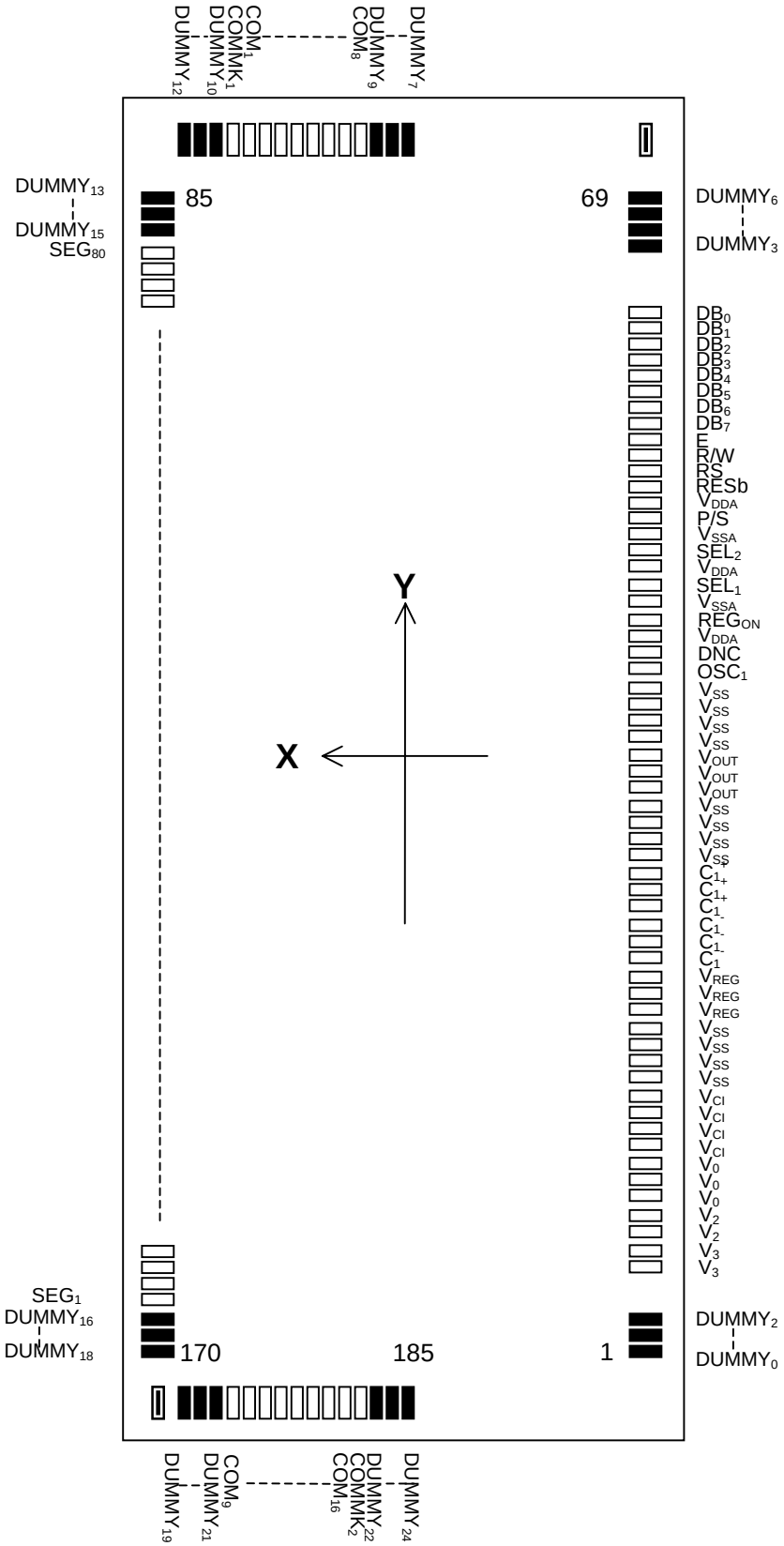
Note) A mode setup is decided by the combination of SEL_1 and SEL_2 terminals.

Mode B (TOP VIEW) SEL_1=1, SEL_2=1



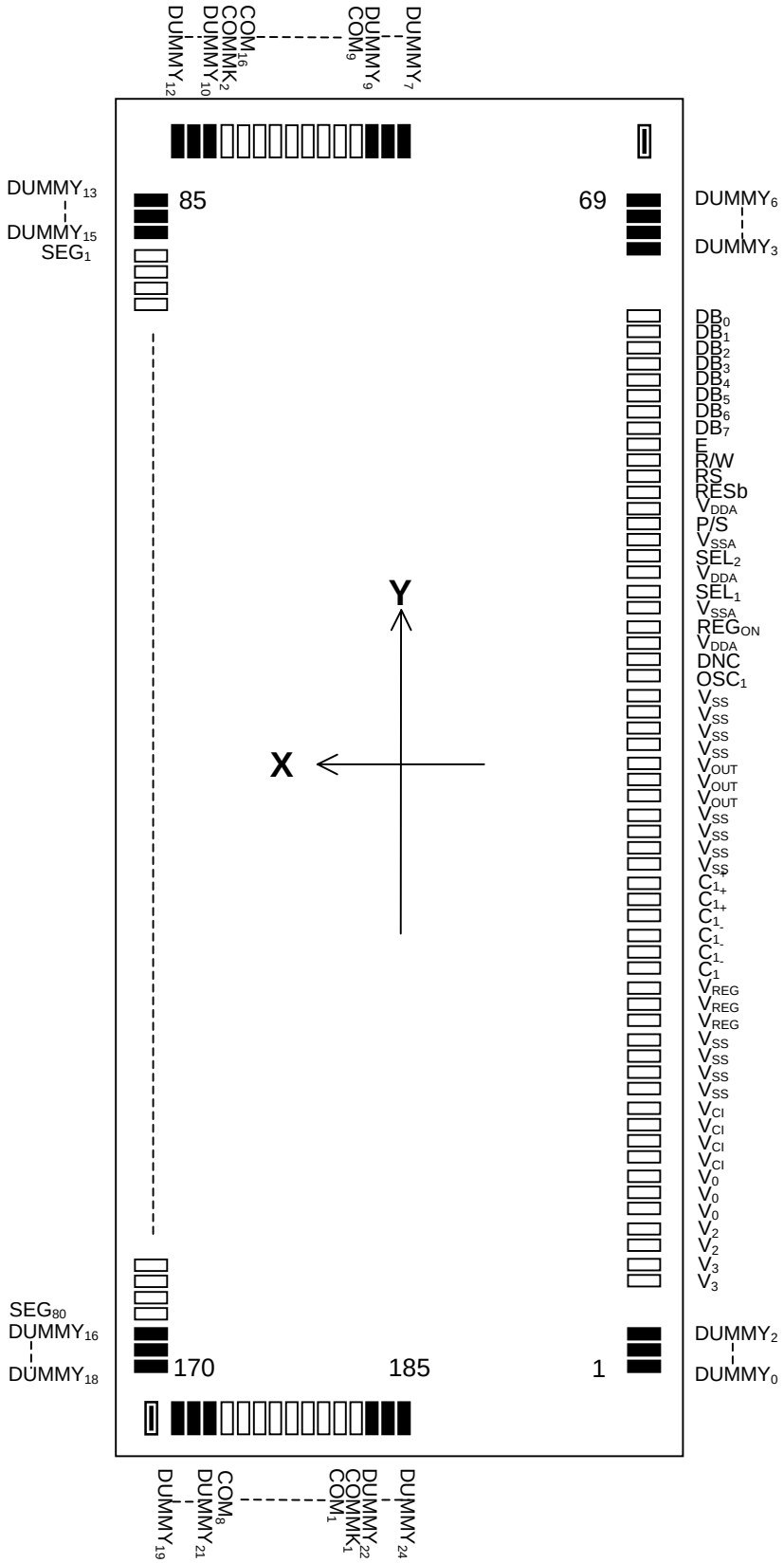
Note) A mode setup is decided by the combination of SEL_1 and SEL_2 terminals

Mode C (TOP VIEW) SEL_1=1, SEL_2=0



Note) A mode setup is decided by the combination of SEL_1 and SEL_2 terminals

Mode D(TOP VIEW) SEL_1=0, SEL_2=1



Note) A mode setup is decided by the combination of SEL_1 and SEL_2 terminals

■ PAD COORDINATES 1

Chip Size(5330μm X 2080μm)

PAD No.	Terminal	X= μm	Y= μm
1	$DUMMY_0$	-2503	-891
2	$DUMMY_1$	-2448	-891
3	$DUMMY_2$	-2393	-891
4	V_3	-2283	-891
5	V_3	-2228	-891
6	V_2	-2063	-891
7	V_2	-2008	-891
8	V_0	-1953	-891
9	V_0	-1898	-891
10	V_0	-1843	-891
11	V_{CI}	-1788	-891
12	V_{CI}	-1733	-891
13	V_{CI}	-1678	-891
14	V_{CI}	-1623	-891
15	V_{SS}	-1568	-891
16	V_{SS}	-1513	-891
17	V_{SS}	-1458	-891
18	V_{SS}	-1403	-891
19	V_{REG}	-1348	-891
20	V_{REG}	-1293	-891
21	V_{REG}	-1238	-891
22	C_1^-	-1183	-891
23	C_1^-	-1128	-891
24	C_1^-	-1073	-891
25	C_1^+	-963	-891
26	C_1^+	-908	-891
27	C_1^+	-853	-891
28	V_{SS}	-798	-891
29	V_{SS}	-743	-891
30	V_{SS}	-688	-891
31	V_{SS}	-633	-891
32	V_{OUT}	-578	-891
33	V_{OUT}	-523	-891
34	V_{OUT}	-468	-891
35	V_{DD}	-413	-891
36	V_{DD}	-358	-891
37	V_{DD}	-303	-891
38	V_{DD}	-248	-891
39	V_{SS}	-193	-891
40	V_{SS}	-138	-891
41	V_{SS}	-83	-891
42	V_{SS}	-28	-891
43	OSC_1	28	-891
44	DNC	138	-891
45	V_{DDA}	248	-891
46	REG_{ON}	303	-891
47	V_{SSA}	413	-891
48	SEL_1	468	-891
49	V_{DDA}	578	-891
50	SEL_2	633	-891

PAD No.	Terminal	X= μm	Y= μm
51	V_{SSA}	743	-891
52	PS	798	-891
53	V_{DDA}	908	-891
54	RESb	963	-891
55	RS	1073	-891
56	RW	1183	-891
57	E	1293	-891
58	DB_7	1403	-891
59	DB_6	1513	-891
60	DB_5	1623	-891
61	DB_4	1733	-891
62	DB_3	1843	-891
63	DB_2	1953	-891
64	DB_1	2063	-891
65	DB_0	2173	-891
66	$DUMMY_3$	2228	-891
67	$DUMMY_4$	2283	-891
68	$DUMMY_5$	2338	-891
69	$DUMMY_6$	2393	-891
70	$DUMMY_7$	2516	-142
71	$DUMMY_8$	2516	-87
72	$DUMMY_9$	2516	-32
73	COM_9	2516	23
74	COM_{10}	2516	78
75	COM_{11}	2516	133
76	COM_{12}	2516	188
77	COM_{13}	2516	243
78	COM_{14}	2516	298
79	COM_{15}	2516	353
80	COM_{16}	2516	408
81	COM_{MK2}	2516	463
82	$DUMMY_{10}$	2516	518
83	$DUMMY_{11}$	2516	573
84	$DUMMY_{12}$	2516	628
85	$DUMMY_{13}$	2338	891
86	$DUMMY_{14}$	2283	891
87	$DUMMY_{15}$	2228	891
88	SEG_{80}	2173	891
89	SEG_{79}	2118	891
90	SEG_{78}	2063	891
91	SEG_{77}	2008	891
92	SEG_{76}	1953	891
93	SEG_{75}	1898	891
94	SEG_{74}	1843	891
95	SEG_{73}	1788	891
96	SEG_{72}	1733	891
97	SEG_{71}	1678	891
98	SEG_{70}	1623	891
99	SEG_{69}	1568	891
100	SEG_{68}	1513	891

■ PAD COORDINATES 2

PAD No.	Terminal	X= µm	Y= µm
101	SEG_{67}	1458	891
102	SEG_{66}	1403	891
103	SEG_{65}	1348	891
104	SEG_{64}	1293	891
105	SEG_{63}	1238	891
106	SEG_{62}	1183	891
107	SEG_{61}	1128	891
108	SEG_{60}	1073	891
109	SEG_{59}	1018	891
110	SEG_{58}	963	891
111	SEG_{57}	908	891
112	SEG_{56}	853	891
113	SEG_{55}	798	891
114	SEG_{54}	743	891
115	SEG_{53}	688	891
116	SEG_{52}	633	891
117	SEG_{51}	578	891
118	SEG_{50}	523	891
119	SEG_{49}	468	891
120	SEG_{48}	413	891
121	SEG_{47}	358	891
122	SEG_{46}	303	891
123	SEG_{45}	248	891
124	SEG_{44}	193	891
125	SEG_{43}	138	891
126	SEG_{42}	83	891
127	SEG_{41}	28	891
128	SEG_{40}	-28	891
129	SEG_{39}	-83	891
130	SEG_{38}	-138	891
131	SEG_{37}	-193	891
132	SEG_{36}	-248	891
133	SEG_{35}	-303	891
134	SEG_{34}	-358	891
135	SEG_{33}	-413	891
136	SEG_{32}	-468	891
137	SEG_{31}	-523	891
138	SEG_{30}	-578	891
139	SEG_{29}	-633	891
140	SEG_{28}	-688	891
141	SEG_{27}	-743	891
142	SEG_{26}	-798	891
143	SEG_{25}	-853	891
144	SEG_{24}	-908	891
145	SEG_{23}	-963	891
146	SEG_{22}	-1018	891
147	SEG_{21}	-1073	891
148	SEG_{20}	-1128	891
149	SEG_{19}	-1183	891
150	SEG_{18}	-1238	891

PAD No.	Terminal	X= µm	Y= µm
151	SEG_{17}	-1293	891
152	SEG_{16}	-1348	891
153	SEG_{15}	-1403	891
154	SEG_{14}	-1458	891
155	SEG_{13}	-1513	891
156	SEG_{12}	-1568	891
157	SEG_{11}	-1623	891
158	SEG_{10}	-1678	891
159	SEG_{9}	-1733	891
160	SEG_{8}	-1788	891
161	SEG_{7}	-1843	891
162	SEG_{6}	-1898	891
163	SEG_{5}	-1953	891
164	SEG_{4}	-2008	891
165	SEG_{3}	-2063	891
166	SEG_{2}	-2118	891
167	SEG_{1}	-2173	891
168	$DUMMY_{16}$	-2228	891
169	$DUMMY_{17}$	-2283	891
170	$DUMMY_{18}$	-2338	891
171	$DUMMY_{19}$	-2516	628
172	$DUMMY_{20}$	-2516	573
173	$DUMMY_{21}$	-2516	518
174	COM_{8}	-2516	463
175	COM_{7}	-2516	408
176	COM_{6}	-2516	353
177	COM_{5}	-2516	298
178	COM_{4}	-2516	243
179	COM_{3}	-2516	188
180	COM_{2}	-2516	133
181	COM_{1}	-2516	78
182	COM_{MK1}	-2516	23
183	$DUMMY_{22}$	-2516	-32
184	$DUMMY_{23}$	-2516	-87
185	$DUMMY_{24}$	-2516	-142
186			
187			
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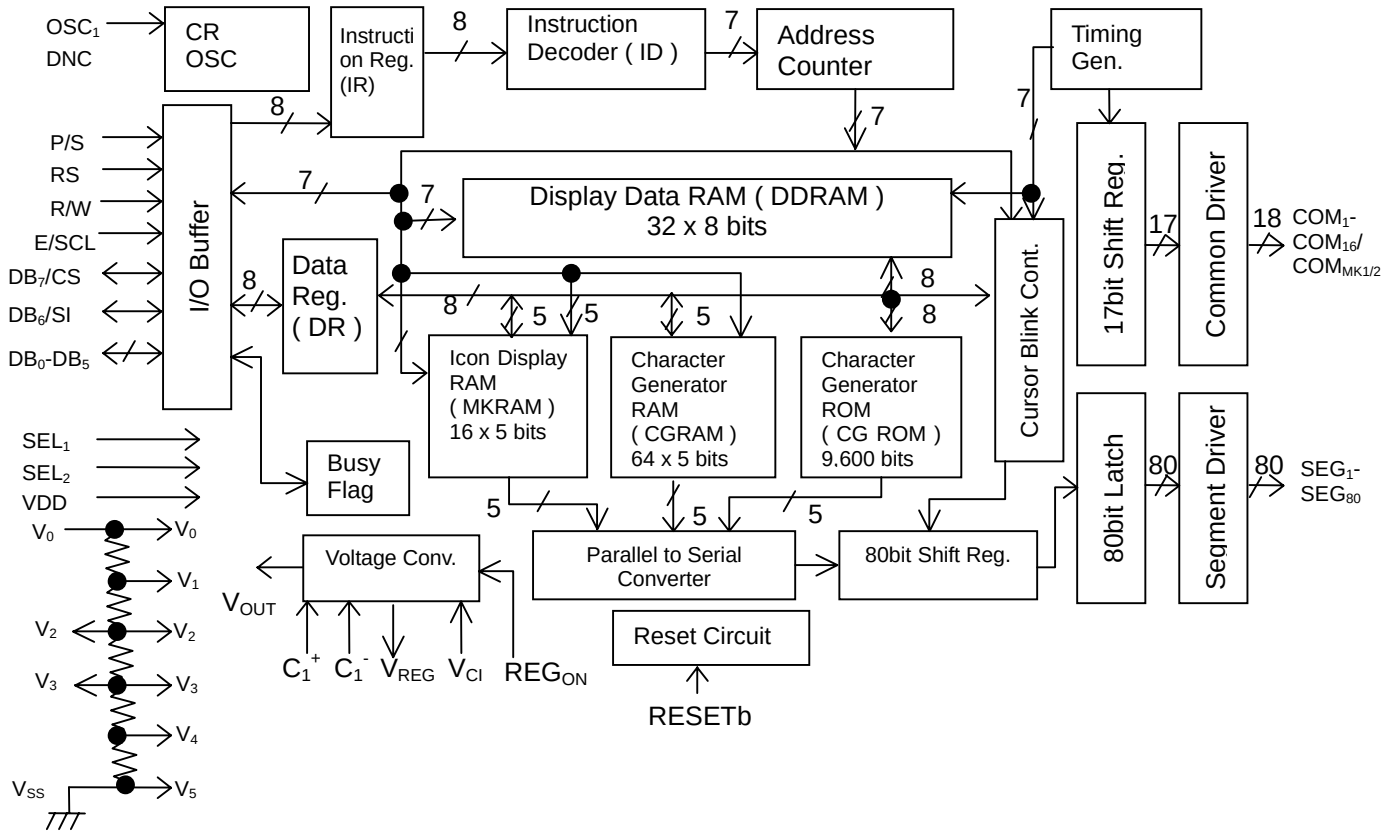
198			
199			
200			

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

PAD No	SYMBOL	I/O	FUNCTION
35-38 15-18 28-31 39-42	V_{DD}, V_{SS}	–	Power Source : V_{DD} = 2.4 to 5.5V, GND : V_{SS} = 0V
45,49 53 47,51	V_{DDA}, V_{SSA}	–	These terminals are internally connected to the V_{DD} and V_{SS} level. These terminals are used to fix the selection terminals to the V_{DD} and V_{SS} level. V_{SSA} should be open if not using. Note) Do not use this terminal for a main power supply.
4-5 6-7 8-10	V_0, V_2, V_3	–	LCD Driving Voltage
43	OSC_1	I	System clock input terminal This terminal should be open for internal clock operation.
44	DNC	–	DNC terminal This terminal should be open.
52	P/S	I	Parallel or serial interface selection terminal “L” : Serial interface / “H” : Parallel interface
55	RS	I	Resister selection signal Input "0":Instruction Resister (Writing) Busy Flag (Reading) "1":Data Register (Writing / Reading)
56	R/W	I	Read/Write selection signal Input "0":Write "1":Read In serial interface mode, only data writing is available. And at the same time, R/W pin shall be fixed at V_{SS}.
57	E	I	Read/write activation Signal Input in parallel mode
	SCL	I	Shift clock input in serial mode
58	DB_7	I/O	3-state Data Bus for Upper bit to transfer the data between MPU and **NJU6636** in Parallel operation mode. DB_7 is also Interface, “1” : Parallel Interface
	CS	I	Chip select signal input Serial operation mode
59	DB_6	I	3-state Data Bus for Upper bit to transfer the data between MPU and NJU6636 in Parallel operation mode.
	SIO	I	Data input terminal in Serial operation mode
60-65	DB_5– DB_0	I/O	3-state Data Bus for Lower 6bit to transfer the data between MPU and NJU6636 in Parallel operation mode. When the serial operation mode, these terminal should be open.
48	SEL1	I	Common driver location order select terminal
50	SEL2	I	Segment driver location order select terminal
73-80 174-181	COM_1 – COM_{16}	O	LCD Common driving signal output terminals
81, 182	$COMMK_{1,2}$	O	Icon Common driving signal output terminals
88-167	SEG_1 – SEG_{80}	O	LCD Segment driving signal output terminals

PAD No	SYMBOL	I/O	FUNCTION
22-24 25-17	$C1^+$, $C1^-$	I/O	Capacitor for Voltage Converter Connecting terminal
11-14	V_{CI}	I	Voltage regulator input terminal
46	REG_{ON}	I	Voltage regulator select terminal. REG_{ON} = “H” (Voltage regulator ON) / ”0” (Voltage regulator OFF)
19-21	V_{REG}	O	Voltage regulator output Terminal This terminal internally connected Voltage Converter input terminal. Decupling capacitor should be connected between V_{REG} and V_{SS}. (C=1µF)
32-34	V_{OUT}	O	Voltage Converter Output Terminal
54	RESETb	I	Reset Terminal When the “L” level input over than 1.5ms to this terminal, the system will be reset.
1-3 66-72 82-87 168-173 183-185	$DUMMY_{0-24}$	–	Dummy Terminal These terminal are electrically open.

■ FUNCTIONAL DESCRIPTION

(1) Description for each blocks

(1-1) Register

The **NJU6636** incorporates two 8-bit registers, an Instruction Register (IR) and a Data Register (DR).
The Register (IR) stores Instruction codes such as "Clear Display" and "Return Home", and address data for Display Data RAM (DD RAM) and Character Generator RAM (CG RAM). The MPU can write the Instruction code and address data to the Register (IR), but it can not read out from the Register (IR).
The Register (DR) is a temporary storing register, the data in the Register (DR) is written into the DD RAM or CG RAM and read out from the DD RAM or CG RAM.
The data in the Register (DR) written by the MPU is transferred from the Register automatically to the DD RAM or CG RAM by Internal operation.
After reading the data in the Register (DR) by the MPU, the next address data in the DD RAM or CG RAM is transferred automatically to the Register (DR) for the next MPU reading.
These two registers are selected by the selection signal RS as shown below:

Table 1. Register operation control by RS and R/W signals.

Table 1. Register Operation

RS	R/W	Operation
0	0	Write
0	1	Read busy flag (DB_7) and address counter (DB_0 to DB_6)*
1	0	Write (DR to DD RAM, CG RAM or MK RAM)
1	1	Read (DD RAM, CG RAM or MK RAM to DR)*

* Using Parallel Interface

(1-2) Busy Flag (BF)

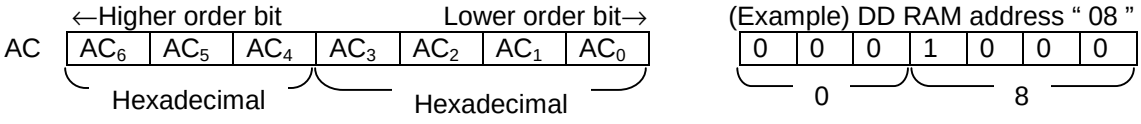
When the internal circuits are operating, the busy flag is "1", and any instruction reading is inhibited.
The busy flag (BF) is output from DB_7 when RS="0" and R/W="1" as shown in table 1.
The next instruction should be written after busy flag (BF) goes to "0". (Using Parallel Interface)

(1-3) Address Counter(AC)

The address Counter (AC) addresses the DD RAM and CG RAM.
When the address setting instruction is written into the Register (IR), the address information is transferred from Register (IR) to the counter (AC). The selection of either the DD RAM or CG RAM is also determined by this instruction.
After writing (or reading) the display data to (or from) the DD RAM or CG RAM, the counter (AC) increments (or decrements) "1" automatically.
The address data in the Counter (AC) is output from DB_6 to DB_0 when RS="0" and R/W="1" as shown in table 1. (Using Parallel Interface)

(1-4) Display Data RAM (DD RAM)

The display data RAM (DD RAM) consisting of 32 x 8 bits stores up to 32-character display data represented in 8-bit code.
The DD RAM address data set in the address Counter (AC) is represented in hexadecimal.



The relation between DD RAM address and display position on the LCD is shown below.

- 16 character / 2 line Display

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	←Display Position
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	←DD RAM Address
2nd line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	(Hexadecimal)

The relation between DD RAM address and display position on the LCD shown below.

[Left Shift Display]

(00) ←	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
(10) ←	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	00

[Right Sift Display]

1F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	→ (0F)
0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	→ (1F)

(1-5) Character Generator ROM(CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 8 dots character pattern represented in 8-bit character codes. The storage capacity is up to 240 kinds of 5 x 8 dots character pattern. The correspondence between character code and standard character pattern is shown in Table 2.

User-defined character pattern (Custom Font) are also available by mask option.

Table 2. CG ROM Character Pattern (ROM version –02)

Lower 4 bit (Hexadecimal) \ Upper 4 bit (Hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1	(02)															
2	(03)															
3	(04)															
4	(05)															
5	(06)															
6	(07)															
7	(08)															
8																
9																
A																
B																
C																
D																
E																
F																

(1-6) Character Generator RAM

The character generator RAM (CG RAM) stores any kinds of character pattern in 5 x 8 dots written by the user program to display user's original character pattern. The CG RAM stores 4 kinds of character in 5 x 8 dots mode.
To display user's original character pattern stored in the CG RAM, the address data $(00)_H$ – $(07)_H$ should be written to the DD RAM as shown in Table 3.
Table 3. shows the correspondence among the character pattern, CG RAM address and data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern (5 x 8 dots)

Character Code (DD RAM Data)	CG RAM Address			Character Pattern (CG RAM Data)	
7 6 5 4 3 2 1 0 ← → Upper bit Lower bit	6 5 4 3 2 1 0 ← → Upper bit Lower bit			4 3 2 1 0 ← → Upper bit Lower bit	
0 0 0 0 ∗ 0 0 0	1 0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 1 0 0 0 0 0	Character Pattern Example (1) ←Cursor Position
0 0 0 0 ∗ 0 0 1	1 0 0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		1 0 0 0 1 0 1 0 1 0 1 1 1 1 1 0 0 1 0 0 1 1 1 1 1 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0	Character Pattern Example (2) ← Cursor Position
		0 0 0 0 0 1			
•	•	•		•	
•	•	•		•	
•	•	•		•	
•	•	•		•	
•	•	•		•	
0 0 0 0 ∗ ∗ 1 1	1 1 1 1	1 0 0 1 0 1 1 1 0 1 1 1			

Notes:
1. Character code bits 0 to 2 correspond to the CG RAM address 3 to 5 (3bits : 8 patterns).
2. CG RAM address 0, 1 and 2 designate a character pattern line position.
   The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the data of 8th line should be "0".
   If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position corresponding to the CG RAM data bits 0 to 4 are all shown above. The bits 5 to 7 of the CG RAM do not exist.
4. CG RAM character patterns are selected when character code bits 4 to 7 are all "0" and addressed by character code bits 0 and 1.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.
6. After power ON or hardware reset, the contents of CG RAM can not be initialized, be sure to set the RAM before display ON.

(1-7) Icon Display RAM (MK RAM)

The NJU6636 can display maximum 80 Icons.
The Icon Display can be controlled by writing the data in MK RAM corresponds to the Icon.
The relation between MK RAM address and Icon Display position is shown in Table 4.

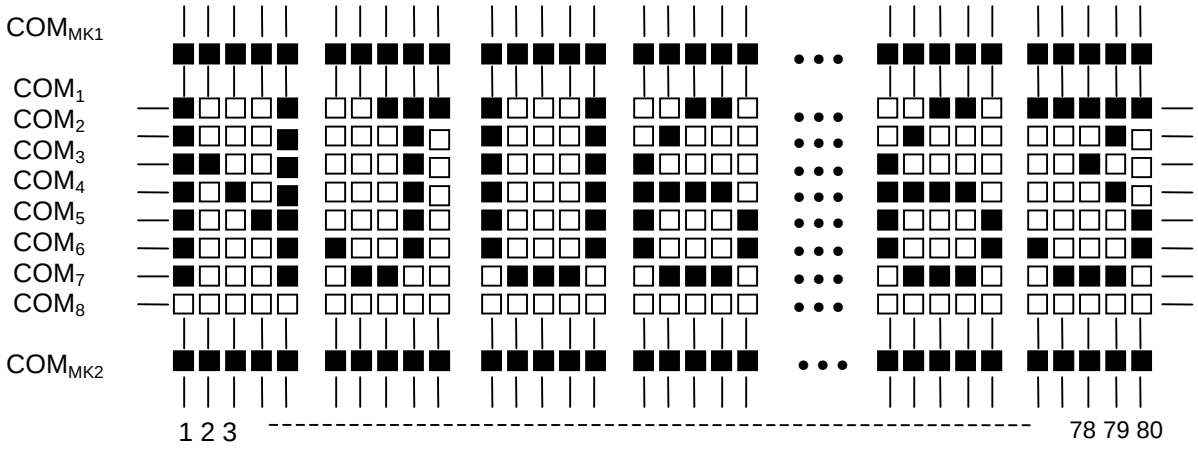


Table 4. Correspondence among Icon Position, MK RAM Address Data

MK RAM Address (20_H to $2F_H$)		Bits for Icon Display Position							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0010 0000	20_H	*	*	*	1	2	3	4	5
0010 0001	21_H	*	*	*	6	7	8	9	10
0010 0010	22_H	*	*	*	11	12	13	14	15
0010 0011	23_H	*	*	*	16	17	18	19	20
0010 0100	24_H	*	*	*	21	22	23	24	25
.	.								
0010 1100	$2C_H$	*	*	*	60	61	62	63	64
0010 1101	$2D_H$	*	*	*	65	66	67	68	69
0010 1110	$2E_H$	*	*	*	70	71	72	73	74
0010 1111	$2F_H$	*	*	*	75	76	78	79	80

Notes: 1. When the Icon display function using, the system should be initialized by the software initialization because of the MK RAM does not initialize except the software initialization
2. In the table 4, the bits D_5 to D_7 mentioned by * are invalid.

(1-8) Timing Generator

The timing generator generates a timing signals for the DD RAM, MK RAM, CG RAM, CG ROM and other internal circuit operation. RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.
Therefore, when the data write to the DD RAM for example, there will be undesirable Influence, such as flickering, in areas other than the display area.

(1-9) LCD Driver

LCD driver consists of 18-common driver and 80-segment driver.
80 bits of character pattern data are shifted in the shift-register and latched when the 80 bits shift performed completely. This latched data controls display driver to output LCD driving waveform.

(1-10) Cursor Blinking Control Circuit

This circuits controls cursor On/Off and cursor position character blinks. The cursor or blinks appears in the digit position at the DD RAM address set in the address counter(AC).
When the address counter is $(04)_H$, a cursor position is shown as follows:

	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
AC	0	0	0	0	1	0	0

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
2nd line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	(Hexadecimal)

Cursor Position

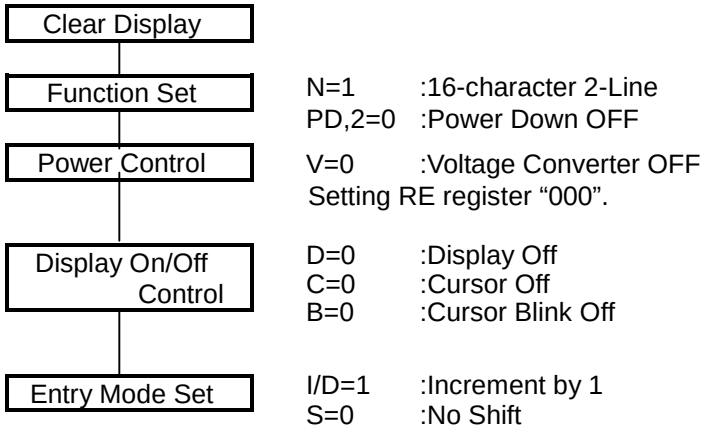
Note) The cursor or blinks appears when the address counter (AC) selects the CG RAM.
But the displayed cursor and blink are meaningless.
If the AC stores the CG RAM address data, the cursor and blink are displayed in the meaningless position.

(2) Power on Initialization by internal circuits

(2-1) Initialization By internal Reset circuits

The **NJU6636** is initialized automatically by the internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed.

During the internal power on initialization, the busy flag (BF) is "1" and this status is kept 10ms after V_{DD} = 2.4V. Initialization flow is shown below:

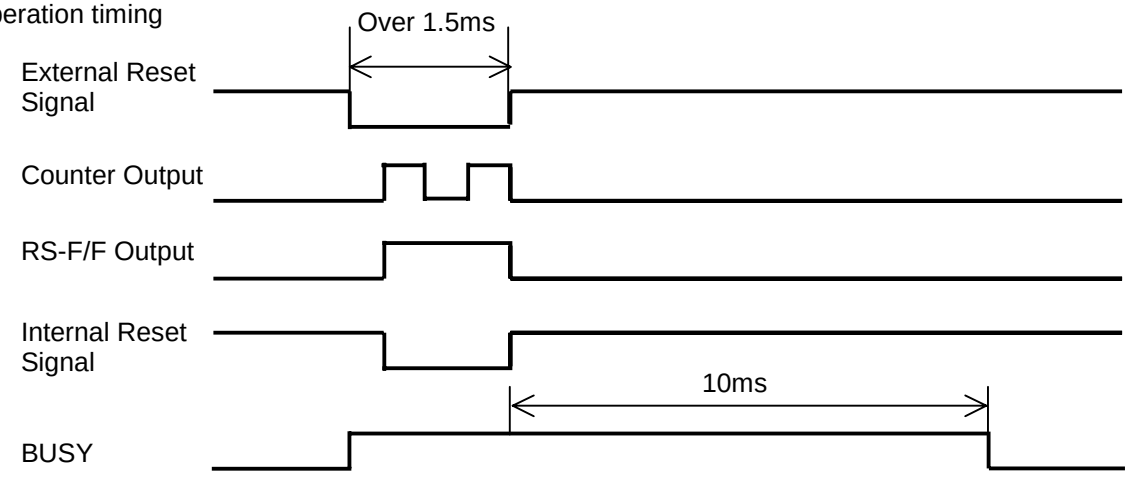


Note) If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power on initialization Circuits will not operate and initialization will not be performed.
In this case, the initialization by MPU software is required.

(2-2) Initialization By Hardware

The **NJU6636** incorporates RESET terminal to initialize the all system. When the "L" level input over than 1.5ms to the RESET terminal, the reset sequence is executed. In this time, the busy signal output during 10ms after RESET terminal goes to "H".

• Operation timing



(3) Instructions

The **NJU6636** incorporates two resisters, which are Instruction Register (IR) and a Data Register (DR).
These two registers store control information temporarily to allow interface between **NJU6636** and MPU or peripheral ICs operating different cycles. The operation of **NJU6636** is determined by this control signal from MPU. The control information includes register selection signals (RS), read/write signals (R/W) and data bus signals (DB_0 to DB_7).
Table 5. Shows each instruction and its operating time.

Table 5. Table of Instruction

INSTRUCTION	CODE										DESCRIPTION	EXEC TIME (f_{OSC}=110kHz)
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Maker Test	0	0	0	0	0	0	0	0	0	0	All “0” code is using for maker testing.	–
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets DD RAM address 0 in AC.	1500µs
Return Home / Font Size Set	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 In AC and returns display being shifted to original position. DD RAM contents remain unchanged.	91µs
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and species shift of display are performed In data read/write. I/D=1:Increment, I/D=D:Decrement,S=1:Accopa nies display shift.	91µs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B)	91µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Move cursor and shifts display without changing DD RAM contents. S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to right R/L=0 : Shift to the left	136.4µs
Function Set	0	0	0	0	1	1	N	0	PD_2	PD	Sets number of display lines (N) and power down mode (PD_2, PD). N=0 : 16-Character 1-Line N=1 : 16-Character 2-Line PD_2=0 : Power down 2 OFF PD_2=1 : Power down 2 ON PD=0 : Power down OFF PD=1 : Power down ON	91µs
Power Control	0	0	0	1	0	V	0	RE			Sets Voltage Doubler ON/OFF. (V), sets data to Voltage regulator.	91µs*1
Set RAM Address	0	0	1	RAM address							Sets RAM address. After this instruction, the data is transferred to / from RAM.	91µs
Read Busy Flag & Address	0	1	BF	AC							Read busy flag and AC contents (Note2) BF=1 : Internally operating BF=0 : Can accept instruction	0µs
Write Data to CG, MK or DD or MK RAM	1	0	Write Data(DD RAM)								Writes data into CG, MK or DD RAM.	91µs
			*	*	*	(CG, MK RAM)						
Read Data from CG, MK or DD RAM	1	1	Read Data(DD RAM)								Reads data from CG, MK or DD RAM (Note2)	136.4µs
			*	*	*	(CG, MK RAM)						
Explanation of Abbreviation	DD RAM : Display data RAM, CG RAM : Character generator RAM ACG : CG RAM address, ADD : DD RAM address, Corresponds to cursor address AC : Address counter used for both DD and CG RAM											

*=Don’t Care

Note1: f_{OSC}=110kHz when the f_{OSC} changes, the execute time also changes.
Execution time of the Power control instruction is the internal that from the instruction executed by internal circuit to the instruction sent to the power supply circuit. In actual application the power supply system need longer time to stabilize.

Note2: Using Parallel Interface only.

(3-1) Description of instruction

(a) Maker Test

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	0

All “0” code in 8-bit length is usable for NOP (Not Operating instruction).

(b) Clear Display

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code “1” is written into DB_0.
In case of normal display mode, when this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address 0 is set into the address counter and entry mode is set an increment. If the cursor or blink are displayed, they are returned to the left end of the LCD.
The S of entry mode and CG RAM data does not change.
In case of double height mode, when this instruction is executed, the space code $(20)_H$ is written into DD RAM address,$(00)_H$ to $(0F)_H$.

Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

(c) Return Home / Font Size Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	1	*

Return home instruction is executed when the code “1” is written Into DB_1. When this Instruction is executed, the DD RAM address 0 is set to address counter. Display is returned to the original position if shifted, the cursor or blink is returned to the left end of the LCD. If the cursor or blink are on the display, the DD RAM contents are not changed.

(d) Entry Mode Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets cursor moving direction and display shift On/Off, is executed when the code “1” is written into DB_2 and the codes of (I/D) and (S) are written into DB_1 (I/D) and DB_0 (S) as shown below.
(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	FUNCTION
0	Address increment : The address of the DD RAM increment (+1) when the read/write, and the cursor or blink moves to the right.
1	Address decrement : The address of the DD or CG RAM decrement (-1) when the read/write, and the cursor or blink move to the left.

S	FUNCTION
1	Entire display shift. The shift direction is determined by I/D: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated with only the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shifting

(e) Display ON/OFF Control

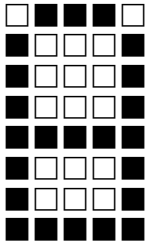
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display On/Off control instruction which controls the display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into DB_3 and the codes of (D), (C) and (B) are written into DB_2(D), DB_1(C) and DB0(B) as shown below.

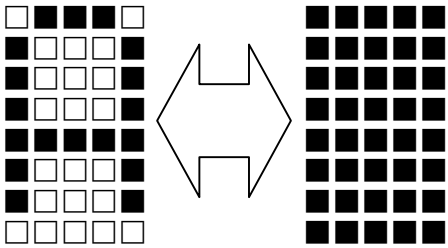
D	FUNCTION
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

C	FUNCTION
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

B	FUNCTION
1	The cursor position character is blinking. Blinking rate is 395.6ms (2-line) and 418.9ms (1-line) at f_{OSC}=110kHz. The blink is displayed alternatively with all on (it means all black) and characters display. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Character Font 5 x 7dots
(1) Cursor display example



Alternating display
(2) Blink display example

The cursor or blinks also appear when the address counter (AC) selects the CG RAM.
But the displayed cursor and blink are meaningless.
If the AC storing the CG RAM address data, the cursor and blink are displayed in the meaningless position.

(f) Cursor Display Shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

*=Don't Care

The Cursor/Display shift instruction shifts the cursor position or display the right or left without writing reading display data.
The contents of address counter (AC) is not changed by operation of display shift only.
This instruction is executed when the code "1" is written into DB_4 and the codes of (S/C) and (R/L) are written into DB_3 (S/C) and DB_2(R/L) as shown below.

S/C	R/L	FUNCTION
0	0	Shifts the cursor position to the left ((AC) is decrement by 1)
0	1	Shifts the cursor position to the right ((AC) is incremented by 1)
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	Shifts the entire display to the right and the cursor follows it.

(g) Function Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	1	1	N	0	PD_2	PD

*=Don't Care

Function set instruction which sets the number of display lines and power down mode, is executed when the code "1" is written into DB_5, DB_4 and the codes of (N), (PD_2) and (PD) are written into DB_3 (N), DB_1 (PD_2), and DB_0 (PD) as shown below (character font is fixed 5 x 8 dots).

Note) This function set instruction must be performed at the head of the program prior to all other instructions (except Busy flag/Address read).

N	FUNCTION
0	Set the 16-Character 1-Line Display
1	Set the 16-Character 2-Line Display

PD_2	FUNCTION
0	Normal operation
1	Power down mode on (The display goes to off automatically)

PD	FUNCTION
0	Normal operation
1	Power down mode on (The display goes to off automatically)

(h) Set Power Control

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	1	0	V	0	C_2	C_1	C_0
			← Higher order bit →				← Lower order bit →			

Power Control instruction which sets the Voltage Doubler, Oscillator ON/OFF and sets data to Voltage Regulator, is executed when the code "1" is written into DB_6 and the codes of (V) and (C_2 to C_0) are written into DB_4 (V) and DB_2 to DB_0 (C_2 to C_0), as shown below.

V	FUNCTION
0	Voltage Converter stop the operation
1	Voltage Converter starts the operation

C_2	C_1	C_0	V_{REG}(V)
0	0	0	Min.
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	Max.

(i) Set RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	A	A	A	A	A	A	A
			← Higher order bit →				← Lower order bit →			

Set CG RAM address instruction is executed when the code "1" is written into DB_7 and the address is written into DB_6 to DB_0 as shown above.
The address data (DB_6 to DB_0) is written into the address counter (AC) by this instruction. Affter this instruction execution, the data writing / reading is performed into / from the address RAM.
The RAM includes DD RAM, CG RAM and MK RAM are shared by address as shown below.

		CG RAM address
DD RAM	1^{st} Line :	from $(00)_H$ to $(0F)_H$
DD RAM	2^{nd} Line :	from $(10)_H$ to $(1F)_H$
MK RAM	80icon :	from $(20)_H$ to $(2F)_H$
CG RAM	8character :	from $(40)_H$ to $(7F)_H$

(j) Read Busy Flag & Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A	A	A	A	A	A	A
			← Higher order bit →				← Lower order bit →			

This instruction reads out the internal status of the **NJU6636**. When this instruction is executed, the busy flag (BF) which indicates the internal operation, is read out from DB_7 and the address of CG RAM, MK RAM or DD RAM is read out from DB_6 to DB_0 (an address for CG RAM, MK RAM or DD RAM is determined by the previous instruction). Using parallel Interface only.
(BF)=1 indicates that internal operation is in progress. The next instruction is inhibited when (BF)=1. Check the (BF) status before the next write operation.

(k) Write Data to RAM

Write data to DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	D	D	D	D	D	D	D	D
			← Higher order bit →				← Lower order bit →			

Write data to CG RAM, MK RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	1	0	*	*	*	D	D	D	D	D	∗=Don't Care
			← Higher order bit →				← Lower order bit →				

Write Data to CG RAM, MK RAM or DD RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).
By the execution of this instruction, the binary 5-bit data "DDDDD" are written into the CG RAM or MK RAM, and the binary 8-bit data "DDDDDDDD" are written into the DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction.
After this instruction execution, the address increment(+1) or decrement(-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

(l) Read Data from RAM

Read data to DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	1	D	D	D	D	D	D	D	D
			← Higher order bit →				← Lower order bit →			

Read data to CG RAM

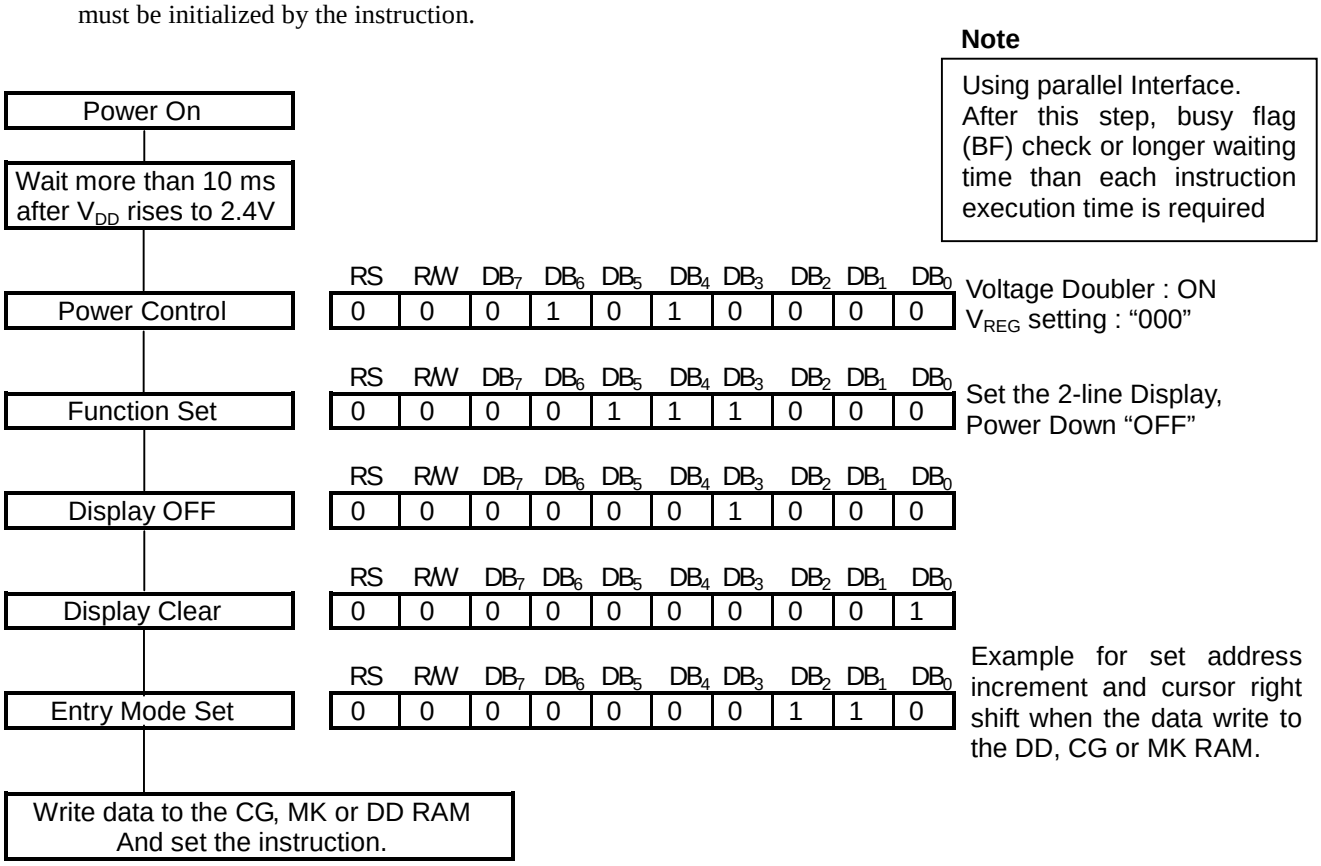
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	1	1	*	*	*	D	D	D	D	D	∗=Don't Care
			← Higher order bit →				← Lower order bit →				

Read Data to CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and (R/W).
By the execution of this instruction, the binary 5-bit data "DDDDD" are read out from CG RAM, MK RAM and the binary 8-bit data "DDDDDDDD" are read out from DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction. (Using parallel Interface)
Before executing this instruction, either the CG RAM address set or DD RAM address set must be executed, otherwise the first read out data Invalidated.
When this instruction is serially executed, the next address data is normally read from the second read.
The address set instruction is not required if the cursor shift instruction is executed just beforehand (only DD RAM reading).
The cursor shift instruction has same function as the DD RAM address set, so that after reading the DD RAM, the address increment or decrement is executed automatically according to the entry mode.
But display shift does not occur regardless of the entry mode.

Note) The address counter (AC) is automatically incremented by 1 after write instructions to either of the CG RAM, MK RAM or DD RAM. Even if the read instruction is executed after this instruction, the addressed data can not be read out correctly.
For a correct data read out, either the address set instruction or cursor shift instruction (only with DD RAM) must be implemented just before this instruction or from the second time read out instruction execution if the read out instruction is executed 2 times consecutively.

(3-2) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not method, the **NJU6636** must be initialized by the instruction.



(4) Power Down function

NJU6636 incorporates two power down mode to decrease the operating current during standby status.
The status of internal circuits at the two power down mode is shown below :

PD ="1": Voltage converter, Voltage regulator and Oscillator stops operation.
Segment and Common drivers output VSS level.
The contents of DD RAM, CG RAM and MK RAM are saved.

PD_2="1": Voltage converter and Voltage regulator stops operation.
Segment and Common drivers output VSS level.
The contents of DD RAM, CG RAM and MK RAM are saved.

Note. The other instruction one unavailable after Power Down functioned. Make sure to turn off Power Down function before executing other instructions.
Executing the Display OFF before Power Down is recommended. If Power Down is executed during Display ON, unexpected pixels may be turned on.

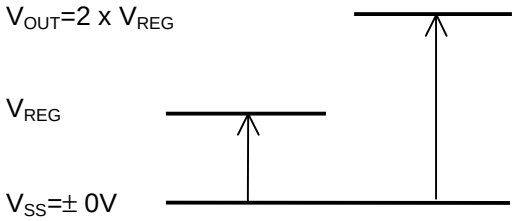
(5) LCD DISPLAY

(5-1) LCD Powr supply

NJU6636 incorporates a 2 x Voltage Converted and bleeder resistance to generate the waveform of LCD driving high voltage.

(a) Voltage converter

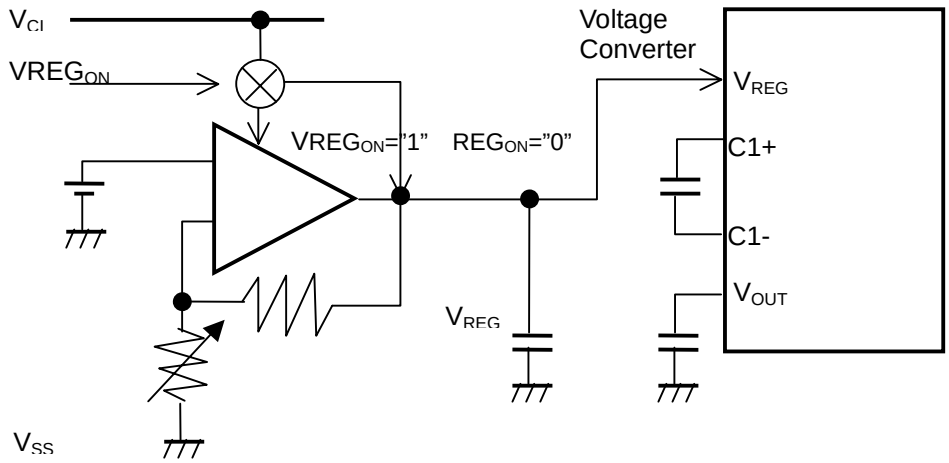
By connecting the capacitor between C_1^+ and C_1^-, V_{SS} and V_{OUT} respectively, V_{CI} or V_{REG} (set by internal voltage regulator) is 2 times boosted and output from V_{OUT}.



(b) Voltage regulator

Voltage regulator generates the reference voltage to Voltage Converter by setting the $VREG_{ON}$ terminal.

$VREG_{ON}$ = "1" :Voltage regulator ON
$VREG_{ON}$ = "0" :Voltage regulator OFF



Recommend value : C=1µF

Note) Recovery from Power Down status or just after power ON, it need 10mS for LCD Power Supply circuit to function, please set waiting time till display ON.

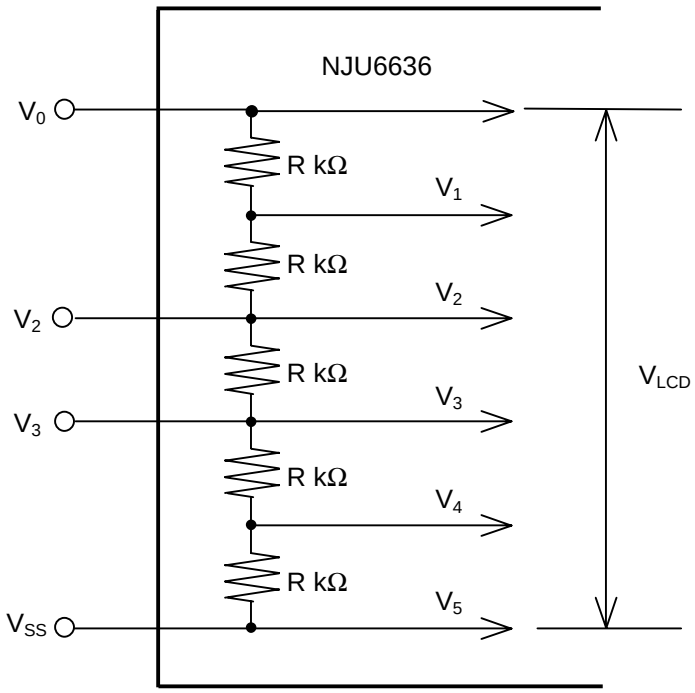
(c) Bleedr Resistance

Each LCD driving voltage (V1, V2, V3, V4) is generated by the bleedr resistance.
The bleeder resistance is set 1/5 bias suitable for 1/17 duty ration and 40kΩ(Typ.) resistance total.

LCD Driving Voltage vs. Duty Ratio

Power Supply	Duty Ratio	1/17, 1/9
	Bias	1/5
	V_2	$3/5V_0$
	V_3	$2/5V_0$
	V_{SS}	V_{SS}

The V_{LCD} is maximum swing of LCD waveform.



LCD Driving Voltage example

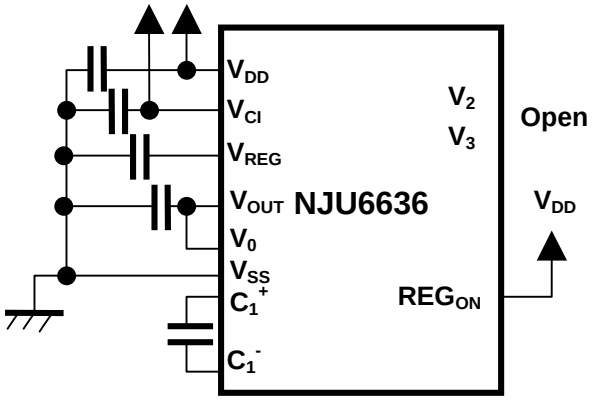
Note) Power ON or power OFF is in the following order.

1. Using the internal power Supply
   Power ON : First V_{DD}, then V_{CI} power ON, after the built-in Voltage Regulator outputting stabilized V_{REG}, turn the Voltage Converter on. After the Voltage Converter stabilized, Execute Display ON instruction
   Power OFF: First Display OFF, then stop the operation of the Voltage Converter, turn off the V_{CI} and then turn off the V_{DD}.
2. Using the external Power Supply
   Power ON : V_0 should be turned on after the V_{DD} turned on.
   Power OFF : After Display OFF, turn off the V_0 and then turn off the V_{DD}.

(d) Internal power supply operation (1/5 Bias)

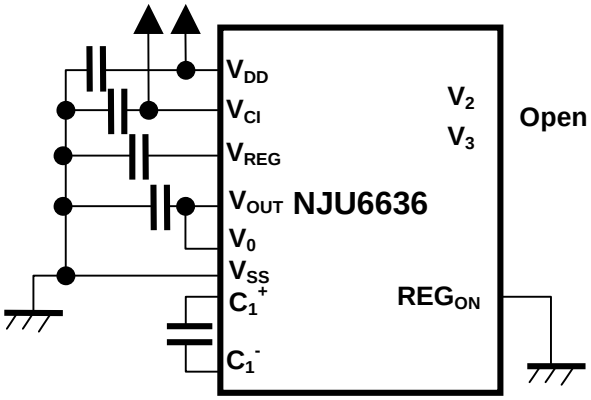
Voltage Converter, Voltage Reglator Using

$V_{CI}=V_{DD}=3V$



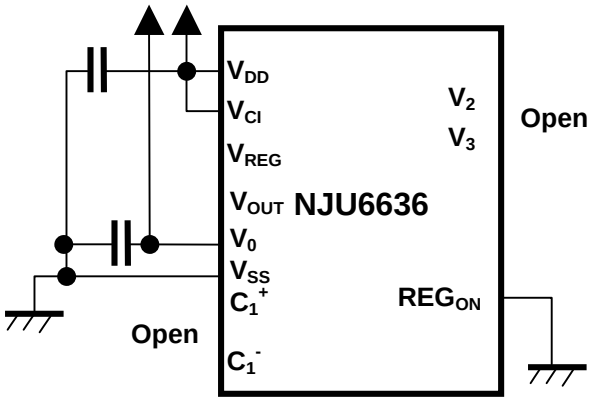
Voltage Converter Using

$V_{CI}=V_{DD}=3V$



(e) External power supply operation (1/5 Bias)

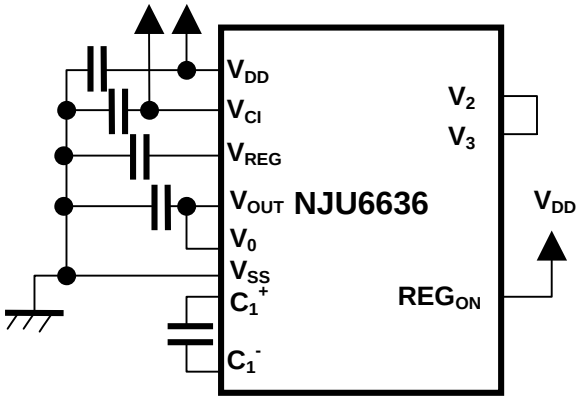
$V_0=5V$ $V_{DD}=3V$



(f) Internal power supply operation (1/4 Bias)

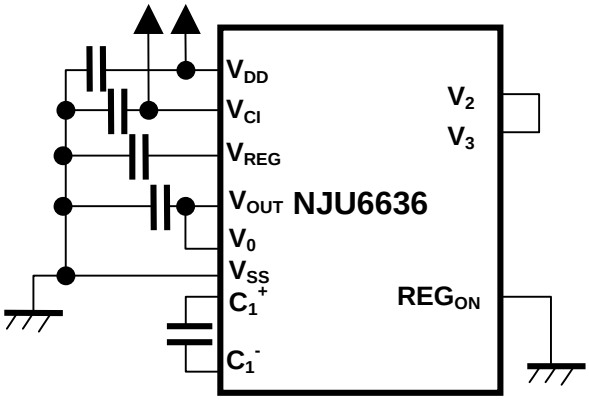
Voltage Converter, Voltage Reglator Using

$V_{CI}=V_{DD}=3V$



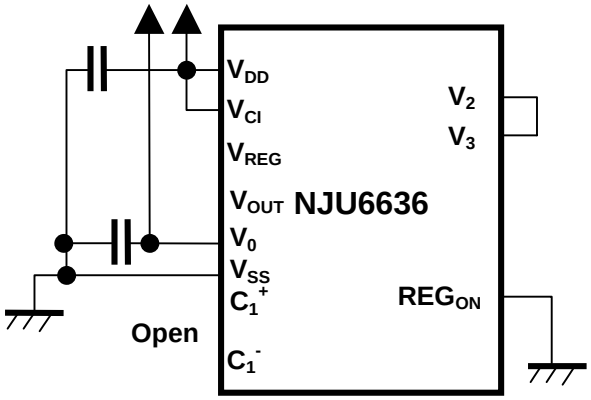
Voltage Converter Using

$V_{CI}=V_{DD}=3V$



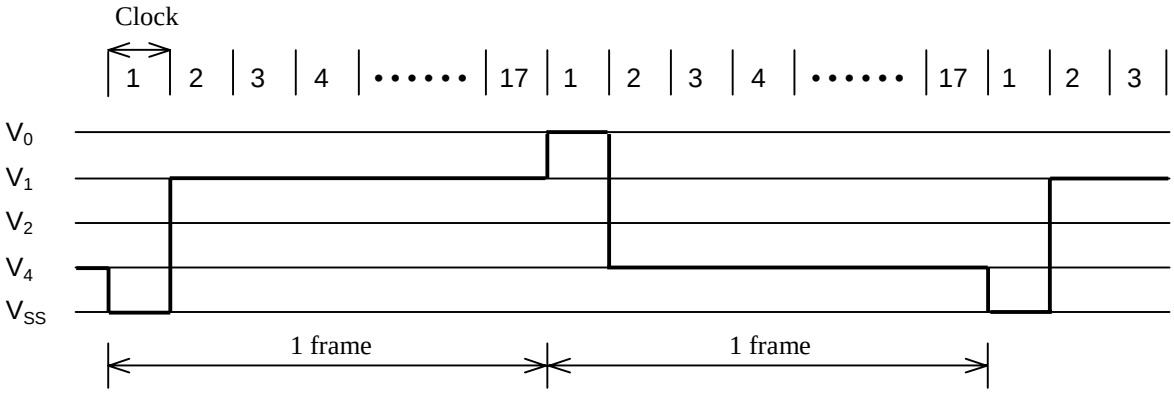
(g) External power supply operation (1/4 Bias)

$V_0=5V$ $V_{DD}=3V$



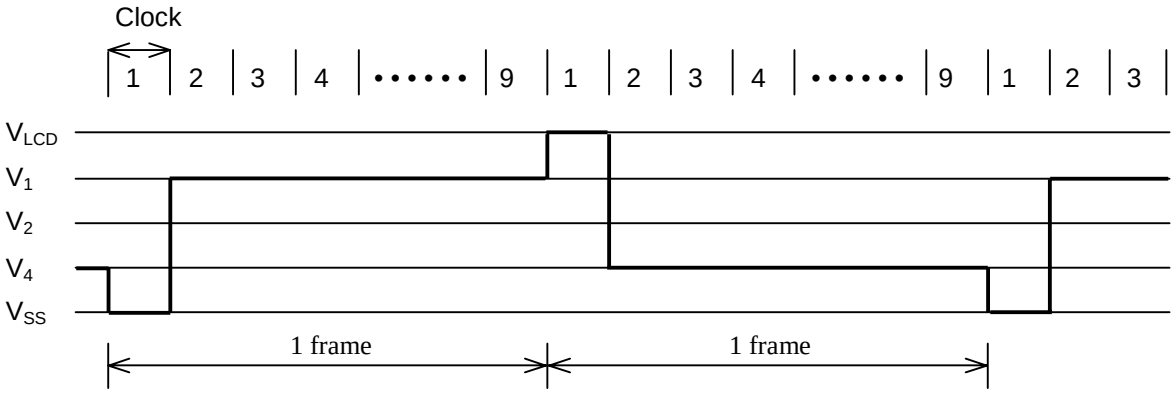
(6) Relation between oscillation frequency and LCD frame frequency.
LCD frame frequency example mentioned below is based on 110kHz oscillation. (1 clock = 9.091μs)

- 1/17 duty



1 frame = 9.091(μs) x 80 x 17 = 12.36(ms)
Frame frequency = 1/12.36(ms) = 80.88(Hz)

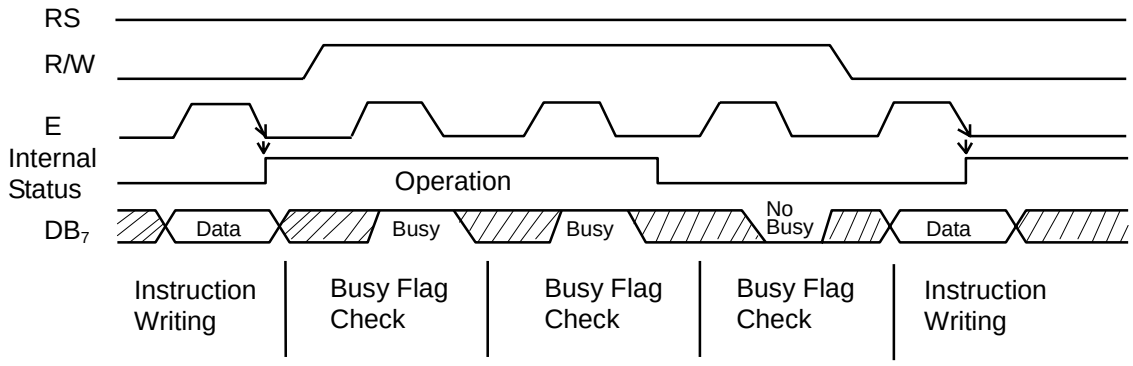
- 1/9 Duty



1 frame = 9.091(μs) x 80 x 9 = 6.55(ms)
Frame frequency = 1/6.55(ms) = 152.78(Hz)

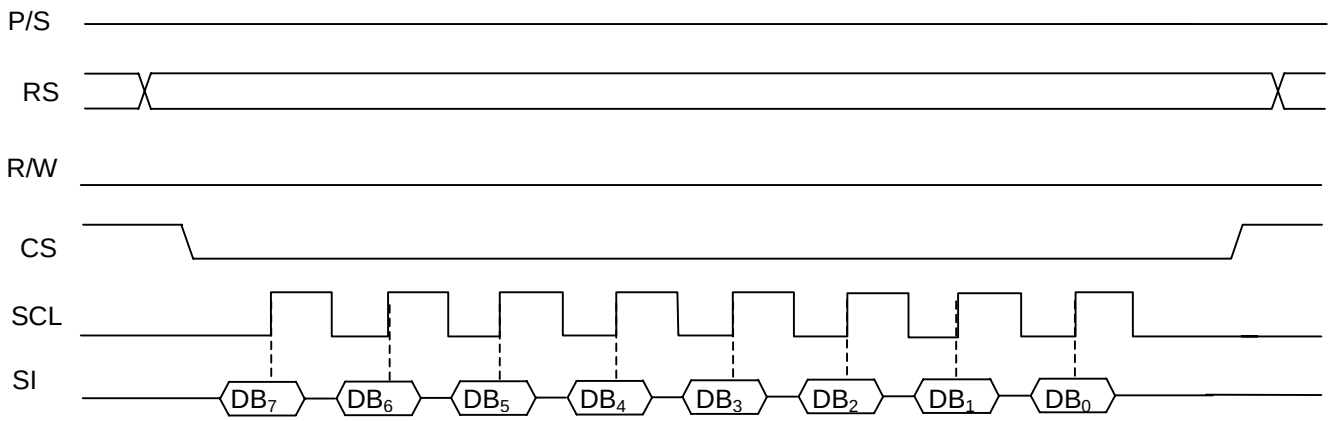
(7) Interface with MPU
Interface circuits of **NJU6636** can be connected to serial or 8-bit parallel.

(7-1) 8-bit MPU interface



(7-2) Serial Interface with MPU

Serial interface circuit is activated when the P/S terminal is set to "L" level (V_{SS}) then the chip select terminal(CS) goes to "L" level. The data input is MSB first like as the order of DB_7, DB_6 to DB_0. The input data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The shift register converted to parallel data at the CS rise edge input. In case of entering over than 8-bit data, valid data is last 8-bit data. The output data is exited from the shift register synchronized at the fall edge of the serial clock SCL. The time chart for the serial interface is shown below. Furthermore, in serial interface mode, only data writing is available. And at the same time, R/W pin shall be fixed at V_{SS}.



Note : The level ("L" or "H") of RS terminal should be set before CS terminal goes to "L" level.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Operating Temperature	T_{opr}	-40 to +85	°C
Storage Temperature	T_{stg}	-55 to +125	°C

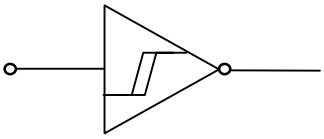
Note 1.) If the LSI is used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.
Note 2.) Decoupling capacitor should be connected between V_{DD}, $V_{ci,}$, V_0 and $V_{SS.}$
Note 3.) All voltage values are specified as V_{SS} =0V
Note 4.) The relation $V_{DD}>V_{SS}$, Vci>V_{SS} V_{SS}=0V must be maintained. V_0 should be turned on after the V_{DD} turned on.

■ ELECTRICAL CHARACTERISTICS (Applies to NJU6636A) (VDD=2.4 to 5.5V, VSS=0V, Ta=-40 to 85°C)

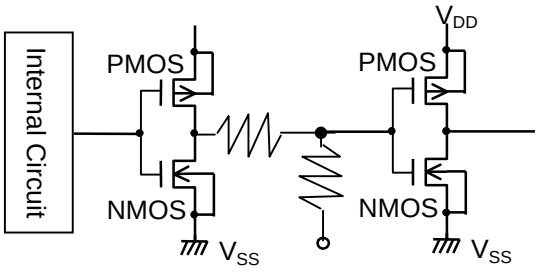
PARAMETER	SYMBOL	SYMBOL		MIN	TYP	MAX	UNIT	NOTE
Operating Volt.	V_{DD}	V_{DD}		2.4	-	5.5	V	
Input Voltage 1	V_{IH1}			$0.8V_{DD}$	-	V_{DD}	V	5
	V_{IL1}			-	–	$0.2V_{DD}$	V	
Output Voltage	I_{OH}	$-I_{OH}$=0.205mA		2	–	–	V	6
	I_{OL}	I_{OL}=1.6mA, V_{DD}=3V		–	–	0.5	V	
Driver On-resist. (COM/SEG)	R_{COM}	$\pm I_d$=1µA , V_0=3/6V (All com. Term.)		–	–	20	kΩ	7
	R_{SEG}	$\pm I_d$=1µA , V_0=3/6V (All Seg. Term.)		–	–	30	kΩ	
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{DD}		-1	–	1	µA	7
Pull-up Resist Current	$-I_P$	V_{DD}=3V, V_{IN}=0V (ALL DB Term.)		–	11	50	µA	9
Operating Current	I_{DD}	V_{DD}=3V, Display ON f_{OSC}=110kHz (CR Oscillation) Internal Regulator ON : "000" V_{IN}=0V or 3V Ta=25°C		–	60	200	µA	10
	I_{CI}			–	240		µA	
	I_{REG}			–	4	30	µA	
	I_O			–	125	400	µA	
	I_{STB1}	V_{DD}=V_{CI}=3V, PD=1, Ta=25°C		–	3	10	µA	
	I_{STB2}	V_{DD}=V_{CI}=3V, PD_2=1, Ta=25°C		–	25	100	µA	
LCD Driving Voltage	V_{LCD}	V_0 Terminal, V_{DD}=3V		3.0	–	6.0	V	
Bleeder Resist.	R_B	V_{DD}-VSS=5V, RB=(V0-VS)/IB, Ta=25°C		34	40	46	kΩ	
Oscillation Freq.	f_{OSC}	V_{DD}=3V, Ta=25°C		90	110	130	kHz	
Ext. CLK Freq.	f_{CP}	OSC_1 Terminal		90	110	130	kHz	
Ext. CLK Duty	Duty	OSC_1 Terminal		45	50	55	%	
Int. Regulator Output Volt.	V_{REG}	VCI=5V, Ta=25°C	REG : (000)	2.134	2.2	2.266	V	11
			REG : (001)	2.231	2.3	2.369		
			REG : (010)	2.328	2.4	2.472		
			REG : (011)	2.425	2.5	2.575		
			REG : (100)	2.522	2.6	2.678		
			REG : (101)	2.619	2.7	2.781		
			REG : (110)	2.716	2.8	2.884		
			REG : (111)	2.813	2.9	2.987		
Int. Regulator V_{IN}-V_{OUT}	V_{IO}	I_{OUT}=1mA, Ta=25°C		–	0.2	0.6	V	11
Int. Regulator Input Volt.	V_{CI}	Regulator Using		3.5	–	6	V	11
Int. Regulator Lord Reg.	V_{REG}	V_{CI}=5V, I_{OUT}=1-5mA, Ta=25°C		–	–	200	mV	11
Output Voltage	V_{OUT}	V_{CI}=3V, REG_{ON}, Ta=25°C		5.4	5.8	–	V	12

- Input / Output structure except LCD driver are shown below:
- Input Terminal Structure

E, RESb Terminals

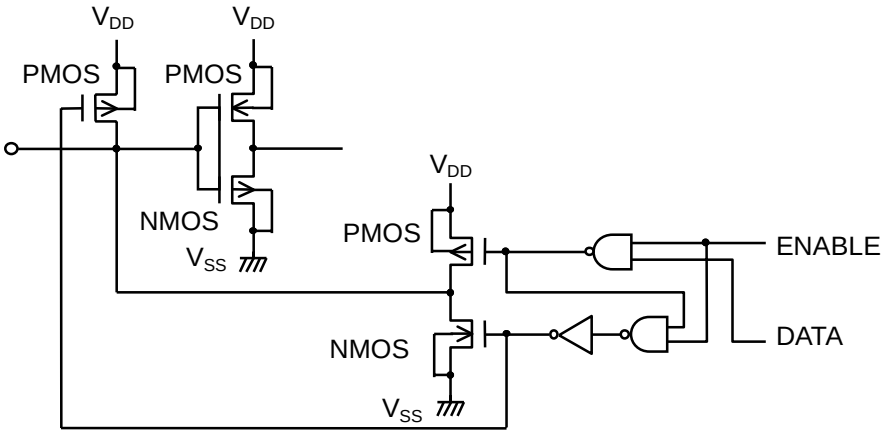


OSC_1Terminal



- Input / Output Terminal Structure

DB_0 to DB_7 Terminals



Note 5.) OSC_1, P/S, RS, R/W, E, SCL, DB_7 to DB_0, SEL_1, SEL_2, REG_{ON}, RESb

Note 6.) DB_7 (CS) , DB_6 (SIO), DB_5 to DB_0.

Note 7.) R_{COM} and R_{SEG} are the resistance values between power supply terminals (V_0, V_2, V_3, V_{ss}) and each common terminal (COM_1 to COM_{16}), and supply voltage (V_0, V_2, V_3, V_{ss}) and each segment terminal (SEG_1 to SEG_{80}) respectively, and measured when the current Id is flown on every common and segment terminals at the same time.

Note 8.) P/S, RS, R/W, E, SCL, SEL_1, SEL_2, REG_{ON}, RESb.

Note 9.) DB_7(CS), DB_6(SIO), DB_5 to DB_0.

Note 10.) I_{DD} : Applies to the V_{DD}.
- V_{OUT} and V_0 are connected, Voltage Converter ON

I_{CI} : Applies to the V_{CI}.
- V_{OUT} and V_0 are connected, Voltage Converter ON

I_{REG}: Applies to the V_{CI}.
- V_{OUT} is open, V_0=5V, Voltage Converter OFF

I_0: Applies to the V_0.
- V_{OUT} is open, V_0=5V, voltage Converter OFF

I_{STB1}: Applies to the V_{DD} and V_{CI}.
- V_{OUT} and V_0 are connected.

I_{STB2}: Applies to the V_{DD} and V_{CI} .
- V_{OUT} and V_0 are connected.

Use 1µF capacitor connecting V_{REG} - V_{SS}, C_1^- - C_1^+, V_{OUT} - V_{SS}, and evaluate via V_{REG}.

Note 11.) V_{REG}
- Use 1µF capacitor connecting V_{CI} - V_{SS}, V_{REG} - V_{SS}, and evaluate via V_{REG}.

Note 12.) V_{OUT}
- Connect V_{OUT} and V_0, and use 1µF capacitor connecting V_{REG} - V_{SS}, C_1^- - C_1^+ and V_{OUT} - V_{SS}.

■ Bus timing characteristics (V_{DD}=2.4 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C)

• Write operation sequence (write from MPU to **NJU6636**)

PARAMETER		SYMBOL	MIN	MAX	UNIT	CONDITION
Enable Cycle Time		t_{CYCE}	1000	–	ns	Fig.1
Enable Pulse Width	"High" level	PW_{EH}	400	–		
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}	–	20		
Set up Time	RS, R/W-E	t_{AS}	200	–		
Address Hold Time		t_{AH}	200	–		
Data Set up Time		t_{DSW}	200	–		
Data Hold Time		t_H	200	–		

Lord Condition of DB_0 to DB_7 : CL=100pF

Timing Characteristics (Write Operation)

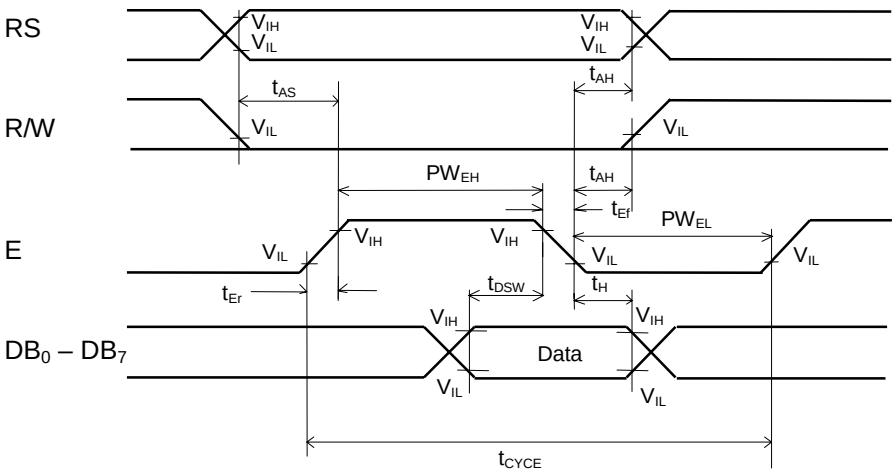


Fig.1

• Read operation sequence (Read from **NJU6636** to MPU)

PARAMETER		SYMBOL	MIN	MAX	UNIT	CONDITION
Enable Cycle Time		t_{CYCE}	1000	–	ns	Fig.2
Enable Pulse Time	"High" level	PW_{EH}	600	–		
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}	–	20		
Set up Time	RS, R/W-E	t_{AS}	200	–		
Address Hold Time		t_{AH}	200	–		
Data Delay Time		t_{DDR}	–	600		
Data Hold Time		t_{DHR}	0	–		

Lord Condition of DB_0 to DB_7 : CL=100pF

Timing Characteristics (Read Operation)

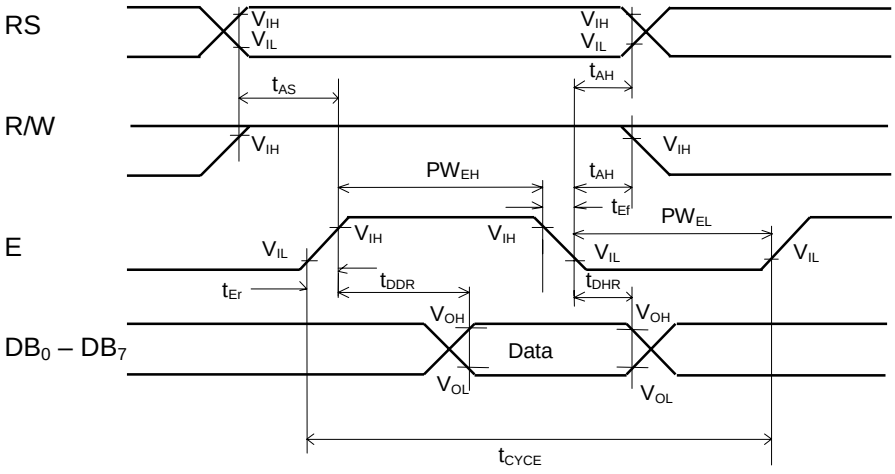


Fig. 2

■ Bus timing characteristics (V_{DD}=2.4 to 5.5V, V_{SS}=0V, Ta=-40 to 85°C)

• Serial Interface sequence

PARAMETER		SYMBOL	MIN	MAX	UNIT	CONDITION
Serial Clock Cycle Time		t_{CYCE}	1000	–	ns	Fig.3
Serial Clock Width	"High" level	t_{SCH}	300	–		
	"Low" level	t_{SCL}	700	–		
Serial Clock Rise Time, Fall Time		t_{SCR}, t_{SCF}	–	20		
Chip Select Pulse width		P_{WCS}				
Chip Select Set Up Time		t_{CSU}				
Chip Select Hold Time		t_{CH}				
Chip Select Rise Time, Fall Time		t_{CSR},t_{CSF}				
Set up Time	RS-E	t_{AS}	200	–		
Address Hold Time		t_{AH}	200	–		
Serial Input Data Set up Time		t_{DSISU}	200	–		
Serial Input Data Hold Time		t_{SIH}	200	–		

Serial Interface

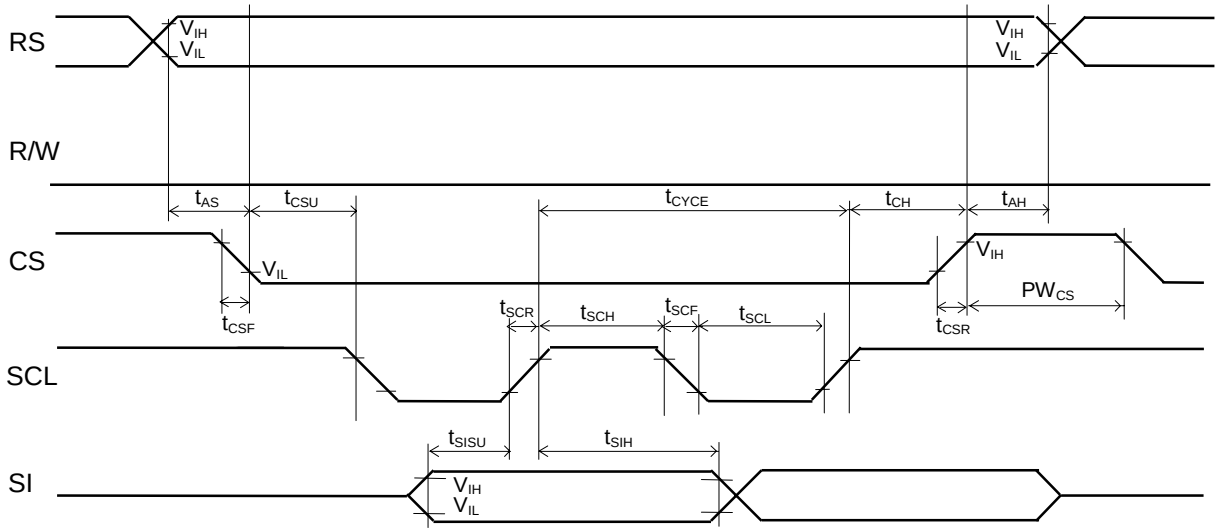
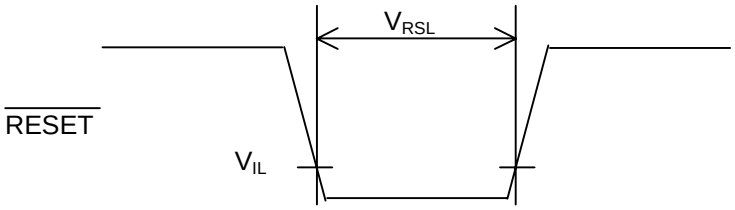


Fig. 3

• The Input Condition when using the Hardware Reset Circuit (Ta=-40 to 85°C)

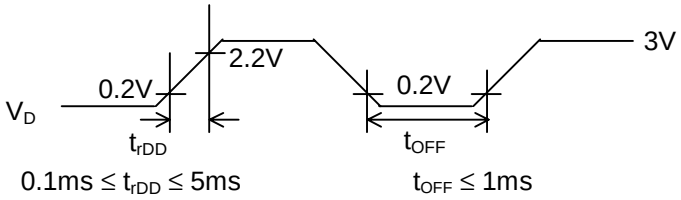
P A R A M E T E R	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
RESET input "Low" level width	t_{RSL}	f_{OSC} =110kHz	1.5	–	–	ms

Input timing



• Power supply condition when using the internal initialization circuit (Ta=-40 to 85°C)

P A R A M E T E R	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Power supply rise time	t_{rDD}	–	0.1	–	5	ms
Power supply OFF time	t_{OFF}	–	1	–	–	ms



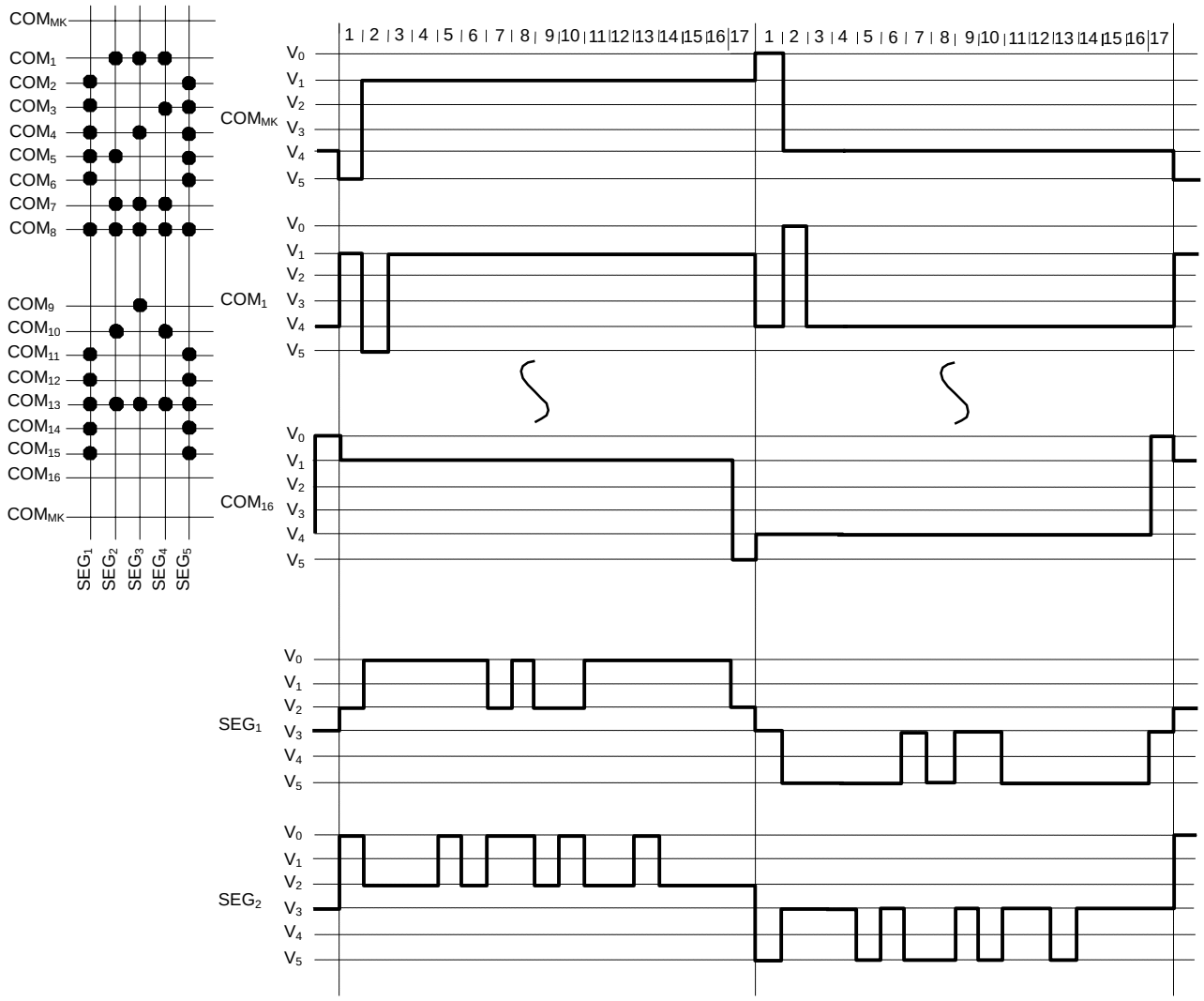
0.1ms ≤ t_{rDD} ≤ 5ms t_{OFF} ≤ 1ms

*t_{OFF} specifies the power OFF time in a short period OFF or cyclical ON/OFF

Note.) Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction(Refer to initialization by the instruction).

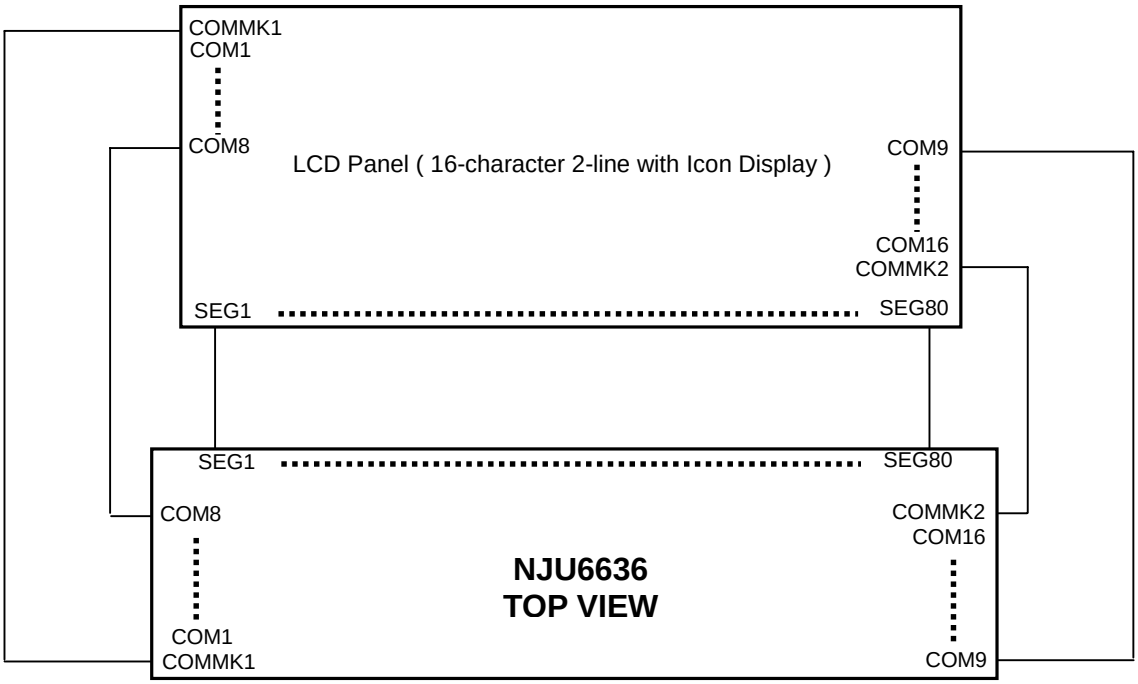
■ LCD DRIVING WAVE FROM

NJU6636 1/17 Duty driving

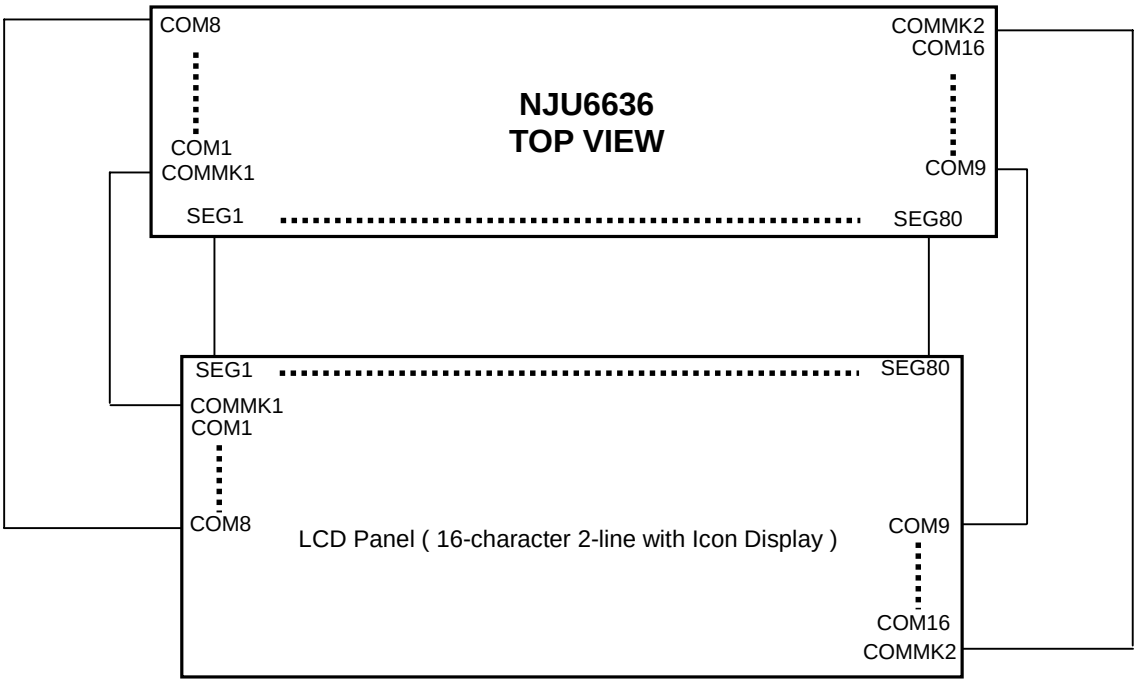


■ APPLICATION CIRCUITS

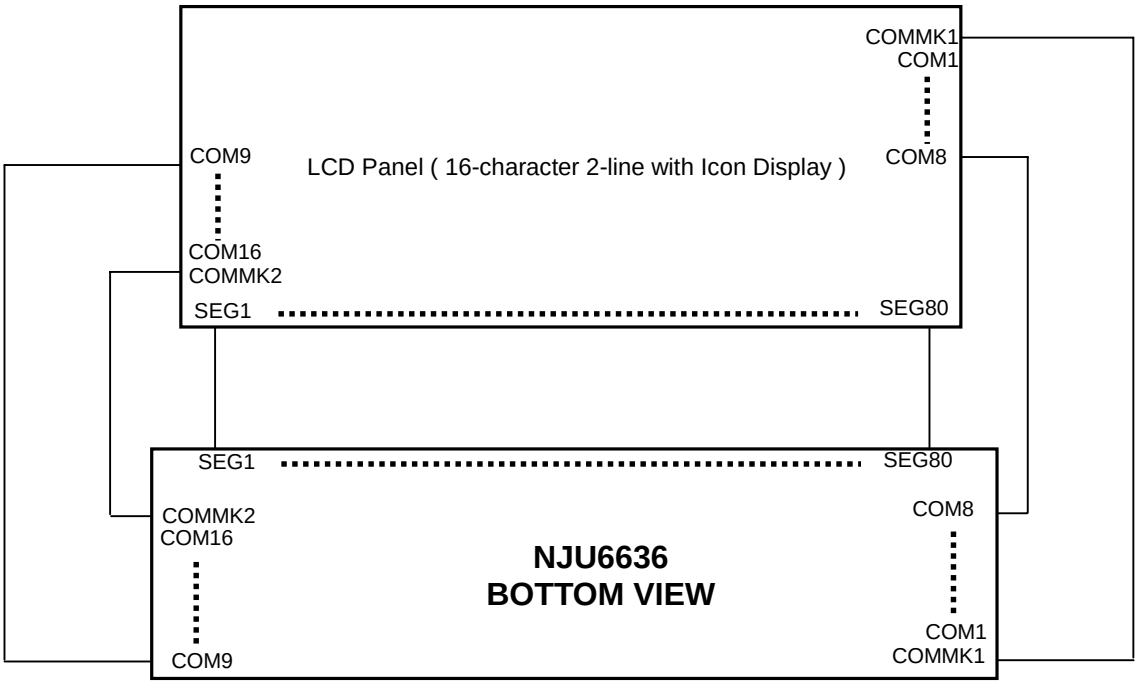
SEL1=0, SEL2=0



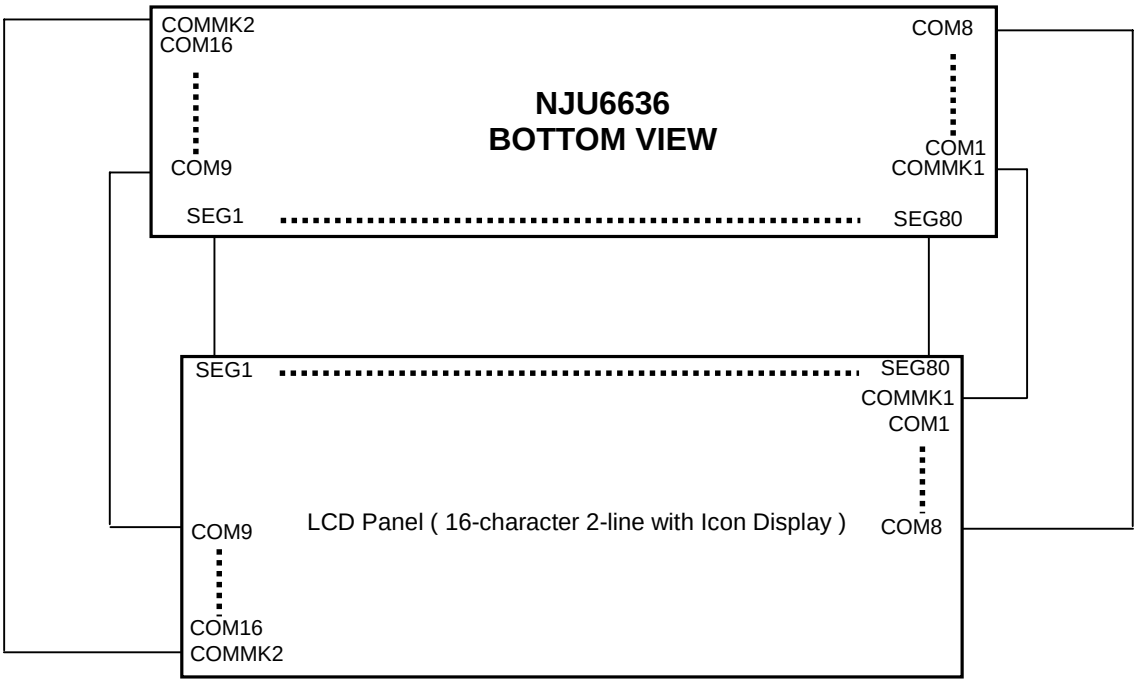
SEL1=1, SEL2=1



SEL1=0, SEL2=1



SEL1=1, SEL2=0



MEMO

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