MX29F100T/B

1M-BIT [128Kx8/64Kx16] CMOS FLASH MEMORY

FEATURES

- 5V±10% for read, erase and write operation
- 131072x8/ 65536x16 switchable
- Fast access time:55/70/90/120ns
- Low power consumption
  - 30mA maximum active current
  - 1uA typical standby current
- Command register architecture
  - Byte/ Word Programming (7us/ 14us typical)
  - Erase (16K-Bytex1, 8K-Bytex2, 32K-Bytex1, and 64K-Byte x1)
- Auto Erase (chip) and Auto Program
  - Automatically erase any combination of sectors or with Erase Suspend capability.
  - Automatically program and verify data at specified address
- Status Reply
  - Data polling & Toggle bit for detection of program and erase cycle completion.
- Compatibility with JEDEC standard
  - Pinout and software compatible with single-power supply Flash
  - Superior inadvertent write protection
- Sector protection
  - Hardware method to disable any combination of sectors from program or erase operations
  - Sector protect/unprotect for 5V only system or 5V/ 12V system
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1 to VCC+1V
- Boot Code Sector Architecture
  - T = Top Boot Sector
  - B = Bottom Boot Sector
- Low VCC write inhibit is equal to or less than 3.2V
- Package type:
  - 44-pin SOP
  - 48-pin TSOP
- Ready/Busy pin(RY/$\overline{BY}$)
  - Provides a hardware method or detecting program or erase cycle completion
- Erase suspend/ Erase Resume
  - Suspend an erase operation to read data from, or program data to a sector that is not being erased, then resume the erase operation.
- Hardware $\overline{RESET}$ pin
  - Hardware method of resetting the device to reading the device to reading array data.

GENERAL DESCRIPTION

The MX29F100T/B is a 1-mega bit Flash memory organized as 131,072 bytes or 65,536 words. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29F100T/B is packaged in 44-pin SOP and 48-pin TSOP. It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

The standard MX29F100T/B offers access time as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29F100T/B has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

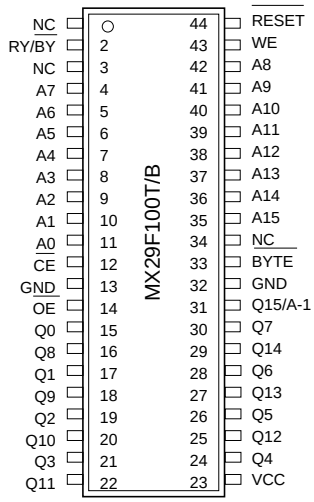
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29F100T/B uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29F100T/B uses a 5.0V±10% VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

44SOP(500mil)



48 TSOP(TYPE I) (12mm x 20mm)

(NORMAL TYPE)

(REVERSE TYPE)

PIN DESCRIPTION:

SYMBOL	PIN NAME
A0-A15	Address Input
Q0-Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr.(Byte mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{RESET}$	Hardware Reset Pin, Active low
$\overline{WE}$	Write Enable Input
RY/$\overline{BY}$	Ready/Busy Output
$\overline{BYTE}$	Word/Byte Selection Input
VCC	Power Supply Pin (+5V)
GND	Ground Pin
NC	Pin Not Connected Internally

BLOCK STRUCTURE

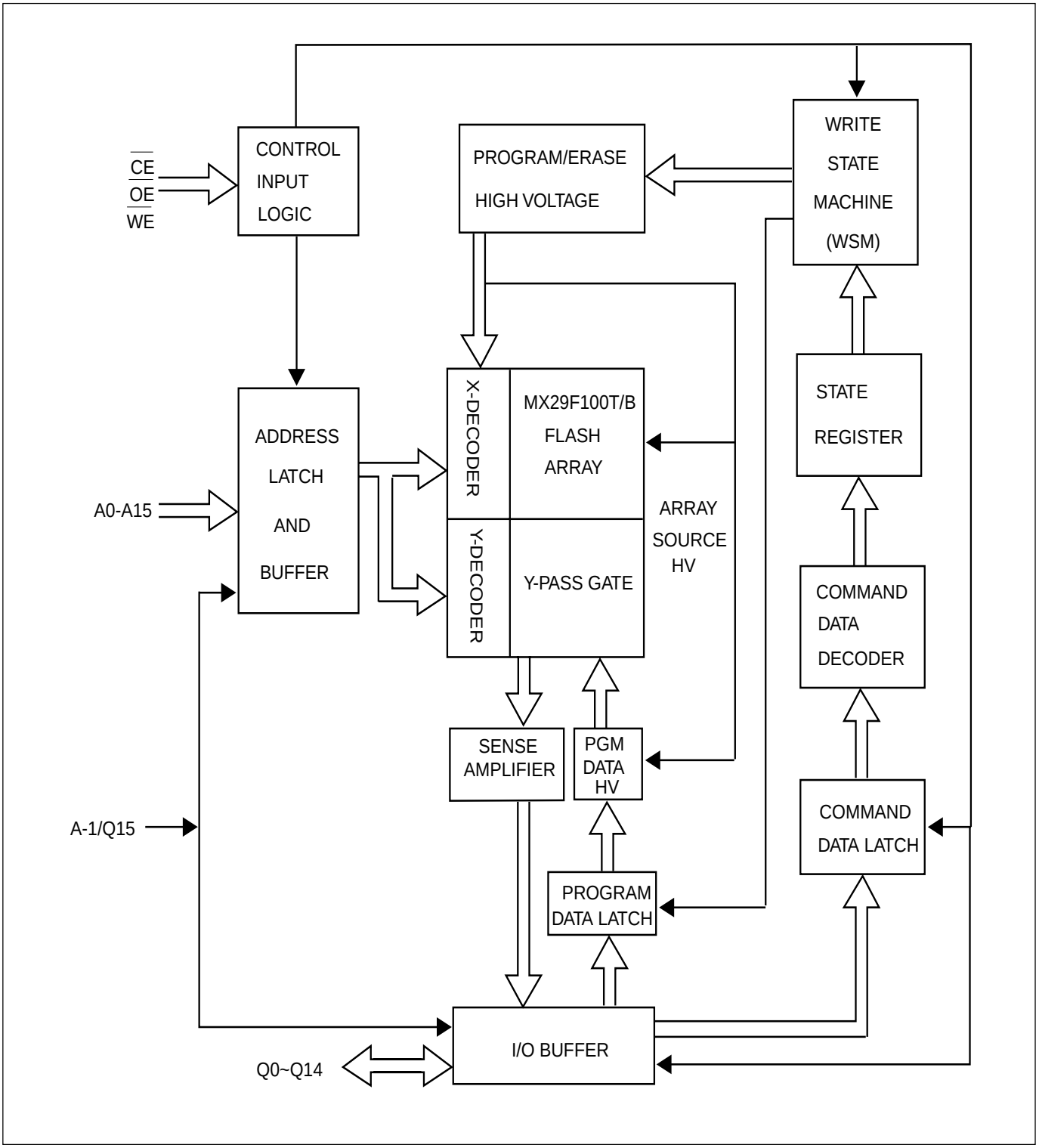
MX29F100T Top Boot Sector Addresses Tables

	A15	A14	A13	A12	(x8)Address Range		(x16) Address Range	
SA0	0	X	X	X	00000h-0FFFFh	64KB	00000h-07FFFh	32KW
SA1	1	0	X	X	10000h-17FFFh	32KB	08000h-0BFFFh	16KW
SA2	1	1	0	0	18000h-19FFFh	8KB	0C000h-0CFFFh	4KW
SA3	1	1	0	1	1A000h-1BFFFh	8KB	0D000h-0DFFFh	4KW
SA4	1	1	1	X	1C000h-1FFFFh	16KB	0E000h-0FFFFh	8KW

MX29F100B Bottom Boot Sector Addresses Tables

	A15	A14	A13	A12	(x8)Address Range		(x16) Address Range	
SA0	0	0	0	X	00000h-03FFFh	16KB	00000h-01FFFh	8KW
SA1	0	0	1	0	04000h-05FFFh	8KB	02000h-02FFFh	4KW
SA2	0	0	1	1	06000h-07FFFh	8KB	03000h-03FFFh	4KW
SA3	0	1	X	X	08000h-0FFFFh	32KB	04000h-07FFFh	16KW
SA4	1	X	X	X	10000h-1FFFFh	64KB	08000h-0FFFFh	32KW

BLOCK DIAGRAM



AUTOMATIC PROGRAMMING

The MX29F100T/B is byte/ word programmable using the Automatic Programming algorithm. The Automatic Programming algorithm does not require the system to time out sequence or verify the data programmed. The typical chip programming time of the MX29F100T/B at room temperature is less than 2 seconds.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 10 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than two second. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are internally controlled by the device.

AUTOMATIC BLOCK ERASE

The MX29F100T/B is block(s) erasable using MXIC's Auto Block Erase algorithm. Block erase modes allow blocks of the array to be erased in one erase cycle. The Automatic Block Erase algorithm automatically programs the specified block(s) prior to electrical erase. The timing and verification of electrical erase are internally controlled by the device.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm requires the user to only write program set-up commands (include 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, verifies the program and counts the number of sequences. A status bit similar to $\overline{\text{DATA}}$ polling and a status bit toggling between consecutive read cycles, provides feedback to the user as to the status of the programming operation.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, verifies the erase and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of $\overline{\text{WE}}$.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29F100T/B electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is complete, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

TABLE1. SOFTWARE COMMAND DEFINITIONS

Command		Bus	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Cycle	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset		1	XXXH	F0H										
Read		1	RA	RD										
Read Silicon ID	Word	4	555H	AAH	2AAH	55H	555H	90H	ADI	DDI				
	Byte	4	AAAH	AAH	555H	55H	AAAH	90H	ADI	DDI				
Sector Protect Verify	Word	4	555H	AAH	2AAH	55H	555H	90H	(SA) x02H	XX00H XX01H				
	Byte	4	AAAH	AAH	555H	55H	AAAH	90H	(SA) x04H	00H 01H				
Porgram	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
	Byte	4	AAAH	AAH	555H	55H	AAAH	A0H	PA	PD				
Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
	Byte	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	AAAH	10H
Sector Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
	Byte	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	SA	30H
Sector Erase Suspend		1	XXXH	B0H										
Sector Erase Resume		1	XXXH	30H										
Unlock for sector protect/unprotect		6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	20H

Note:

1. ADI = Address of Device identifier; A1=0, A0 = 0 for manufacture code,A1=0, A0 = 1 for device code. (Refer to table 3)
   DDI = Data of Device identifier : C2H for manufacture code, D9H/DFH(x8) and 22D9H/22DFH(x16) for device code.
   X = X can be VIL or VIH
   RA=Address of memory location to be read.
   RD=Data to be read at location RA.
2. PA = Address of memory location to be programmed.
   PD = Data to be programmed at location PA.
   SA = Address to the sector to be erased.
3. The system should generate the following address patterns: 555H or 2AAH to Address A10~A0 in word mode/ AAAH or 555H to Address A10~A-1 in byte mode.
   Address bit A11~A15=X=Don't care for all address commands except for Program Address (PA) and Sector Address (SA). Write Sequence may be initiated with A11~A15 in either state.
4. For Sector Protect Verify Operation : If read out data is 01H, it means the sector has been protected. If read out data is 00H, it means the sector is still not being protected.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 1 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device(when applicable).

TABLE 2. MX29F100T/B BUS OPERATION

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	D0 ~ Q15
Read Silicon ID Manfacturer Code(1)	L	L	H	L	L	X	V_{ID}(2)	C2H(Byte mode) 00C2H(Word mode)
Read Silicon ID Device Code(1)	L	L	H	H	L	X	V_{ID}(2)	D9H/DFH(Byte mode) 22D9H/22DFH (Word mode)
Read	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	D_{IN}(3)
Sector Protect with 12V system(6)	L	V_{ID}(2)	L	X	X	L	V_{ID}(2)	X
Chip Unprotect with 12V system(6)	L	V_{ID}(2)	L	X	X	H	V_{ID}(2)	X
Verify Sector Protect with 12V system	L	L	H	X	H	X	V_{ID}(2)	Code(5)
Sector Protect without 12V system (6)	L	H	L	X	X	L	H	X
Chip Unprotect without 12V system (6)	L	H	L	X	X	H	H	X
Verify Sector Protect/Unprotect without 12V system (7)	L	L	H	X	H	X	H	Code(5)
Reset	X	X	X	X	X	X	X	HIGH Z

NOTES:

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 12.5V.
3. Refer to Table 1 for valid Data-In during a write operation.
4. X can be VIL or VIH.
5. Code=00H/0000H means unprotected.
   Code=01H/0001H means protected.
   A15~A12=Sector address for sector protect.
6. Refer to sector protect/unprotect algorithm and waveform.
   Must issue "unlock for sector protect/unprotect" command before "sector protect/unprotect without 12V system" command.
7. The "verify sector protect/unprotect without 12V sysytem" is only following "Sector protect/unprotect without 12V system" command.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

SILICON-ID-READ COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX29F100T/B contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL, A0=VIL retrieves the manufacturer code of C2H/00C2H. A read cycle with A1=VIL, A0=VIH returns the device code of D9H/22D9H for MX29F100T, DFH/22DFH for MX29F100B.

SET-UP AUTOMATIC CHIP/BLOCK ERASE COMMANDS

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array(no erase verified command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the erase operation exceed internal timing limit.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

TABLE 3. EXPANDED SILICON ID CODE

Pins		A0	A1	Q15~Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code(Hex)
Manufacture code	**Word**	VIL	VIL	00H	1	1	0	0	0	0	1	0	00C2H
	Byte	VIL	VIL	X	1	1	0	0	0	0	1	0	C2H
Device code	**Word**	VIH	VIL	22H	0	0	0	1	1	0	1	1	22D9H
for MX29F100T	**Byte**	VIH	VIL	X	0	0	0	1	1	0	1	1	D9H
Device code	**Word**	VIH	VIL	22H	0	0	0	1	1	1	0	0	22DFH
for MX29F100B	**Byte**	VIH	VIL	X	0	0	0	1	1	1	0	0	DFH
Sector Protection Verification		X X	VIH VIH	X X	0 0	0 0	0 0	0 0	0 0	0 0	0 0	1 0	01H(Protected) 00H(Unprotected)

ERASE COMMANDS

The Automatic Block Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Block Erase command and Automatic Block Erase command. Upon executing the Automatic Block Erase command, the device will automatically program and verify the block(s) memory for an all-zero data pattern. The system does not require to provide any control or timing during these operations.

When the block(s) is automatically verified to contain an all-zero pattern, a self-timed block erase and verification begin. The erase and verification operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system does not require to provide any control or timing during these operations.

When using the Automatic Block Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verified command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of $\overline{WE}$, while the command(data) is latched on the rising edge of $\overline{WE}$. Block addresses selected are loaded into internal register on the sixth falling edge of $\overline{WE}$. Each successive block load cycle started by the falling edge of $\overline{WE}$ must begin within 80us from the rising edge of the preceding $\overline{WE}$. Otherwise, the loading period ends and internal auto block erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Block Erase (30H) or Erase Suspend (B0H) during the time-out period resets the derice to read mode.

ERASE SUSPEND

This command is only valid while the state machine is executing Automatic Block Erase operation, and therefore will only be responded to period during Automatic Block Erase operation. Writing the Erase Suspend command during the Block Erase time-out immediately terminates the time-out immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Read Memory Array, Erase Resume and Program commands.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended blocks.

Table 4. Write Operation Status

	Status		Q7	Q6	Q5	Q3	Q2	RY/$\overline{BY}$
In Progress	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	0	0	1	0
	Auto Erase Algorithm		0	Toggle	0	1	Toggle	0
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle (Note1)	1
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data	1
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{Q7}$	Toggle (Note2)	0	0	1 (Note3)	0
Exceeded Time Limits	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	1	0	1	0
	Program/Erase in Auto Erase Algorithm		0	Toggle	1	1	N/A	0
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{Q7}$	Toggle	1	1	N/A	0

Notes:
1.Performing successive read operations from the erase-suspended sector will cause Q2 to toggle.
2.Performing successive read operations from any address will cause Q6 to toggle.
3.Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the Q2 bit. However, successive reads from the erase-suspended sector will cause Q2 to toggle.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions.Another Erase Suspend command can be written after the chip has resumed erasing.

SET-UP AUTOMATIC PROGRAM COMMANDS

To initiate Automatic Program mode, a three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the Automatic Program command A0H.

Once the Automatic Program command is initiated, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are latched on the falling edge, and data are internally latched on the rising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin.

If the program opetation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the program operation exceed internal timing limit. The automatic programming operation is completed when the data read on Q6 stops toggling for two consecutive read cycles and the data on Q7 and Q6 are equivalent to data written to these two bits, at which time the device returns to the Read mode(no program verify command is required).

WRITE OPERATION STATUS

$\overline{DATA}$ POLLING-Q7

The MX29F100T/B also features $\overline{Data}$ Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the complement data of the data last written to Q7. Upon completion of the Automatic Program Algorithm an attempt to read the device will produce the true data last written to Q7. The $\overline{Data}$ Polling feature is valid after the rising edge of the fourth $\overline{WE}$ pulse of the four write pulse sequences for automatic program.

While the Automatic Erase algorithm is in operation, Q7 will read "0" until the erase operation is competed. Upon completion of the erase operation, the data on Q7 will read "1". The $\overline{Data}$ Polling feature is valid after the rising edge of the sixth $\overline{WE}$ pulse of six write pulse sequences for automatic chip/sector erase.

The $\overline{Data}$ Polling feature is active during Automatic Program/Erase algorithm or sector erase time-out.(see section Q3 Sector Erase Timer)

RY/$\overline{BY}$:Ready/$\overline{Busy}$

The RY/$\overline{BY}$ is a dedicated, open-drain output pin that indicates whether an Automatic Erase/Program algorithm is in progress or complete. The RY/$\overline{BY}$ status is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence. Since RY/$\overline{BY}$ is an open-drain output, several RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to Vcc.

If the outputs is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

TOGGLE BIT-Q6

The MX29F100T/B features a "Toggle Bit" as a method to indicate to the host system that the Auto Program/Erase algorithms are either in progress or completed.

While the Automatic Program or Erase algorithm is in progress, successive attempts to read data from the device will result in Q6 toggling between one and zero. Once the Automatic Program or Erase algorithm is completed, Q6 will stop toggling and valid data will be read. The toggle bit is valid after the rising edge of the sixth $\overline{WE}$ pulse of the six write pulse sequences for chip/sector erase.

The Toggle Bit feature is active during Automatic Program/Erase algorithms or sector erase time-out.(see section Q3 Sector Erase Timer)

Q5
Exceeded Timing Limits

Q5 will indicate if the program or erase time has exceeded the specified limits(internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector maynot be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

Q3
Sector Erase Timer

After the completion of the initial sector erase command sequenc the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

Reading Toggle Bits Q6

Whenever the system initally begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program ot erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

DATA PROTECTION

The MX29F100T/B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

TEMPORARY SECTOR UNPROTECT

This feature allows temporary unprotection of previously protected sector to change data in-system. The Temporary Sector Unprotect mode is activated by setting the $\overline{\text{RESET}}$ pin to VID(11.5V-12.5V). During this mode, formerly protected sectors can be programmed or erased as un-protected sector. Once VID is remove from the $\overline{\text{RESET}}$ pin, all the previously protected sectors are protected again.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns(typical) on $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibite by holding any one of $\overline{\text{OE}}$ = VIL, $\overline{\text{CE}}$ = VIH or $\overline{\text{WE}}$ = VIH. To initiate a write cycle $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be a logical zero while $\overline{\text{OE}}$ is a logical one.

POWER SUPPLY DECOUPLING

In order to reduced power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

SECTOR PROTECTION WITH 12V SYSTEM

The MX29F100T/B features hardware sector protection. This feature will disable both program and erase operations for these sectors protected. To activate this mode, the programming equipment must force VID on address pin A9 and control pin $\overline{\text{OE}}$, (suggest VID = 12V) A6 = VIL and $\overline{\text{CE}}$ = VIL.(see Table 2) Programming of the protection circuitry begins on the falling edge of the $\overline{\text{WE}}$ pulse and is terminated on the rising edge. Please refer to sector protect algorithm and waveform.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 (with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ at VIL and $\overline{\text{WE}}$ at VIH. When A1=1, it will produce a logical "1" code at device output Q0 for a protected sector. Otherwise the device will produce 00H for the unprotected sector. In this mode, the address,except for A1, are in "don't care" state. Address locations with A1 = VIL are reserved to read manufacturer and device codes.(Read Silicon ID)

It is also possible to determine if the sector is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected sector.

CHIP UNPROTECT WITH 12V SYSTEM

The MX29F100T/B also features the chip unprotect mode, so that all sectors are unprotected after chip unprotect is completed to incorporate any changes in the code. It is recommended to protect all sectors before activating chip unprotect mode.

To activate this mode, the programming equipment must force VID on control pin $\overline{\text{OE}}$ and address pin A9. The $\overline{\text{CE}}$ pins must be set at VIL. Pins A6 must be set to VIH.(see Table 2) Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotection mechanism begins on the falling edge of the $\overline{\text{WE}}$ pulse and is terminated on the rising.

It is also possible to determine if the chip is unprotected in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs(Q0-Q7) for an unprotected sector. It is noted that all sectors are unprotected after the chip unprotect algorithm is completed.

SECTOR PROTECTION WITHOUT 12V SYSTEM

The MX29F100T/B also feature a hardware sector protection method in a system without 12V power suppply. The programming equipment do not need to supply 12 volts to protect sectors. The details are shown in sector protect algorithm and waveform.

CHIP UNPROTECT WITHOUT 12V SYSTEM

The MX29F100T/B also feature a hardware chip unprotection method in a system without 12V power supply. The programming equipment do not need to supply 12 volts to unprotect all sectors. The details are shown in chip unprotect algorithm and waveform.

POWER-UP SEQUENCE

The MX29F100T/B powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
A9 & $\overline{OE}$ & $\overline{RESET}$	-0.5V to 13.5V

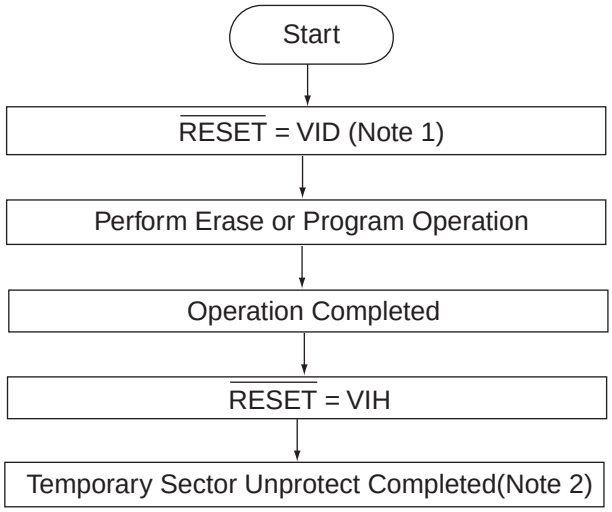
NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

CAPACITANCE TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			8	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOUT = 0V

Temporary Sector Unprotect Operation



Note : 1. All protected sectors are temporary unprotected.
VID=11.5V~12.5V
2. All previously protected sectors are protected again.

READ OPERATION

DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			1	uA	VIN = GND to VCC
ILO	Output Leakage Current			10	uA	VOUT = GND to VCC
ISB1	Standby VCC current			1	mA	$\overline{CE}$ = VIH
ISB2			1	5	uA	$\overline{CE}$ = VCC + 0.3V
ICC1	Operating VCC current			30	mA	IOUT = 0mA, f=1MHz
ICC2				50	mA	IOUT = 0mA, f=10MHz
VIL	Input Low Voltage	-0.3(NOTE 1)		0.8	V	
VIH	Input High Voltage	2.0		VCC + 0.3	V	
VOL	Output Low Voltage			0.45	V	IOL = 2.1mA
VOH	Output High Voltage	2.4			V	IOH = -2mA

NOTES:

1. VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns
   If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

		29F100T/B-70		29F100T/B-90		29F100T/B-12			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		70		90		120	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		70		90		120	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		40		40		50	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Float (Note1)	0	20	0	30	0	30	ns	$\overline{CE}$=VIL
tOH	Address to Output hold	0		0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL

AC CHARACTERISTICS TA = 0°C to 70°C

		29F100T/B-55			
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		55	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		55	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		30	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Float (Note1)	0	20	ns	$\overline{CE}$=VIL
tOH	Address to Output hold	0		ns	$\overline{CE}$=$\overline{OE}$=VIL

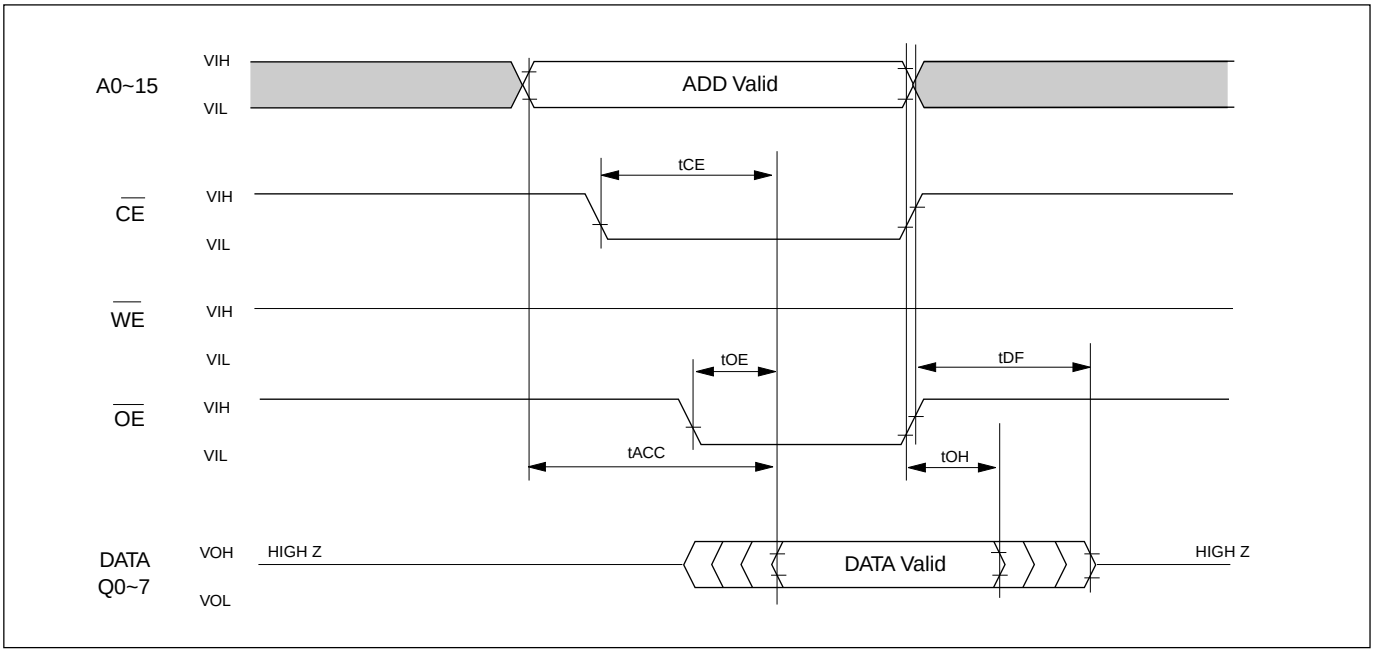
TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V for 70ns max. ; 0V/3.0V for 55ns
- Input rise and fall times: ≤ 10ns for 70ns max. ; ≤ 5ns for 55ns
- Output load: 1 TTL gate + 100pF (Including scope and jig) for 70ns max. ; 1 TTL gate + 30pF (Including scope and jig) for 55ns
- Reference levels for measuring timing: 0.8V & 2.0V for 70ns max. ; 1.5V for 55ns

NOTE:

1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

READ TIMING WAVEFORMS



COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION

DC CHARACTERISTICS TA = 0ºC to 70ºC, VCC = 5V ± 10%

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ICC1 (Read)	Operating VCC Current			30	mA	IOUT=0mA, f=1MHz
ICC2				50	mA	IOUT=0mA, F=10MHz
ICC3 (Program)				50	mA	In Programming
ICC4 (Erase)				50	mA	In Erase
ICCES	VCC Erase Suspend Current		2		mA	CE=VIH, Erase Suspended

NOTES:

1. VIL min. = -0.6V for pulse width is equal to or less than 20ns.
2. If VIH is over the specified maximum value, programming operation cannot be guranteed.
3. ICCES is specified with the device de-selected. If the device is read during erase suspend mode, current draw is the sum of ICCES and ICC1 or ICC2.
4. All current are in RMS unless otherwise noted.

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

		29F100T/B-70		29F100T/B-90		29F100T/B-12			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tOES	$\overline{OE}$ setup time	0		0		0		ns	
tCWC	Command programming cycle	70		90		120		ns	
tCEP	$\overline{WE}$ programming pulse width	35		45		50		ns	
tCEPH1	$\overline{WE}$ programming pluse width High	20		20		20		ns	
tCEPH2	$\overline{WE}$ programming pluse width High	20		20		20		ns	
tAS	Address setup time	0		0		0		ns	
tAH	Address hold time	45		45		50		ns	
tDS	Data setup time	30		45		50		ns	
tDH	Data hold time	0		0		0		ns	
tCESC	$\overline{CE}$ setup time before command write	0		0		0		ns	
tDF	Output disable time (Note 1)		30		40		40	ns	
tAETC	Total erase time in auto chip erase	2(TYP.)		2(TYP.)		2(TYP.)		s	
tAETB	Total erase time in auto block erase	1(TYP.)		1(TYP.)		1(TYP.)		s	
tAVT	Total programming time in auto verify	7/14(TYP.)		7/14(TYP.)		7/14(TYP.)		us	
tBAL	Block address load time	80		80		80		us	
tCH	$\overline{CE}$ Hold Time	0		0		0		ns	
tCS	$\overline{CE}$ setup to WE going low	0		0		0		ns	
tVLHT	Voltge Transition Time	4		4		4		us	
tOESP	$\overline{OE}$ Setup Time to $\overline{WE}$ Active	4		4		4		us	
tWPP1	Write pulse width for sector protect	10		10		10		us	
tWPP2	Write pulse width for sector unprotect	12		12		12		ms	

NOTES:

1. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.

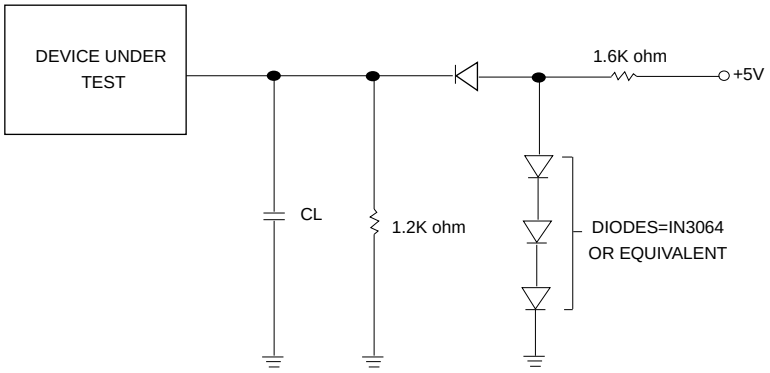
AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

SYMBOL	PARAMETER	29F100T/B-55 MIN.	MAX.	UNIT	CONDITIONS
tOES	$\overline{OE}$ setup time	0		ns	
tCWC	Command programming cycle	55		ns	
tCEP	$\overline{WE}$ programming pulse width	30		ns	
tCEPH1	$\overline{WE}$ programming pluse width High	20		ns	
tCEPH2	$\overline{WE}$ programming pluse width High	20		ns	
tAS	Address setup time	0		ns	
tAH	Address hold time	45		ns	
tDS	Data setup time	20		ns	
tDH	Data hold time	0		ns	
tCESC	$\overline{CE}$ setup time before command write	0		ns	
tDF	Output disable time (Note 1)		20	ns	
tAETC	Total erase time in auto chip erase	2(TYP.)		s	
tAETB	Total erase time in auto block erase	1(TYP.)		s	
tAVT	Total programming time in auto verify	7/14(TYP.)		us	
tBAL	Block address load time	80		us	
tCH	$\overline{CE}$ Hold Time	0		ns	
tCS	$\overline{CE}$ setup to WE going low	0		ns	
tVLHT	Voltge Transition Time	4		us	
tOESP	$\overline{OE}$ Setup Time to $\overline{WE}$ Active	4		us	
tWPP1	Write pulse width for sector protect	10		us	
tWPP2	Write pulse width for sector unprotect	12		ms	

NOTES:

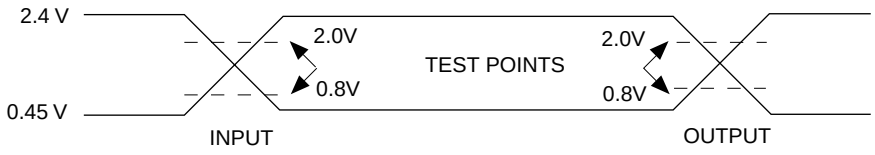
1. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.

SWITCHING TEST CIRCUITS



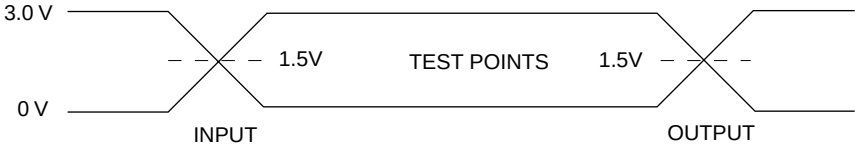
CL=100pF Including jig capacitance for 70ns max.
30pF Including jig capacitance for 55ns

SWITCHING TEST WAVEFORMS(I) for 70ns max.



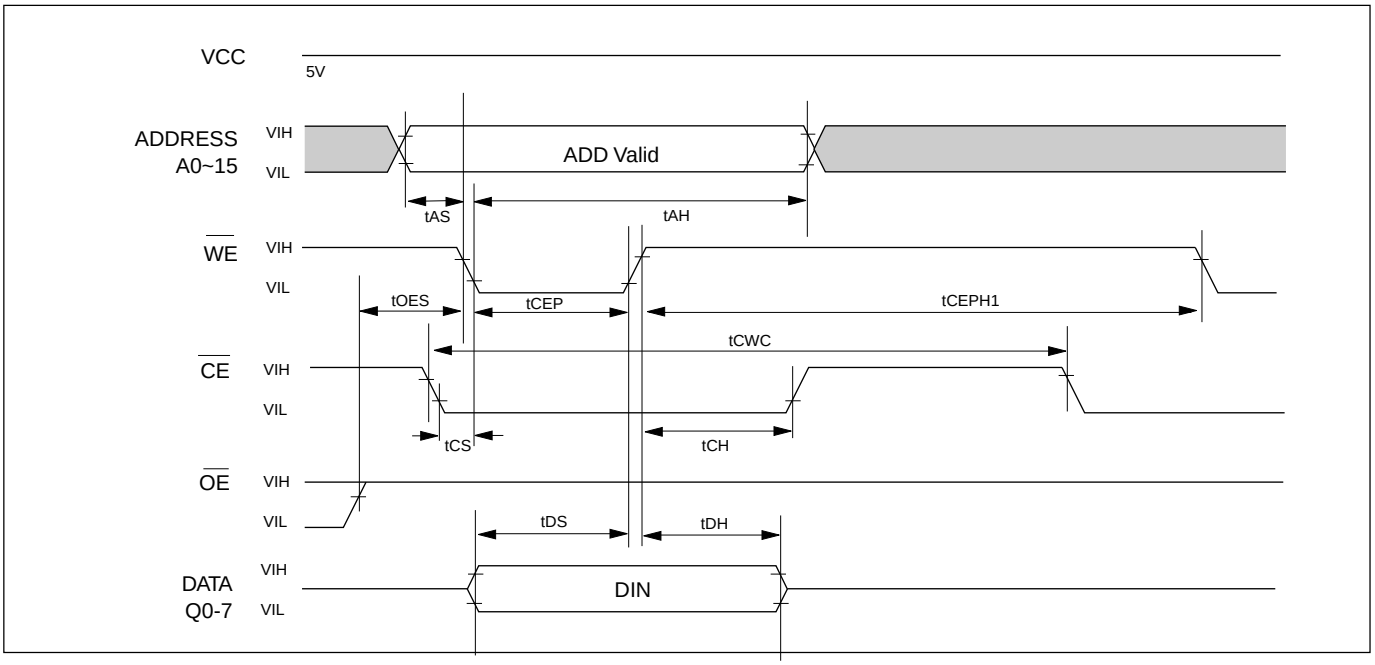
AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are < 10ns.

SWITCHING TEST WAVEFORMS(II) for 55ns



AC TESTING: Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are < 5ns.

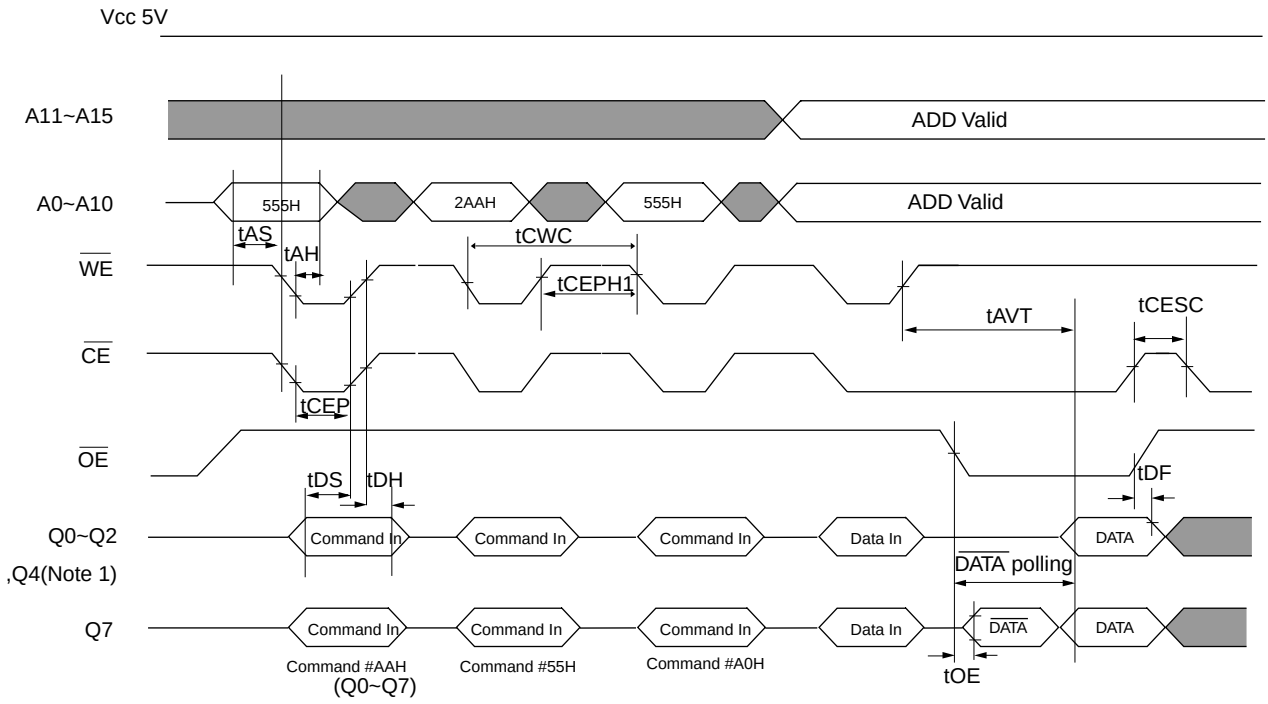
COMMAND WRITE TIMING WAVEFORM



AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional programming by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by DATA polling and toggle bit checking after automatic verification starts. Device outputs DATA during programming and DATA after programming on Q7.(Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

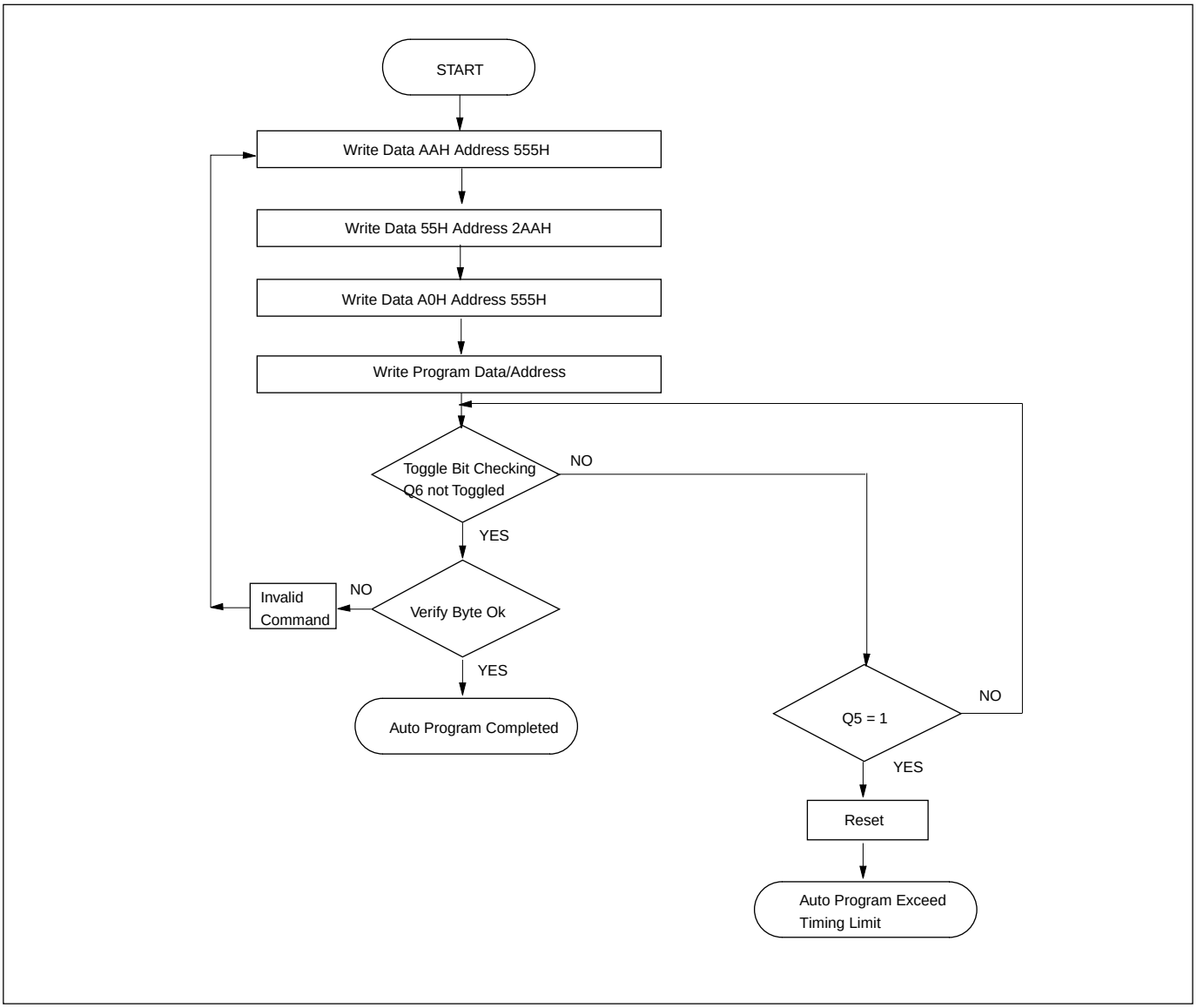
AUTOMATIC PROGRAMMING TIMING WAVEFORM (WORD MODE)



Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit

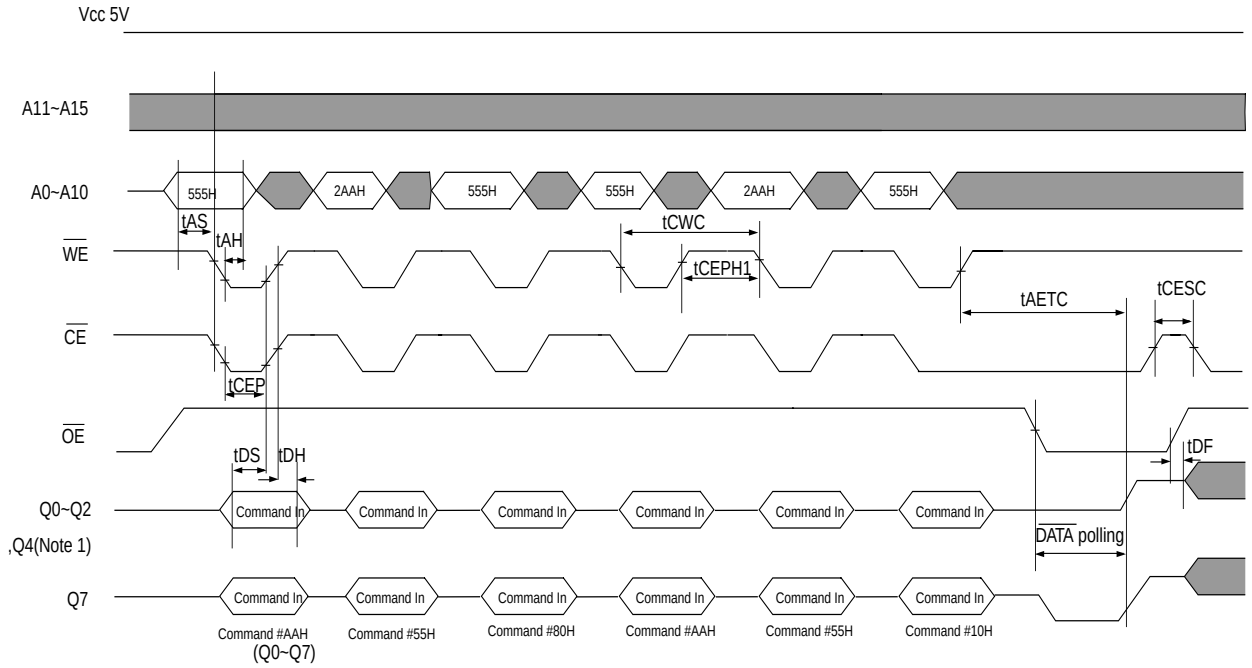
AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART (WORD MODE)



AUTOMATIC CHIP ERASE TIMING WAVEFORM

All data in chip are erased. External erase verification is not required because data is erased automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure 0n Q7.(Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

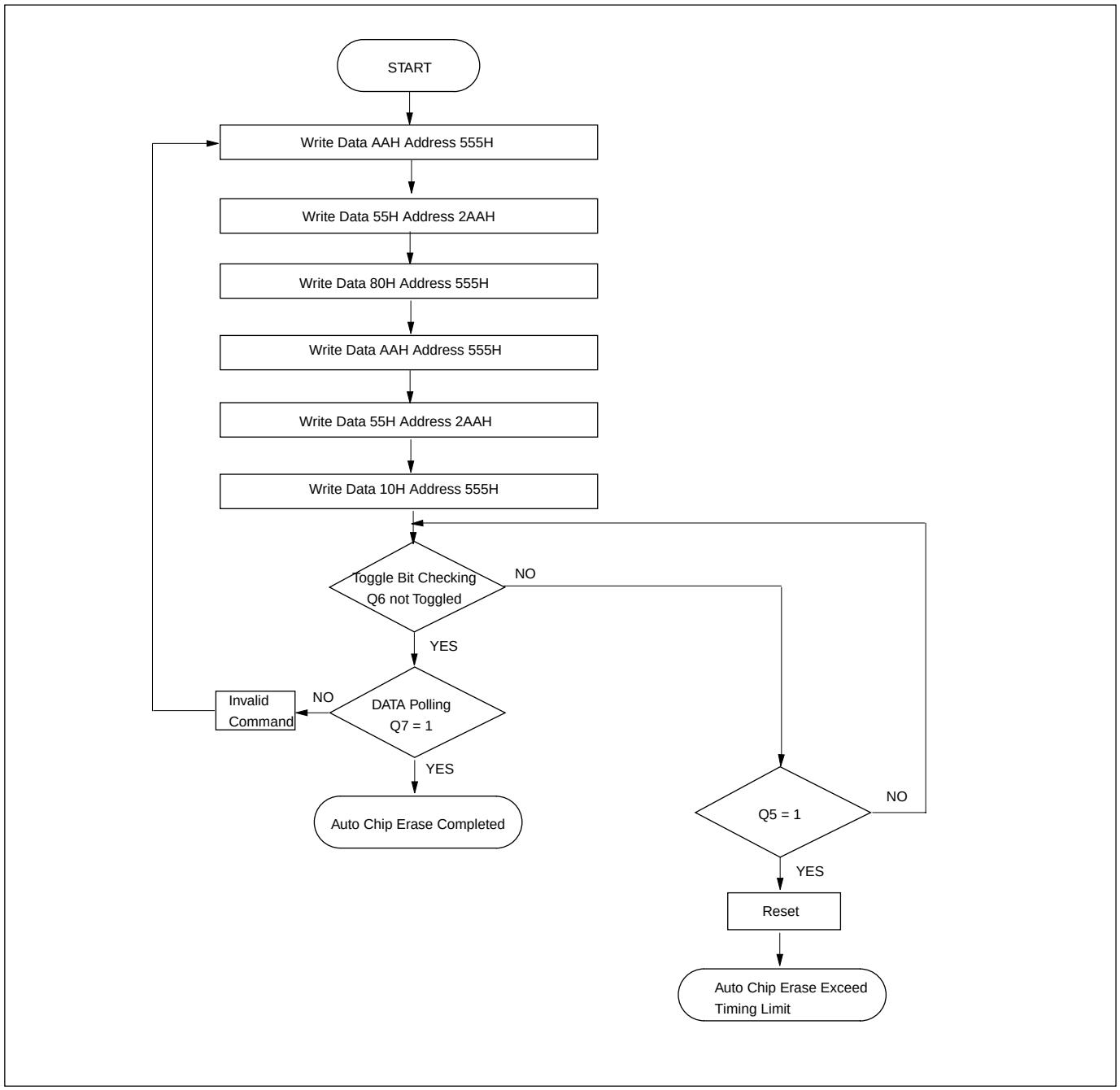
AUTOMATIC CHIP ERASE TIMING WAVEFORM (WORD MODE)



Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit

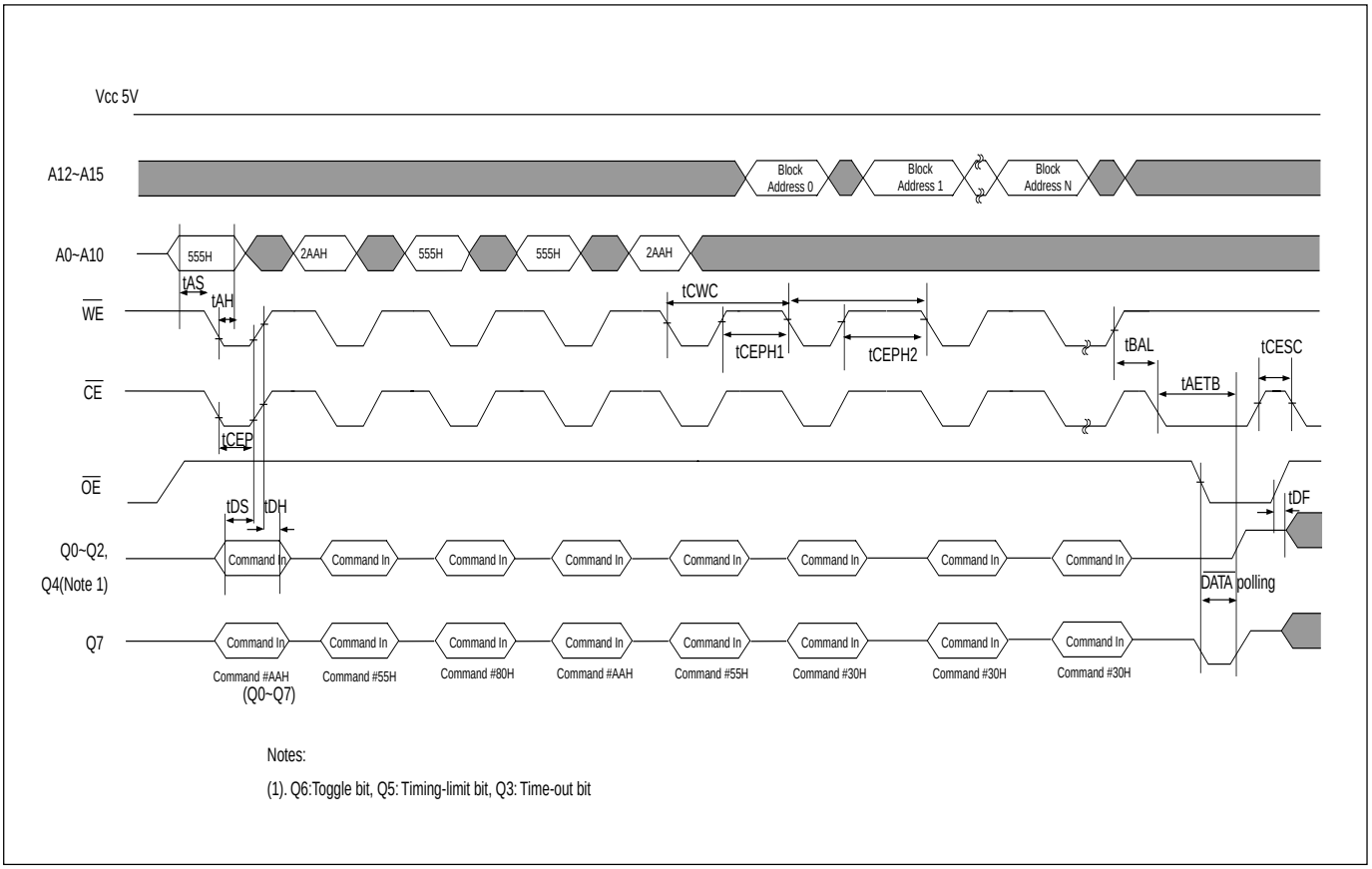
AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART (WORD MODE)



AUTOMATIC BLOCK ERASE TIMING WAVEFORM

Block data indicated by A12 to A15 are erased. External erase verification is not required because data are erased automatically by internal control circuit. Erasure completion can be verified by $\overline{\text{DATA}}$ polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{\text{DATA}}$ polling, timing waveform)

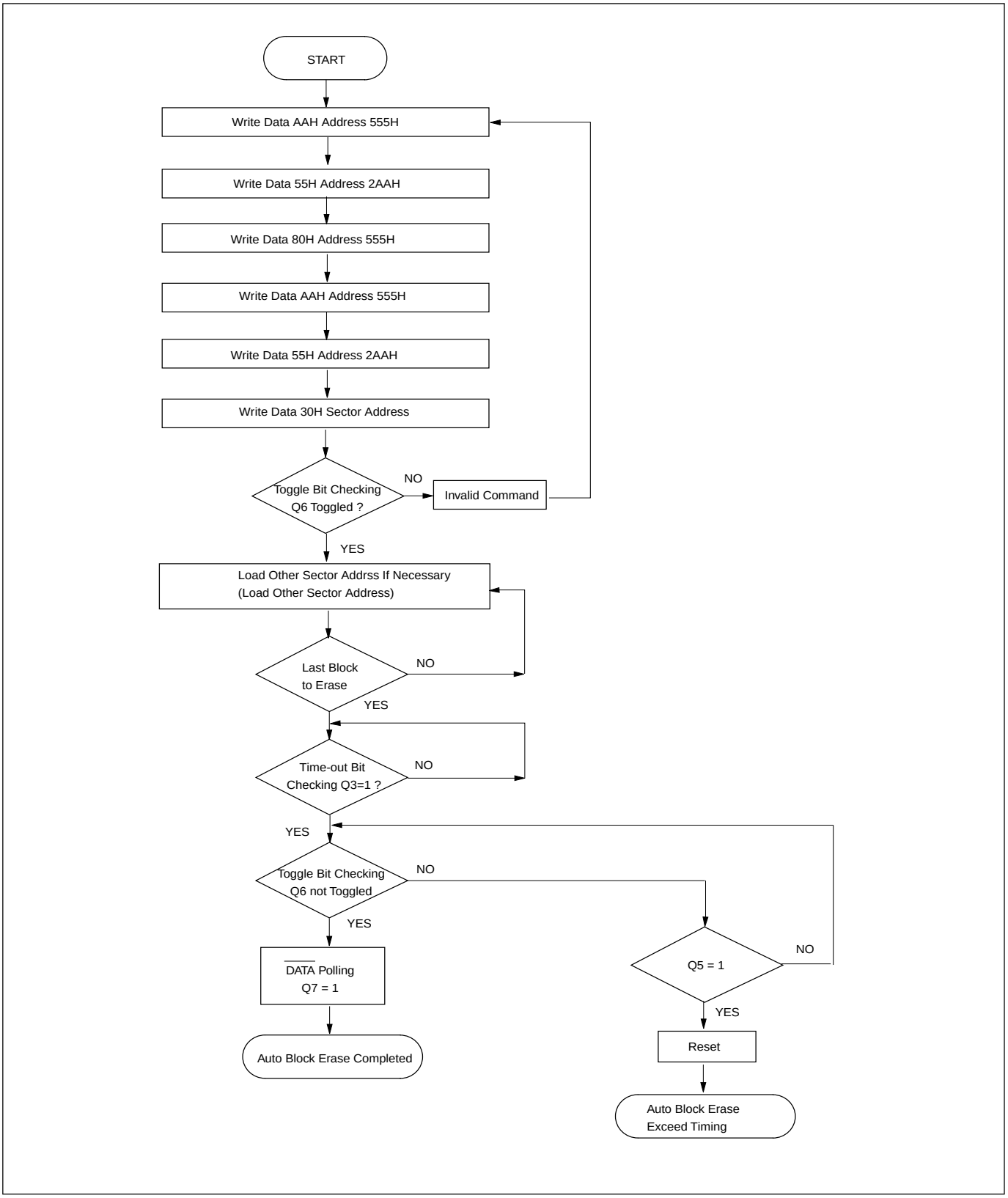
AUTOMATIC BLOCK ERASE TIMING WAVEFORM (WORD MODE)



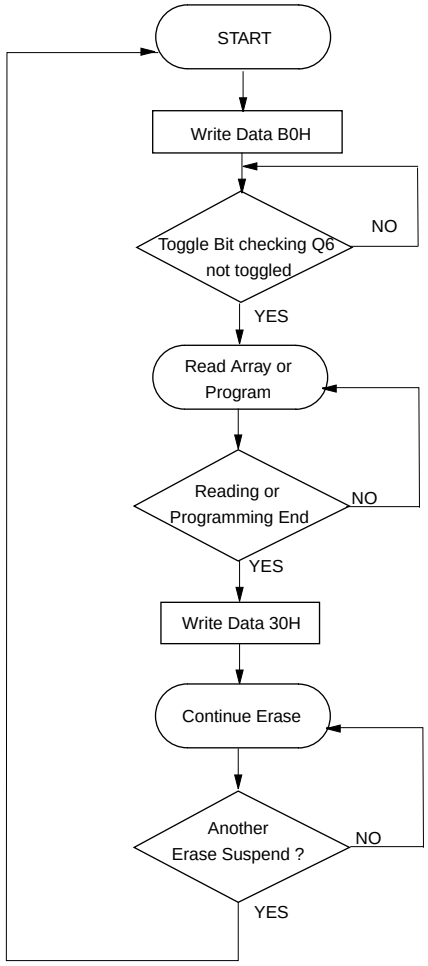
Notes:

(1). Q6:Toggle bit, Q5: Timing-limit bit, Q3: Time-out bit

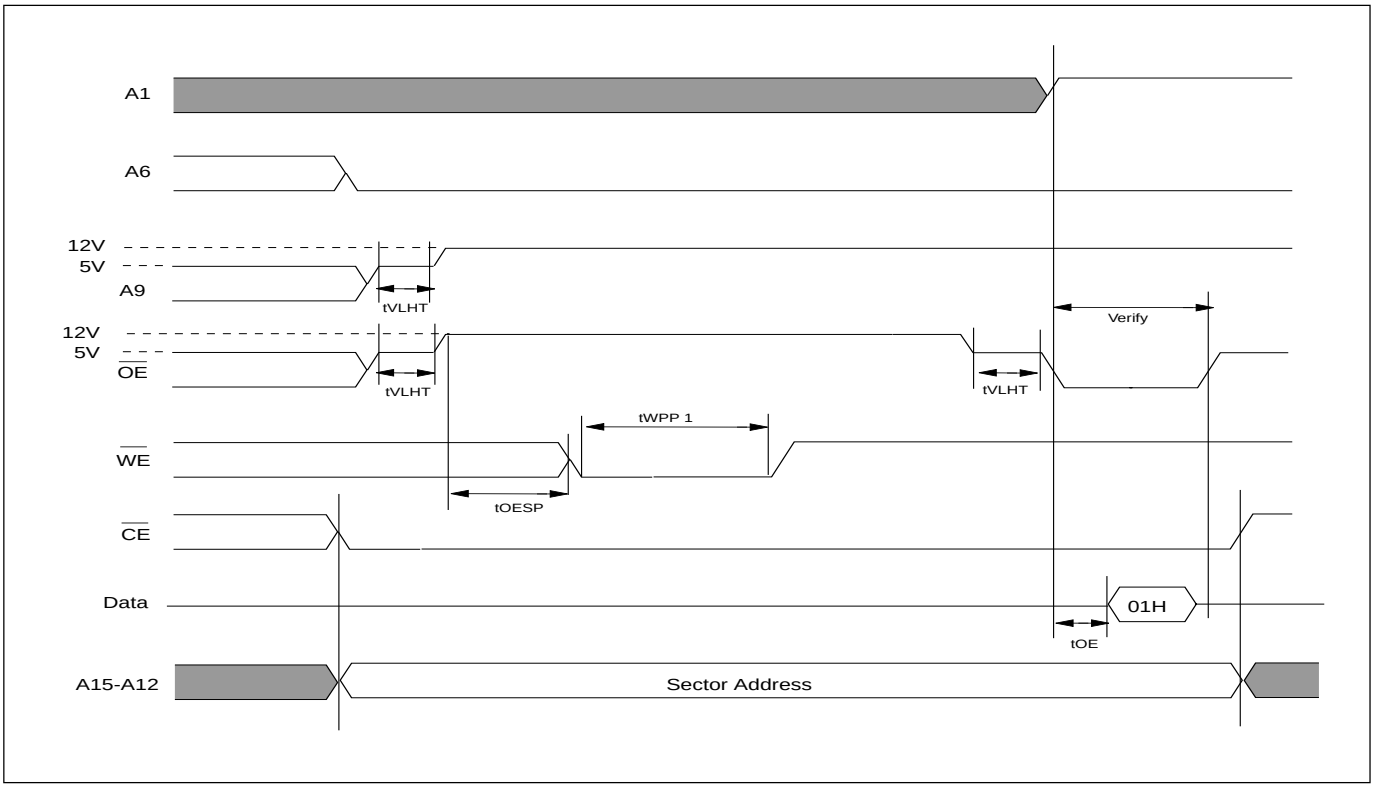
AUTOMATIC BLOCK ERASE ALGORITHM FLOWCHART



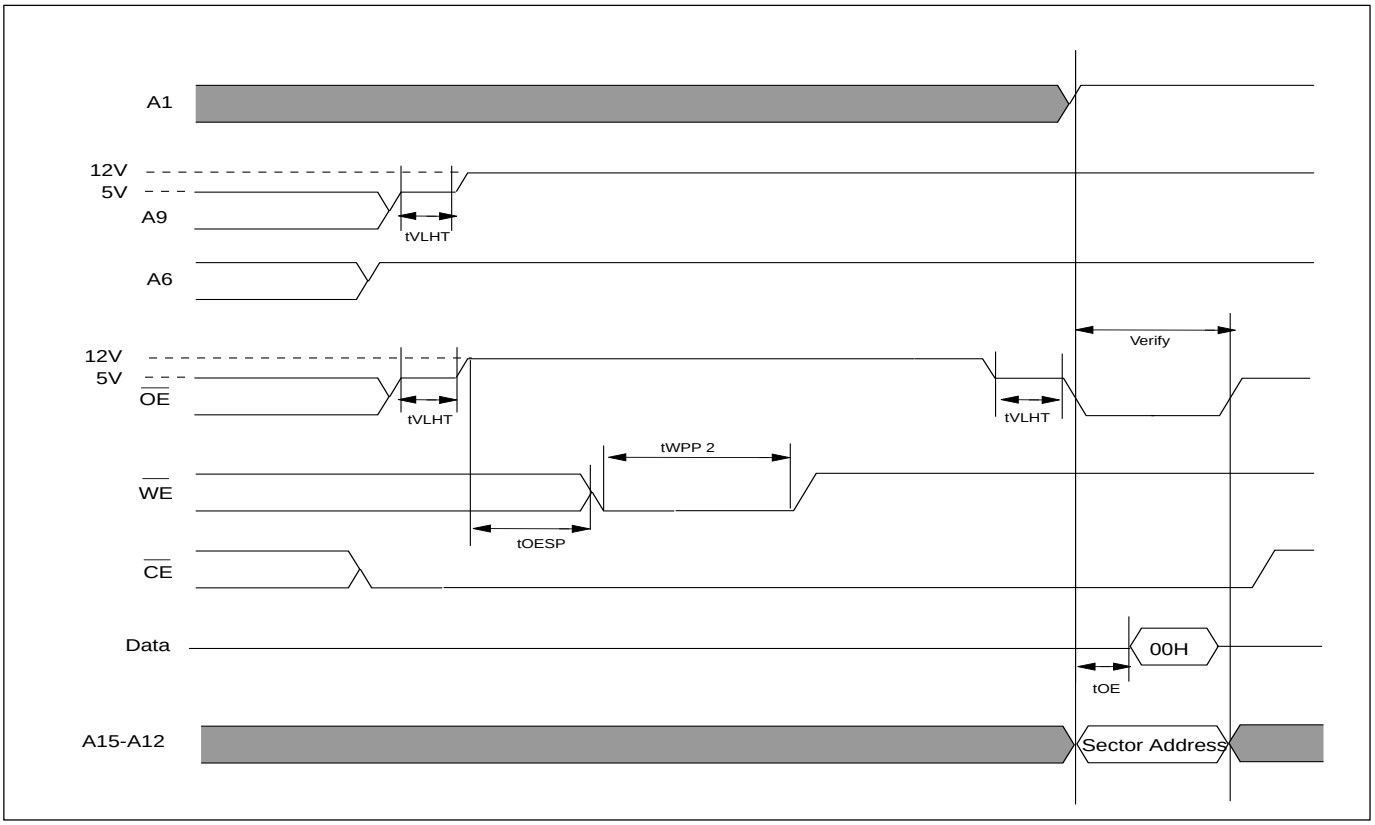
ERASE SUSPEND/ERASE RESUME FLOWCHART



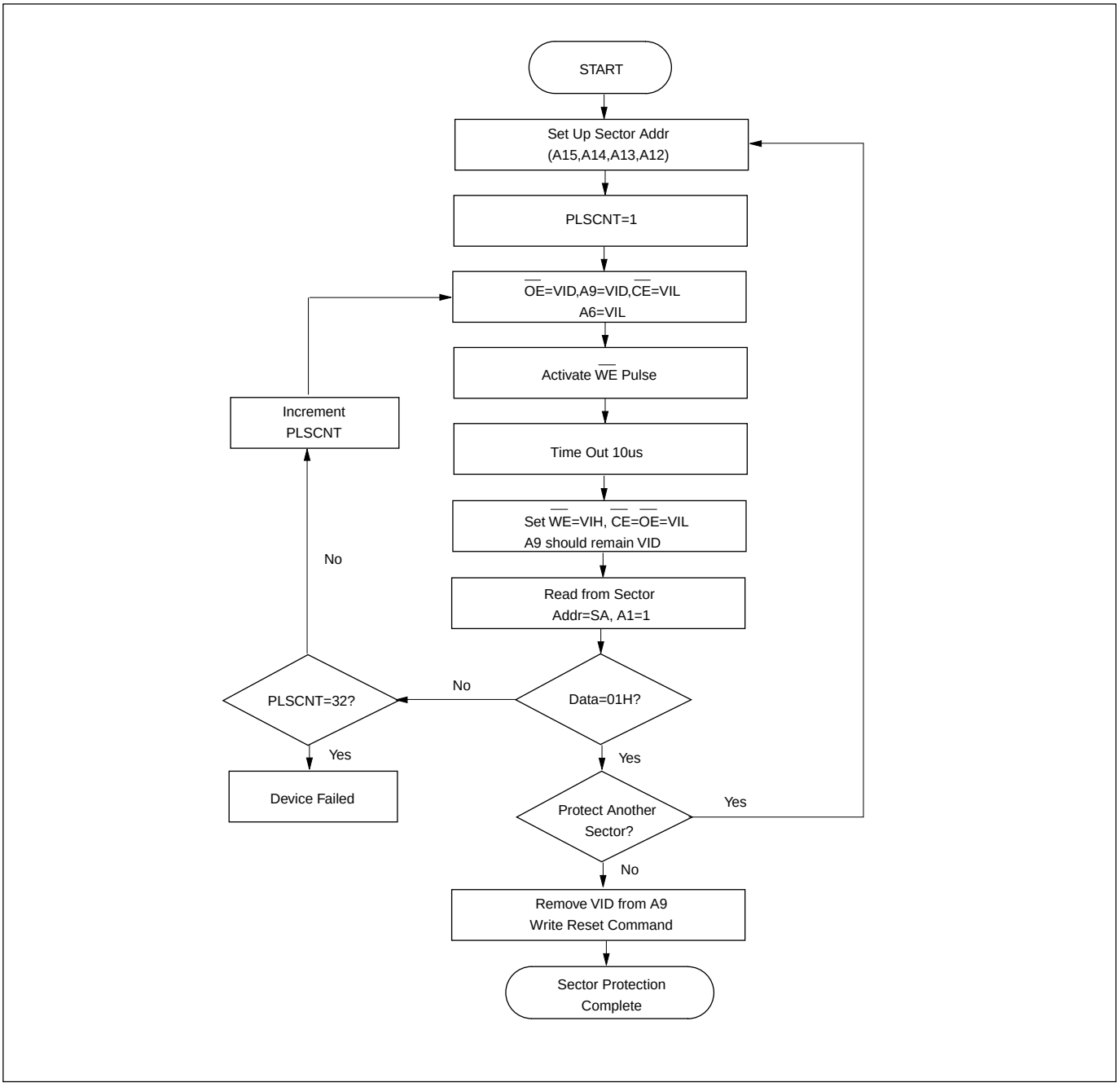
TIMING WAVEFORM FOR SECTOR PROTECTION FOR SYSTEM WITH 12V



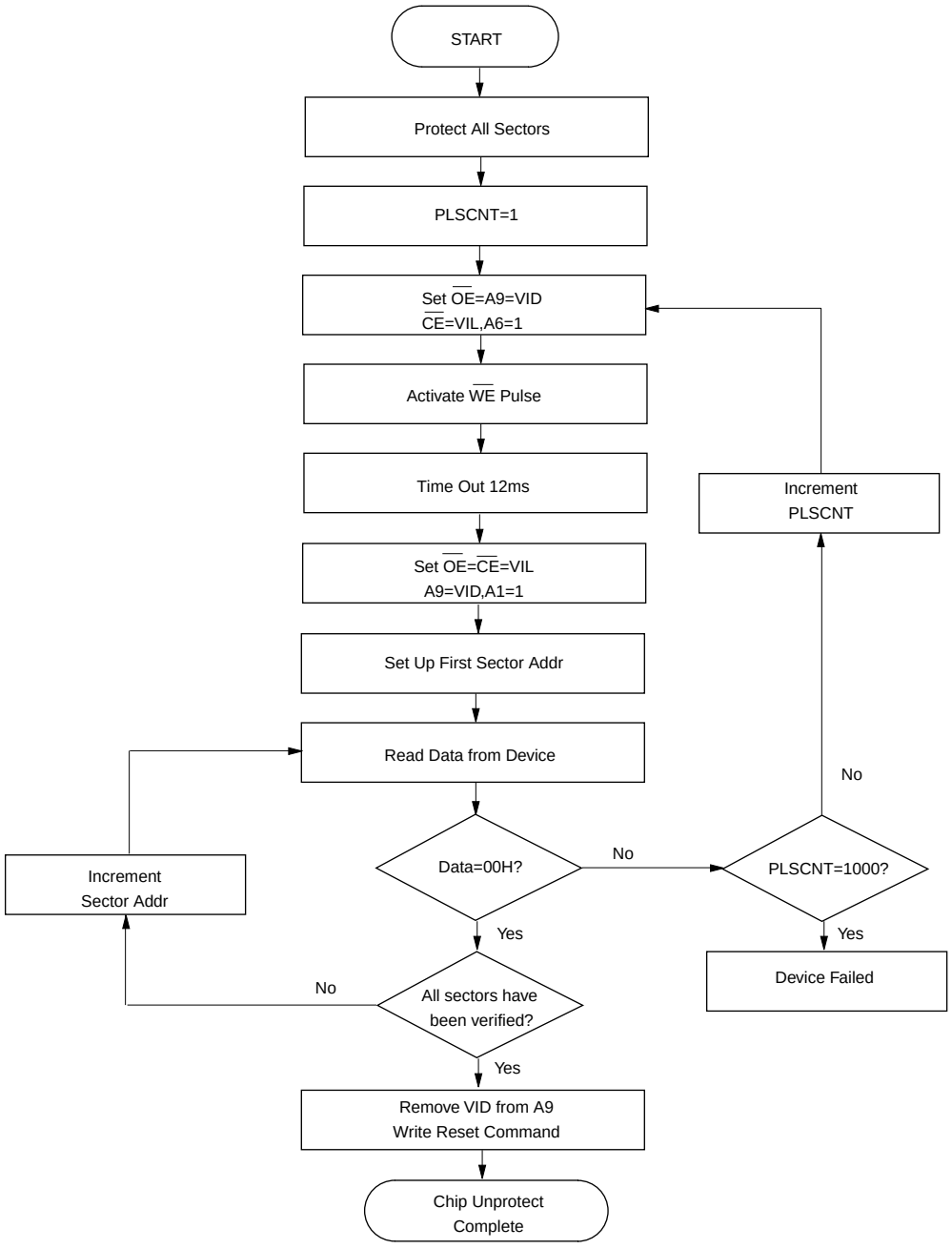
TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITH 12V



SECTOR PROTECTION ALGORITHM FOR SYSTEM WITH 12V

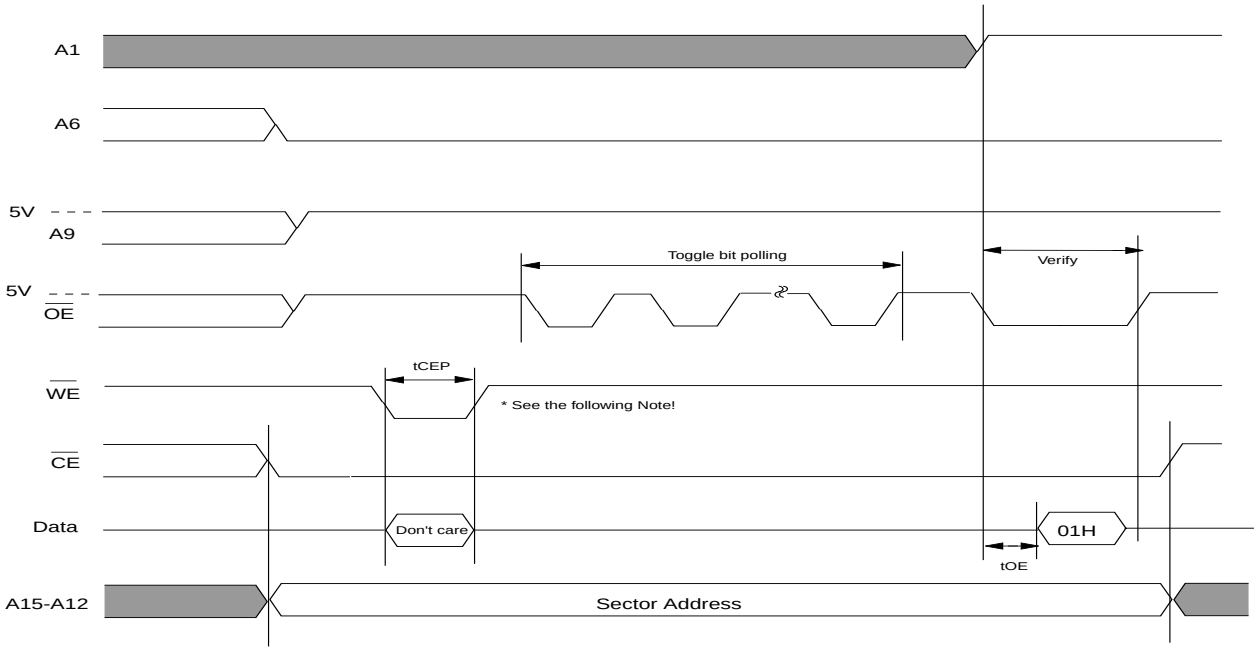


SECTOR UNPROTECTION ALGORITHM FOR SYSTEM WITH 12V



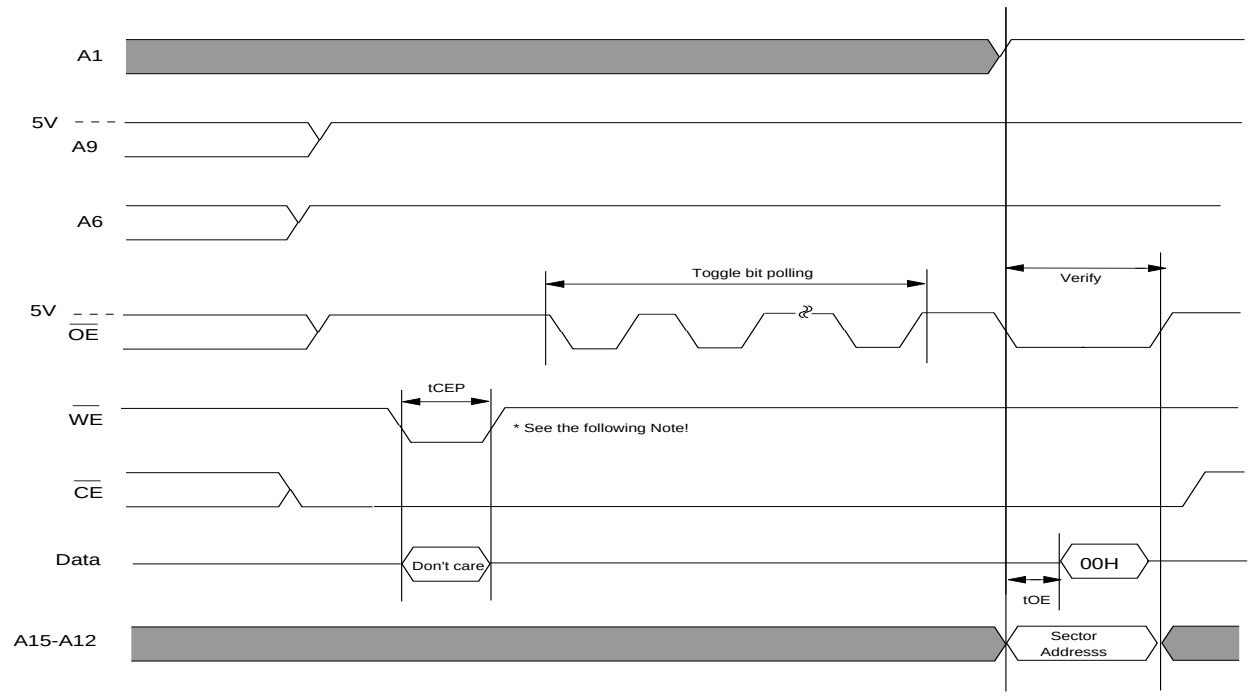
* It is recommended before unprotect the whole chip, all sectors should be protected in advance.

TIMING WAVEFORM FOR SECTOR PROTECTION FOR SYSTEM WITHOUT 12V



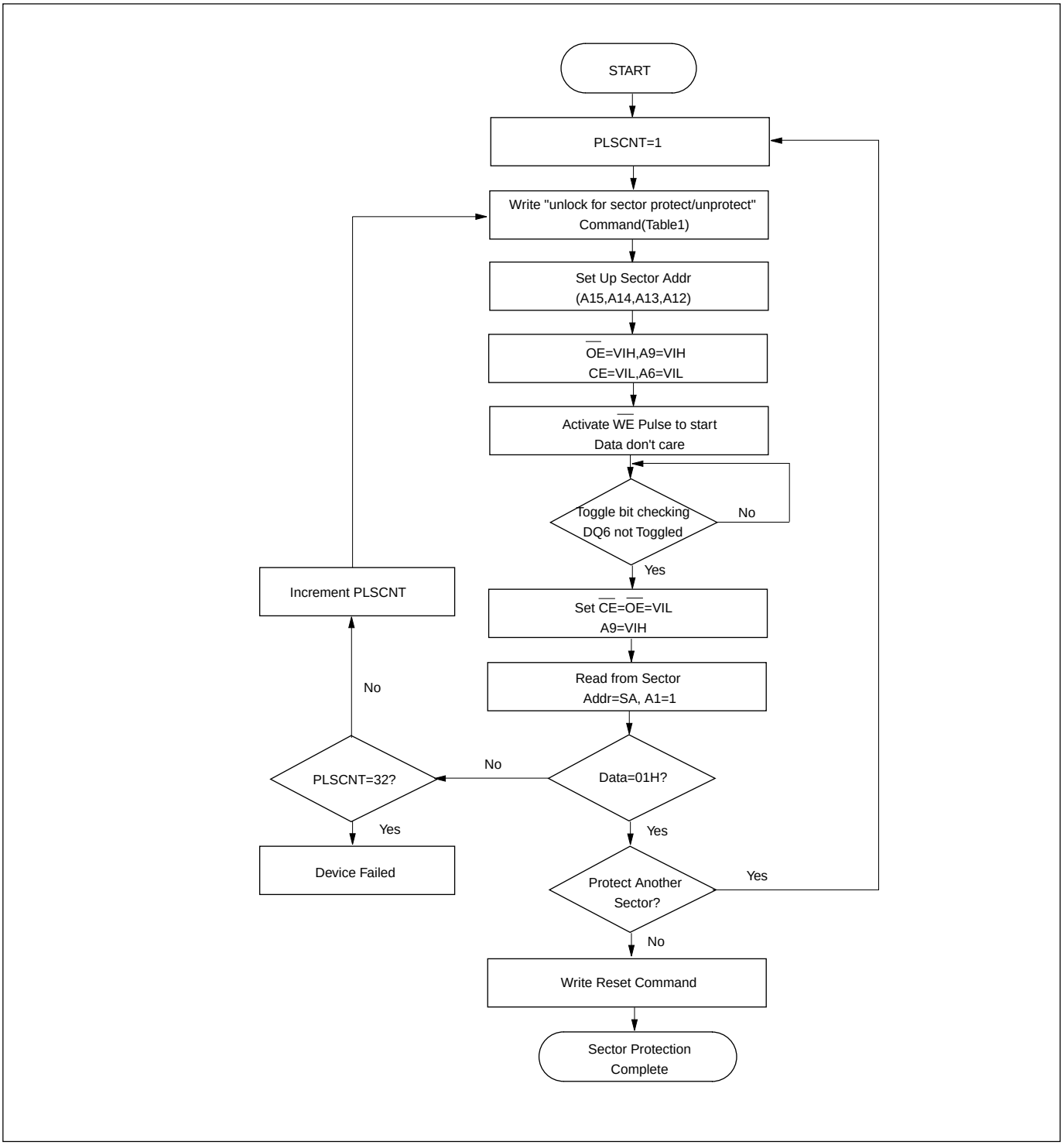
Note: Must issue "unlock for sector protect/unprotect" command before sector protection for a system without 12V provided.

TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITHOUT 12V

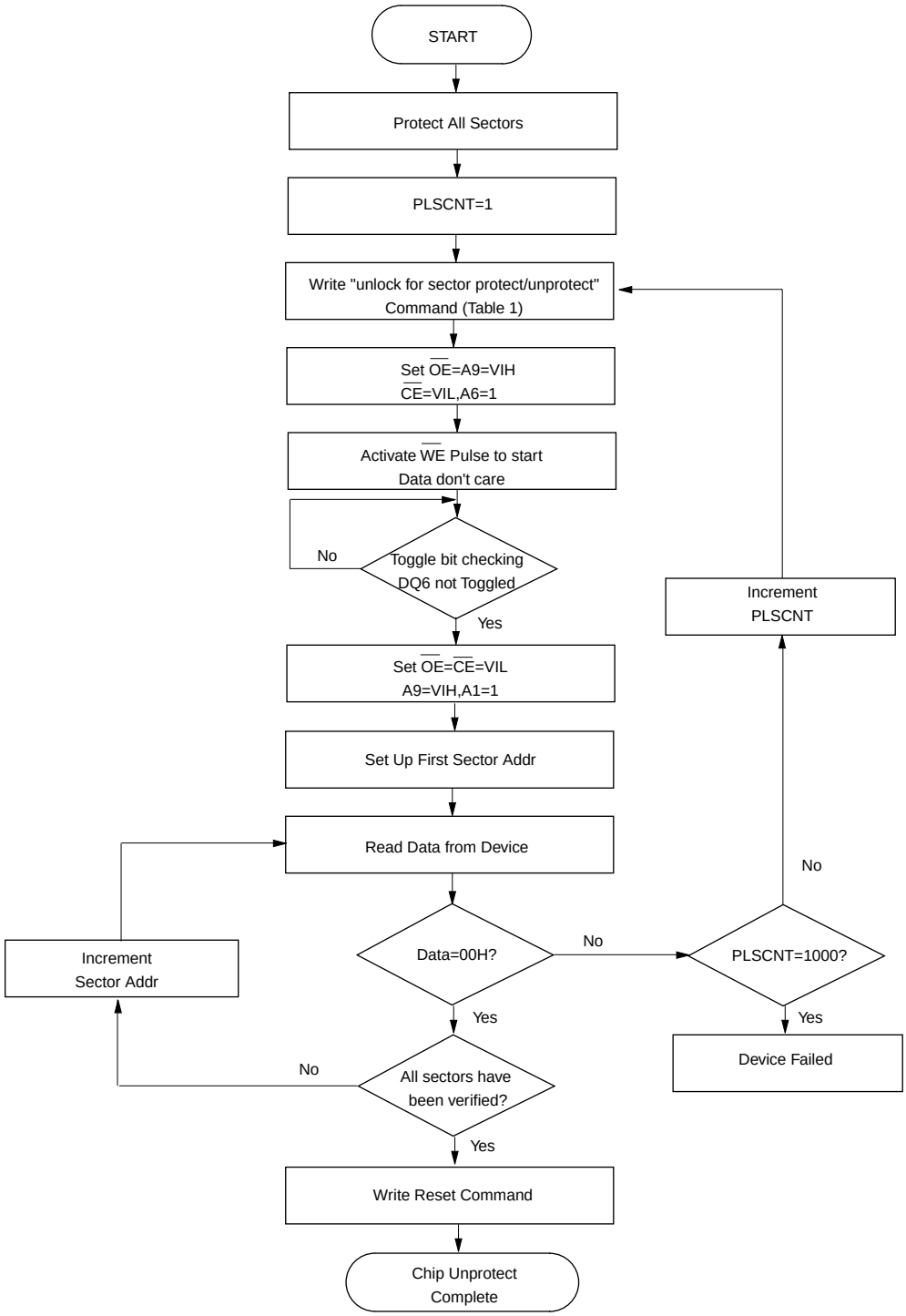


Note: Must issue "unlock for sector protect/unprotect" command before sector unprotection for a system without 12V provided.

SECTOR PROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V

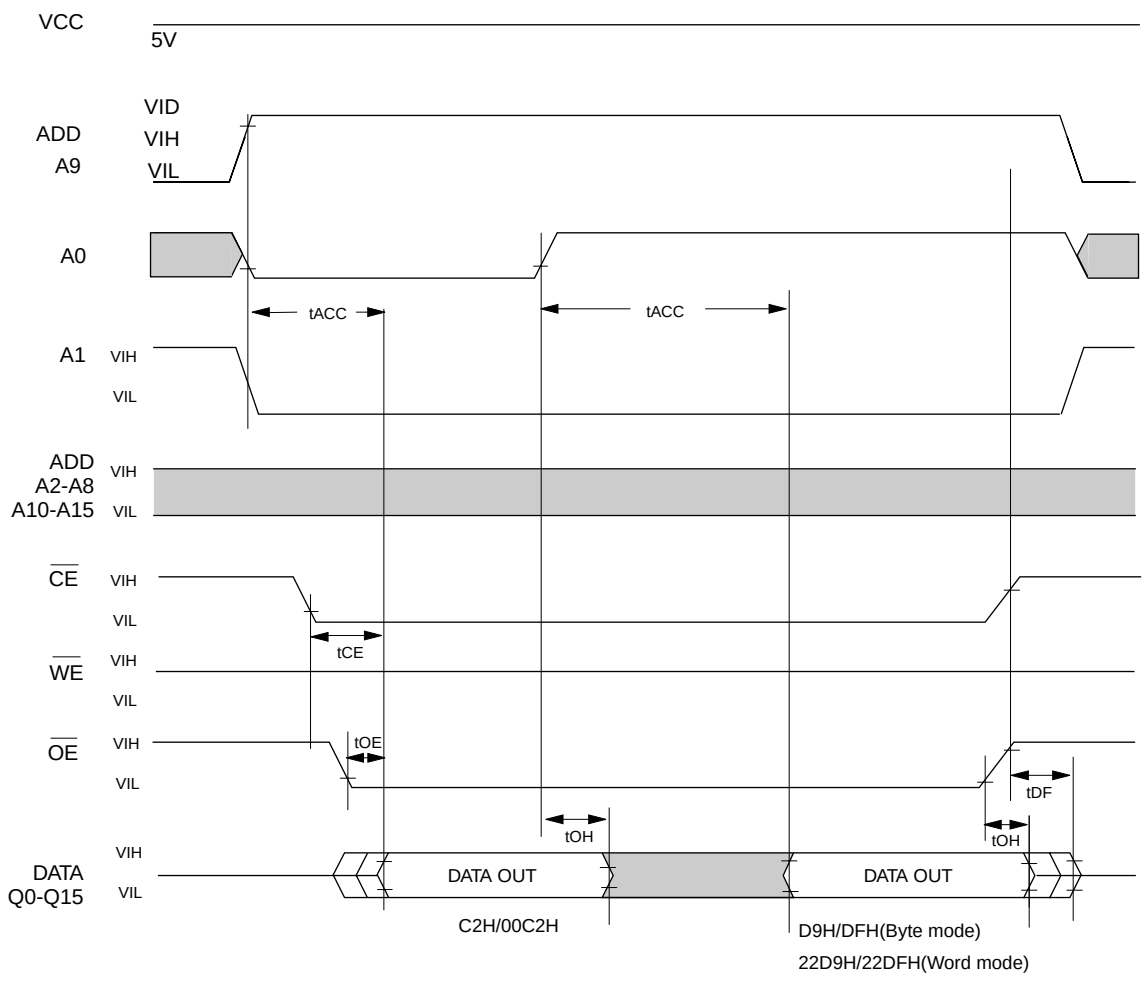


SECTOR UNPROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V



* It is recommended before unprotect the whole chip, all sectors should be protected in advance.

ID CODE READ TIMING WAVEFORM



ORDERING INFORMATION

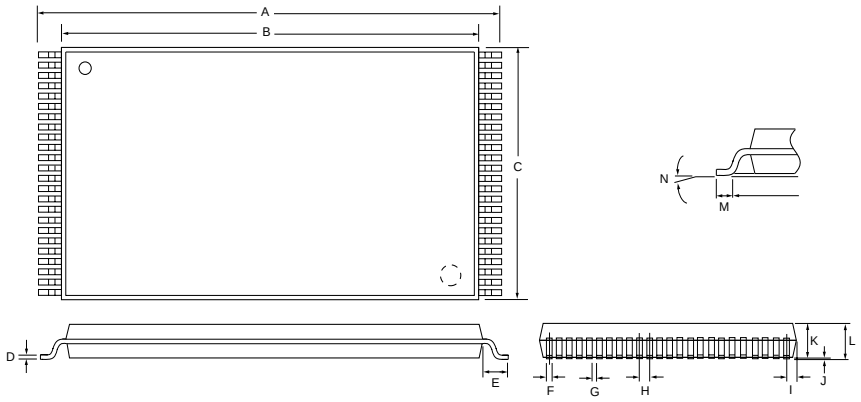
PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE
MX29F100TMC-55	55	50	100	44 Pin SOP
MX29F100TMC-70	70	50	100	44 Pin SOP
MX29F100TMC-90	90	50	100	44 Pin SOP
MX29F100TMC-12	120	50	100	44 Pin SOP
MX29F100TTC-55	55	50	100	48 Pin TSOP (Normal Type)
MX29F100TTC-70	70	50	100	48 Pin TSOP (Normal Type)
MX29F100TTC-90	90	50	100	48 Pin TSOP (Normal Type)
MX29F100TTC-12	120	50	100	48 Pin TSOP (Normal Type)
MX29F100TRC-55	55	50	100	48 Pin TSOP (Reverse Type)
MX29F100TRC-70	70	50	100	48 Pin TSOP (Reverse Type)
MX29F100TRC-90	90	50	100	48 Pin TSOP (Reverse Type)
MX29F100TRC-12	120	50	100	48 Pin TSOP (Reverse Type)

48-PIN PLASTIC TSOP

ITEM	MILLIMETERS	INCHES
A	20.0 ± .20	.787 ± .008
B	18.40 ± .10	.724 ± .004
C	12.20 max.	.480 max.
D	0.15 [Typ.]	.006 [Typ.]
E	.80 [Typ.]	.031 [Typ.]
F	.20 ± .10	.008 ±.004
G	.30 ± .10	.012 ± .004
H	.50 [Typ.]	.020 [Typ.]
I	.45 max.	.018 max.
J	0 ~ .20	0 ~ .008
K	1.00 ± .10	.039 ± .004
L	1.27 max.	.050 max.
M	.50	.020
N	0 ~ 5°	.500

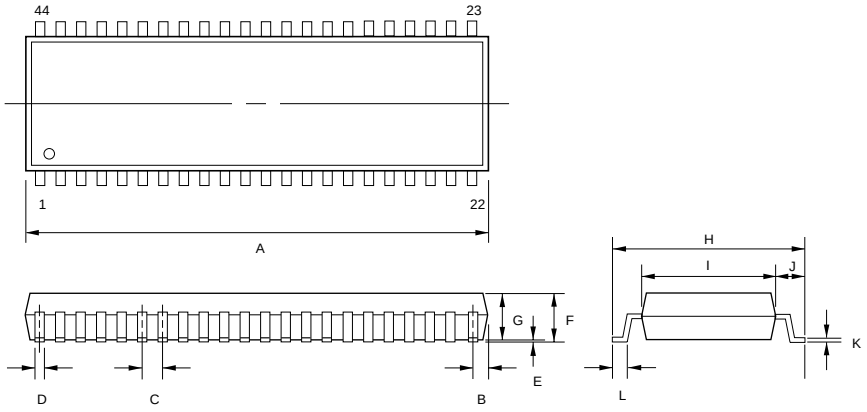
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



44-PIN PLASTIC SOP

ITEM	MILLIMETERS	INCHES
A	28.70 max.	1.130 max.
B	1.10 [REF]	.043 [REF]
C	1.27 [TP]	.050 [TP]
D	.40 ± .10 [Typ.]	.016 ± .004 [Typ.]
E	.010 min.	.004 min.
F	3.00 max.	.118 max.
G	2.80 ± .13	.110 ± .005
H	16.04 ± .30	.631 ± .012
I	12.60	.496
J	1.72	.068
K	.15 ± .10 [Typ.]	.006 ± .004 [Typ.]
L	.80 ± .20	.031 ± .008

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



REVISION HISTORY

Revision	Description	Page	Date
0.2	Device codes are revised to 00D9H/00DFH compatible with AMD's		JUN/29/1998
0.3	The feature of sector unprotect is revised to chip unprotect		JUL/07/1998
0.4	Device ID codes are re-arranged as D9H/DFH for byte mode and 22D9H/22DFH for word mode.		JUL/10/1998
0.5	Sector Protect Verification is added on the software command table.		JUL/30/1998
0.6	Modify the chart of AUTOMATIC BLOCK ERASE TIMING WAVEFORM		AUG/18/1998
0.7	Modify the block diagram		AUG/24/1998
0.8	Modify the Q3 status into "0" for Exceeded Time Limits in Write Operation Status table	P9	SEP/11/1998
0.9	Modify Block Structure Table	P3	OCT/20/1998
0.9.1	Modify "Automatic Block Erase Algo. Flowchart"	P25	OCT/27/1998
	Modify "Sector Protection Algo. For System With 12V"	P28	
0.9.2	Insert the Temporary sector unprotected section & the Temporary sector unprotect operation after the data protection section	P14	NOV/09/1998
	Change IOH value at DC CHARACTERISTICS	P16	
	Change resistance value at SWITCHING TEST CIRCUITS	P19	
0.9.3	Correct typing error	P29,30, P32,33	DEC/09/1998
0.9.4	1)Insert the 45/55ns section	P1,17,18 P19,20,35	JAN/22/1999
	2)Correct Typing Error	P5,8,31	
	3)Modify "Write operation status" Erase suspended Mode Q3 Value from "0" to "1"	P11	
	4)Modify "AC CHARACTERISTICS" tOES value from "50" to "0"	P20,21	
	5)Modify Timing Waveform	P24,26,28	
0.9.5	1)Remove 45ns speed grade	P1,21,22,38	FEB/04/1999
	2)VCC range of 55ns:5V±5% --> 5V±10%	P17,18,19	

MACRONIX INTERNATIONAL CO., LTD.

HEADQUARTERS:
TEL:+886-3-578-8888
FAX:+886-3-578-8887

EUROPE OFFICE:
TEL:+32-2-456-8020
FAX:+32-2-456-8021

JAPAN OFFICE:
TEL:+81-44-246-9100
FAX:+81-44-246-9105

SINGAPORE OFFICE:
TEL:+65-747-2309
FAX:+65-748-4090

TAIPEI OFFICE:
TEL:+886-3-509-3300
FAX:+886-3-509-2200

MACRONIX AMERICA, INC.

TEL:+1-408-453-8088
FAX:+1-408-453-8488

CHICAGO OFFICE:
TEL:+1-847-963-1900
FAX:+1-847-963-1909

http : //www.macronix.com