MN195007

Hardware Specifications

Ver.1.0

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Panasonic Communications Co., Ltd.

This document presents hardware specifications of the MN195007. For information about the middleware that can be installed and its interfaces, refer to the relevant interface specifications.

- Contents -

1. Overview

1.1 Overview

The MN195007 is a 16-bit fixed-point DSP that implements high-speed signal processing. A DSP core, program memory, and work memory assembled on-chip can be combined with an analog front end (AFE) device to build a modem. The MN195007 is integrated 1 chip Digital Signal Processing LSI for FAX modem, Data modem and Voice control and it is suitable as a built-in modem solution.

The V.34 FAX and Voice modem LSI MN195006 is the similar pin layout with the MN195007, so the MN195006 can be replaceable to the MN195007 with minor design change.

1.2 Features

(1) General

- Machine cycle 15.26 ns
- Standard input clock frequency 24.576MHz
- Internal operation clock frequency 65.536MHz
- Operable from a single +3.3V power supply
  Internal logic +1.8V operation (The internal regulator generates+1.8V.)
- 100-pin QFP package (0.5mm pitch, 14mm×14mm)
- Low power consumption mode
- Program ROM 768KB Internal
- Data RAM 64KB Internal
- Operation Mode (3 Modes)
  - DSP mode (MN195006 compatible mode)
  - Serial interface mode
  - Parallel interface mode

(2) DSP core

- Parallel execution (CPU bus memory access, internal dual memory access, pointer change and AND/OR operations executable in a single instruction cycle)
- Hardware multi-loop function
- Eight data memory pointer registers

(3) Host interface

- Physical interface: Dual Port RAM(DPRAM) 1k × 16-bit
- Logical interface: Type 3 interface registers

(4) Dual-channel AFE interface

- Four different interface modes supported
  - 16-bit serial interface
  - 8-bit PCM (μ-Law and A-Law CODEC)
  - 4-bit ADPCM
  - Time-division multiplex serial bus (IOM2)

(5) Key features of each operation mode

a) DSP mode

Supplied various kind of middleware for modem and voice processing

Operation	Support features
FAX Modem	V.34, V.17, V.29, V.27ter, V.23
DATA Modem	V.90, V.34, V.32bis, V.22bis
Voice Processing	Codec : MPC, G.711, G.726 (16,24,32kbps) Digital Echo Canceller Voice multipath Signal detection

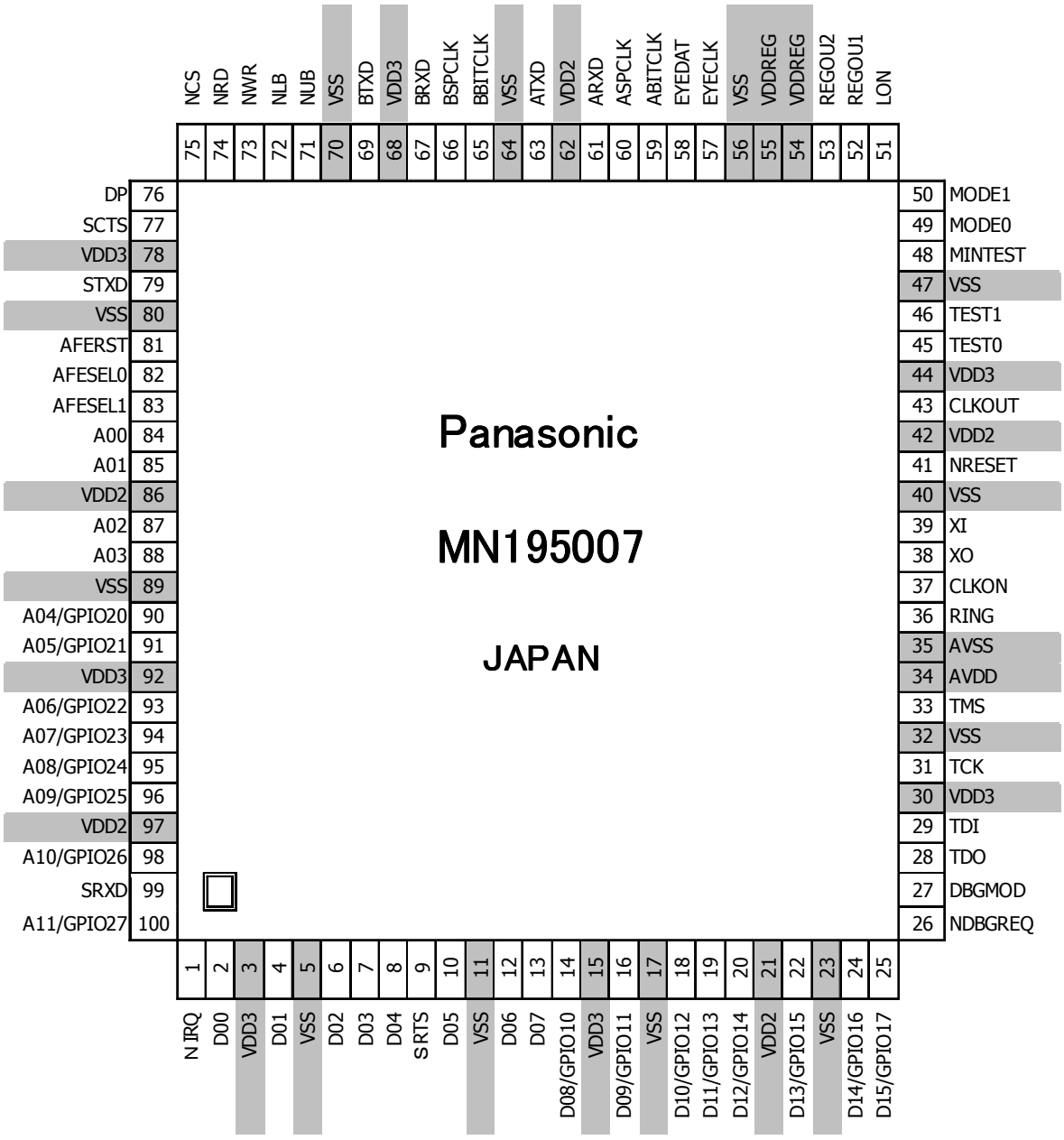
b) Serial Interface mode / Parallel Interface mode

Realize AT command modem with 1 chip

Item	Specifications	
Operation Mode	Serial Interface Mode	Parallel Interface Mode
Applicable Line	Public Service Telephone Line	
Network Operation Method	Recommended NCU : AA / MA / AM / MM	
Number of Line	1 channel	
Dialing Method	BP(DTMF) / DP(10pps,20pps)	
Communication Method	Data modem : Full Duplex Method Fax modem : Half Duplex Method	
Communication Speed	Data : V.22, V.22bis, V.32, V.32bis, V.34, V.90 Fax : V.27ter, V.29, V.17	
Error Correction	MNP Class 2,3,4 / V.42	
Data Compression	MNP Class 5 / V.42bis	
Control Command	Data : AT command compatible Fax : EIA-578(Class1)	
System interface	Standard Serial Interface	16550 Compatible Interface
Data Transfer Speed	460,800bps (max.)	----------
Data Format	Automatic Configuration Function	----------

2. Pin

2.1 Pin Layout



[Figure 1] Pin Layout

2.2 Pin List

2.2.1 Unique Pins

<table>
<tr><th>Signal Name</th><th>Pin #</th><th>I/O</th><th>Functions</th><th>Condition when reset</th></tr>
<tr><td>XI</td><td>39</td><td>I</td><td>X'tal in (24.576MHz)</td><td>---</td></tr>
<tr><td>XO</td><td>38</td><td>O</td><td>X'tal out (24.576MHz)</td><td>---</td></tr>
<tr><td>CLKOUT</td><td>43</td><td>O</td><td>24.576MHz Output</td><td>---</td></tr>
<tr><td>CLKON</td><td>37</td><td>I</td><td>Clock ON/OFF control</td><td>---</td></tr>
<tr><td>LON</td><td>51</td><td>I</td><td>Internal regulator control</td><td>---</td></tr>
<tr><td>TEST0</td><td>45</td><td>I</td><td rowspan="3">Test terminal (“L” during normal operation)
Pull-down resistor is integrated when MINTEST.</td><td rowspan="3">---</td></tr>
<tr><td>TEST1</td><td>46</td><td>I</td></tr>
<tr><td>MINTEST</td><td>48</td><td>I</td></tr>
<tr><td>MODE1</td><td>50</td><td>I</td><td rowspan="2">Mode setting terminal
<table><tr><th>MODE 1</th><th>MODE 0</th><th>Operation Mode</th></tr><tr><td>0</td><td>0</td><td>DSP</td></tr><tr><td>0</td><td>1</td><td>Parallel</td></tr><tr><td>1</td><td>0</td><td>Serial</td></tr></table></td><td>---</td></tr>
<tr><td>MODE0</td><td>49</td><td>I</td><td>---</td></tr>
<tr><td>NRESET</td><td>41</td><td>I</td><td>Reset Input</td><td>---</td></tr>
<tr><td>EYECLK</td><td>57</td><td>O</td><td rowspan="2">Eye Pattern monitor connect terminal</td><td>L</td></tr>
<tr><td>EYEDAT</td><td>58</td><td>O</td><td>L</td></tr>
<tr><td>ABITCLK</td><td>59</td><td>B</td><td>A channel AFE bit clock</td><td>Z</td></tr>
<tr><td>ASPCLK</td><td>60</td><td>B</td><td>A channel AFE Sample clock</td><td>Z</td></tr>
<tr><td>ATXD</td><td>63</td><td>O</td><td>A channel AFE transmit data</td><td>Z</td></tr>
<tr><td>ARXD</td><td>61</td><td>I</td><td>A channel AFE receive data</td><td>---</td></tr>
<tr><td>BBITCLK</td><td>65</td><td>B</td><td>B channel AFE bit clock</td><td>Z</td></tr>
<tr><td>BSPCLK</td><td>66</td><td>B</td><td>B channel AFE Sample clock</td><td>Z</td></tr>
<tr><td>BTXD</td><td>69</td><td>O</td><td>B channel AFE transmit data</td><td>Z</td></tr>
<tr><td>BRXD</td><td>67</td><td>I</td><td>B channel AFE receive data</td><td>---</td></tr>
<tr><td>NDBGREQ</td><td>26</td><td>I</td><td rowspan="6">Terminal for ICE
During normal operation;
TMS, NDBGREQ is “H”
TCK, TCI is “L”
DBGMOD, TDO is “Open”</td><td>---</td></tr>
<tr><td>DBGMOD</td><td>27</td><td>O</td><td>L</td></tr>
<tr><td>TMS</td><td>33</td><td>I</td><td>---</td></tr>
<tr><td>TCK</td><td>31</td><td>I</td><td>---</td></tr>
<tr><td>TDI</td><td>29</td><td>I</td><td>---</td></tr>
<tr><td>TDO</td><td>28</td><td>O</td><td>Z</td></tr>
<tr><td>RING</td><td>36</td><td>I</td><td>Ring-pass input</td><td>---</td></tr>
<tr><td>DP</td><td>76</td><td>O</td><td>Dial calling pulse output</td><td>H</td></tr>
<tr><td>SRTS</td><td>9</td><td>I</td><td>Serial transmit request
(PC -> MN195007)</td><td>Z</td></tr>
<tr><td>SRXD</td><td>99</td><td>I</td><td>Serial receive data (PC -> MN195007)</td><td>Z</td></tr>
<tr><td>SCTS</td><td>77</td><td>O</td><td>Serial transmit permission
(PC <- MN195007)</td><td>H</td></tr>
<tr><td>STXD</td><td>79</td><td>O</td><td>Serial transmit data (PC <- MN195007)</td><td>H</td></tr>
<tr><td>AFERST</td><td>81</td><td>O</td><td>AFE reset signal</td><td>L</td></tr>
<tr><td>AFESEL0</td><td>82</td><td>I</td><td>AFE type signal 0</td><td>---</td></tr>
<tr><td>AFESEL1</td><td>83</td><td>I</td><td>AFE type signal 1</td><td>---</td></tr>
</table>

[Table 1] Unique Pin List

2.2.2 Common Pins

Signal Name	Pin #	Condition when reset	DSP Mode		Serial Mode		Parallel Mode	
			Signal	I/O	Signal	I/O	Signal	I/O
nUB	71	Z	NUB	I	H	O	RXRDY	O
nLB	72	Z	NLB	I	H	O	TXRDY	O
nWR	73	Z	NWR	I	H	O	NWR	I
nRD	74	Z	NRD	I	H	O	NRD	I
nCS	75	Z	NCS	I	H	O	NCS	I
nIRQ	1	Z	NIRQ	O	H	O	IRQ	O
D00	2	Z	D00	B	Ci	O	D00	B
D01	4	Z	D01	B	DTR	I	D01	B
D02	6	Z	D02	B	DSR	O	D02	B
D03	7	Z	D03	B	DCD	O	D03	B
D04	8	Z	D04	B	L	O	D04	B
D05	10	Z	D05	B	L	O	D05	B
D06	12	Z	D06	B	L	O	D06	B
D07	13	Z	D07	B	L	O	D07	B
D08	14	Z	D08	B	GPIO10	B	GPIO10	B
D09	16	Z	D09	B	GPIO11	B	GPIO11	B
D10	18	Z	D10	B	GPIO12	B	GPIO12	B
D11	19	Z	D11	B	GPIO13	B	GPIO13	B
D12	20	Z	D12	B	GPIO14	B	GPIO14	B
D13	22	Z	D13	B	GPIO15	B	GPIO15	B
D14	24	Z	D14	B	GPIO16	B	GPIO16	B
D15	25	Z	D15	B	GPIO17	B	GPIO17	B
A00	84	---	A00	I	---	I	A00	I
A01	85	Z	A01	I	L	O	A01	I
A02	87	Z	A02	I	L	O	A02	I
A03	88	Z	A03	I	L	O	L	O
A04	90	Z	A04	I	GPIO20	B	GPIO20	B
A05	91	Z	A05	I	GPIO21	B	GPIO21	B
A06	93	Z	A06	I	GPIO22	B	GPIO22	B
A07	94	Z	A07	I	GPIO23	B	GPIO23	B
A08	95	Z	A08	I	GPIO24	B	GPIO24	B
A09	96	Z	A09	I	GPIO25	B	GPIO25	B
A10	98	Z	A10	I	GPIO26	B	GPIO26	B
A11	100	Z	A11	I	GPIO27	B	GPIO27	B

[Table 2] Common Pin List

2.2.3 Power / Ground Pins

Signal Name	Functions	I/O	Pin #
VDD3	+3.3V Power (For I/O)	I	3,15,30,44,68,78,92
VDDREG	+3.3V Power (For internal regulator)	I	54,55
REGOUT	Regulator Output (+1.8V)	O	52,53
VDD2	+1.8V Power (For internal logic)	I	21,42,62,86,97
VSS	VSS for I/O, internal logic (Common)	I	5,11,17,23,32,40,47,56, 64,70,80,89
AVDD	Analog Power (3.3V) for PLL	I	34
AVSS	Analog Power (VSS) for PLL	I	35

[Table 3] Power / Ground Pin List

On each tables, I/O code indicates as follows;

I: Input
O: Output
B: Bidirectional (Direction determined by setting)
Z: High impedance

2.3 Pin Definitions

2.3.1 Unique Pin

a) XI, XO

Connect a 24.576 MHz crystal resonator.
Use a crystal resonator only with its frequency deviations not exceeding $\pm 50 \times 10^{-6}$ (with aging and temperature changes included).

When using a crystal oscillator, apply a signal to XI, leaving XO open.

Duty ratio:	40% to 60%
Frequency deviation:	Not exceeding $\pm 50 \times 10^{-6}$ (with aging and temperature changes included)

b) CLKOUT

Buffered output of the signal input from a quartz resonator or quartz oscillator.
Use CLKOUT as an AFE clock.
Output clock signal during reset.

c) LON

Test pin.
Set "High" set on this pin during normal operations.

d) CKON

Oscillation operation control and internal PLL control pin when a quartz resonator oscillator is used.
"High" starts oscillation, and "Low" stops oscillation.
Keep "High" set on this pin during normal operations.

e) MINTEST, TEST1, TEST2

Test pins
Keep "Low" set on these pins during normal operations.

f) Mode [1:0]

Operation mode select pins

Mode [1]	Mode [2]	Operation Mode
0	0	DSP Mode
0	1	Parallel i/f Mode
1	0	Serial i/f Mode
1	1	Not used (inhibit)

[Table 4] Operation Mode List

g) NRESET

Reset pin
"Low" on NRESET enables a reset; "High" cancels the reset.
On a reset, the internal clock shuts down, saving the current drain.

A reset takes effect in a minimum "Low" period of 100 ns while the power input and the CLKON pin are stable. Internal circuitry stabilizes 50 ms after the reset is canceled, getting the modem operation started.

h) EYECLK, EYEDAT
Eye pattern monitor connection pins

i) ABITCLK, BBITCLK Serial data clocks
ASPCLK, BSPCLK Serial data synchronization signals
ATXD, BTXD Transmitted serial data (MN195007 => AFE direction)
ARXD, BRXD Received serial data (MN195007 => AFE direction)

These AFE interface pins are divided into two channels: A and B.
The first letter (A or B) heading each signal name identifies the channel name.

The pin direction switches according to the AFE type set by GPIO [4] and [5].

AFE Type	ABITCLK BBITCLK	ASPCLK BSPCLK	ATXD BTXD	ARXD BRXD
STLC7550 slave mode	Input	Output	Output	Input
STLC7550 master mode	Input	Input	Output	Input
Digital interface	Input	Input	Output	Input
Si3044	Input	Input	Output	Input
Free pin handling	Pull-up	Pull-up	Pull-down	Pull-up

[Table 5] AFE Interface Signal Directions

Note: If a pin is out of use, be sure to carry out free pin handling as specified in [Table 5]. Because ATXD and BTXD enter a high-impedance state when the output pin is reset, be sure to pull them down to finalize the level.

j) AFESEL[0], AFSEL[1]
AFE type selection pins
Set pins depend of connecting AFE type as shown in [Table 6]

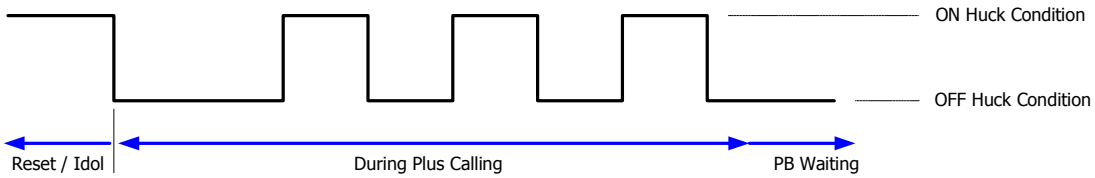
AFESEL [0]	AFESEL [1]	AFE Type
0	0	STLC7550 Slave Mode
0	1	STLC7550 Master Mode RLC5T882 Master Mode RL5T884 Master Mode
1	0	Digital i/f Mode
1	1	Si3044 Master Mode

* Ricoh AFE IC (RTL5T882 and RL5T884) is only supported with master mode.

[Table 6] AFE Type Bit Assignment

k) DP
Dialing pulse Output pin
The default is a high

(i.e.) When dialing "3"



* Please refer "MMD-5005 Modem Type 3 interface D-Mode Specifications" for more details

l) Ring
Ringing pulse input pin for ring detection
Apply a ringing signal at the +3.3V logic level.
Calculates the period between rising or falling edges of an input pulse.
* Please refer "MMD-5005 Modem Type 3 interface D-Mode Specifications" for more details

m) AFERST
AFE reset signal.
Output "Low" signal during Reset (NRESET signal is "Low")

n) VDD3
+3.3V power pin
Supply +3.3V from an external source.

o) VDDREG
Internal regulator (+1.8V output) power pin
Supply +3.3V.

p) VREGOUT1, REGOUT2
Internal regulator voltage (+1.8V) output pins
Have a capacitor rated at 4.7µF or higher inserted between these pins and VSS to stabilize the regulator.
Wire this pin to VDD2.

q) VDD2
+1.8V power input pin. (Power supplied to internal logic operation from +1.8V)
Wire VDD2 to REGOUT and have a capacitor inserted between VDD2 and VSS.

r) VSS
GND pin.
There is no distinction between +3.3V power and +1.8V power VSSs.

s) AVDD
PLL block power pin
Supply +3.3V. There is no need to distinguish AVDD from VDD3 and VDDREG.

t) AVSS
PLL block GND pin
There is no need to distinguish AVSS from VSS

u) SCTS, SRTS, STXD, SRXD
Signal lines for standard serial interface.
All pins are negative logic.
Possible to use DSP mode and Serial mode.

If these pins are not used or use parallel mode, please set as follows;
SRXD, SRTS : Pull-up (Possible to connect VDD)
STXD, SCTS : Open

EIA-232-E asynchronous communication is possible to use these 4 lines.
SCTS : Transmit acceptance information to DTE (to DTE from MN195007)
SRTS : Transmit request from DTE (from DTE to MN195007)
STXD : Transmit data to DTE (to DTE from MN195007)
SRXD : Receiving data from DTE (from DTE to MN195007)

v) NDBGREQ, DBGMOD, TMS, TCK, TDI, TDO
Test pins
Keep followings set on these pins during normal operations.

NDBGREQ, TMS pins : "High"
TCK, TDI pins : "Low"
DBGMOD, TDO pins : "Open"

2.3.2 Common Pins

2.3.2.1 DSP Mode

a) NUB, NLB
Host CPU interface signals
NUB indicates that the upper-order side of the data line is valid.
NLB indicates that the lower-order side of the data line is valid.
Valid only on write; active "Low".

b) NWR
Host CPU interface signal
Write pulse
Active "Low".

c) NRD
Host CPU interface signal
Read pulse
Active "Low".

d) NCS
Host CPU interface signal
Chip Select
Active "Low".

e) NCQ
Host CPU interface signal
Interrupt output
"Low" on this level interrupt indicates that the interrupt is enabled.
A pull-up resistance is required.

f) D [15:0]
Host CPU interface signal
Data I/O

g) A [11:0]
Host CPU interface signal
Address Input

2.3.2.2 Parallel Interface Mode

Host interface by 8 bit data bus, communicate through UART (Universal Asynchronous Receiver / Transmitter) IC16550 common resistor.

a) NWR
Host CPU interface signal
Write pulse
Active "Low".

b) NRD
Host CPU interface signal
Read pulse
Active "Low".

c) NCS
Host CPU interface signal
Chip Select
Active "Low".

d) IRQ
Host CPU interface signal
Interrupt output
"Low" on this level interrupt indicates that the interrupt is enabled.
A pull-up resistance is required.

e) D[7:0]
Host CPU interface signal
Data input/Output

f) A[2:0]
Host CPU interface signal
Address input

g) RXRDY
Become "Active" when receive the data
Active "Low".

h) TXRDY
Become "Active" when no transmit data in internal buffer
Active "Low".

i) GPIP[10:17], GPIO[20:27]
I/O port
Pin functions are set by the kind of software that is installed and are not user-programmable.

<table>
<tr><th>Pin No.</th><th>Function</th><th>Description</th><th>I/O</th><th>Pin Handling</th></tr>
<tr><td>GPIO[20]</td><td>SP0</td><td rowspan="6">Speaker Control Pins
<table><tr><th>Output</th><th>SP1</th><th>SP0</th></tr><tr><td>Mute</td><td>0</td><td>0</td></tr><tr><td>Min</td><td>0</td><td>1</td></tr><tr><td>Mid</td><td>1</td><td>0</td></tr><tr><td>Max</td><td>1</td><td>1</td></tr></table></td><td>Out</td><td rowspan="2">Pull-up individually whichever these pins are used or not</td></tr>
<tr><td>[21]</td><td>SP1</td><td>Out</td></tr>
<tr><td>[22]</td><td>---</td><td>---</td><td>In</td><td rowspan="2">Pull-up or connect VDD</td></tr>
<tr><td>[23]</td><td>---</td><td>---</td><td>In</td></tr>
<tr><td>[24]</td><td>SK</td><td>E2PROM Serial Clock IN</td><td>In</td><td rowspan="2">Using : Pull-up individually
Not Using : Pull-up or connect VDD</td></tr>
<tr><td>[25]</td><td>CS</td><td>E2PROM Chip Select IN</td><td>In</td></tr>
<tr><td>[26]</td><td>DI</td><td>E2PROM Serial Data IN</td><td>In</td><td rowspan="2">Pull-up individually whichever these pins are used or not</td></tr>
<tr><td>[27]</td><td>DO</td><td>E”PROM Serial Data OUT</td><td>Out</td></tr>
<tr><td>GPIO[10:17]</td><td>---</td><td>---</td><td>In</td><td>Pull-up or connect VDD</td></tr>
</table>

[Table 7] GPIO Port Assignment

Note :
In case not using these pins, keep “Ping handling” condition set on these pins as mentioned [table 7]
SP0, SP1, and DO pins are output pin but they become “high Impedance” condition during “RESET”, so pull-down handling is required to set the proper level.
Non using terminal is possible to connect VDD directly.
Connectable E2PROM is “FM93C86A” produced by Firechild

2.3.2.3 Serial Interface Mode

a) CI, DTR, DSR, DCD
Signal lines for standard serial interface.
All pins are negative logic.

EIA-232-E asynchronous communication is possible to use these 4 lines together with other 4 specifically assigned pins “SCTS, SRTS, STXD, and SRXD”.

CI : Call signal detect information to DTE (to DTE from MN195007)
DTR : Transmit acceptance information from DTE (from DTE to MN195007)
DSR : Transmit acceptance information to DTE (to DTE from MN195007)
DCD : Carrier detect information to DTE (to DTE from MN195007)

b) GPIP[10:17], GPIO[20:27]
I/O port

Same function as Parallel Interface Mode. Please refer to [Table 7] for mode details.

3. Electric Characteristics

3.1 Absolute Maximum Rating Specifications

VSS=0V

Item	Symbol	Rating Specification	Unit
External Power Voltage *1	V_{DD}	-0.3 ~ +4.6	V
Internal Power Voltage *1	V_{DDI}	-0.3 ~ +2.5	V
Input Pin Voltage	V_I	-0.3 ~ V_{DD} + 0.3 (Max.4.6)	V
Output Pin Voltage	V_O	-0.3 ~ V_{DD} + 0.3 (Max.4.6)	V
Output Current (TYPE-HL4) *2	I_O	+/- 12	mA
Power input current	I_V	+/- 70 (each pin)	mA
Acceptable Power Loss	P_D	520	mW
Operation temperature	T_{opr}	0 ~ 70	ºC
Storage Temperature	T_{stg}	-55 ~ 150	ºC

[Table 8]

*1 : In case V_{DD} or V_{DDI} is not supplied (OFF), output may be unstable condition. There is no specified sequence for power ON or power OFF. We recommend to power on for both V_{DD} and V_{DDI} at same time.

*2 : Name of TYPE-HL4 pins ;
NIRQ, A[01:11], D[00:15], NLB, NUB, NCS, NRD, NWR, DP, SCTS, SRTS, SRXD, STXD, ATXD, BTXD, ASPCLK, BSPCLK, ABITCLK, BBITCLK, AFERST, AFESEL[0:1], CLKOUT, DBGMOD, TDO, EYECLK, EYEDAT, REGOUT[1:2]

Note : Absolute Maximum Rating Specifications is limit values which do not exceed at any conditions (it may cause the damage or become worse.) This specification values does not guarantee the operation.

3.2 Recommended Operation Conditions

Item	Symbol	Condition	Permissible Range			Unit
			Min	Standard	Max	
External Power Voltage	V_{DD}		3.14	3.3	3.46	V
Internal Power Voltage	V_{DDI}		1.71	1.8	1.89	V
Environmental Temperature	Ta		0		70	ºC
Input rising time	tr		0		100	ns
Input falling time	tf		0		100	ns
Oscillation Frequency	f_{OSC1}	24.576MHz X'tal		24.576		MHz
External recommended Capacity	CX_{IN} CX_{OUT}	V_{DD}=3.3V Implemented Feedback resistor		*Note		pF

Note : Oscillation characteristic should be determined with X'tal Supplier.

[Table 9]

3.3 Input / Output Capacity

Item	Symbol	Condition	Permissible Range			Unit
			Min	Standard	Max	
Input Pins	C_{IN}	$V_{DD} = V_{DDI} = V_I = 0V$ F = 1MHz Ta = 25ºC		7	8	pF
Output Pins	C_{OUT}			7	8	pF
Input/Output Pins	C_{IO}			7	8	pF

[Table 10]

3.4 DC Characteristics

Measurement conditions : V_{DD} = 3.14 ~ 3.46V, V_{DDI} = 1.71 ~ 1.89V, V_{SS} = 0.00V,
f_{TEST} = 66MHz, Ta = 0 ~ 70 degrees C

Item	Symbol	Condition	Permissible Range			Unit
			Min	Standard	Max	
Static Power Current	I_{DDS}	V_I (Pull-up) = OPEN V_I (Pull-down) = OPEN V_I(XI) = V_{DD} (*1) Other input pins and Hi-z condition of input/output pins should apply V_{SS} or V_{DD} level.			2 (*2)	mA
Operation Power Current	I_{DDO}	$V_I = V_{DD}$ or V_{SS} f = 66MHz V_{DD} = 3.3V V_{DDI} = 1.8V Release output			40	mA
Internal Power Operation Power Current	I_{DDIO}	$V_I = V_{DD}$ or V_{SS} f = 66MHz V_{DD} = 3.3V V_{DDI} = 1.8V Release output			100	mA

(*1) : Power supply for X'tal oscillator is used separate power supply for measuring I_{DDS}.
(*2) : Environmental temperature should be 25 ºC.

[Table 11]

Item	Symbol	Condition	Permissible Range			Unit
			Min	Standard	Max	
Oscillation Circuit : XO						
Internal feedback Resistor	R_{f7}	$V_I = V_{DD}$ or V_{SS} V_{DD} = 3.3V		1		MΩ

Input LVCMOS Level : A00, LON, TCK, TDI, TMS, ARXD, BRXD, MODE[0:1], CLKON, RING SRTS, SRXD, AFESEL[0:1], TEST0, TEST1, NRESET, NDBGREQ						
Input Voltage "High" Level	V_{IH}		V_{DD} X 0.7		V_{DD}	V
Input Voltage "Low" Level	V_{IL}		0		V_{DD} X 0.2	V
Input Leakage current	I_{LI}	$V_I = V_{DD}$ or V_{SS}			+/- 10	μA

Input LVCMOS Level (With Pull-down resistor) : MINTEST						
Input Voltage "High" Level	V_{IH}		V_{DD} X 0.7		V_{DD}	V
Input Voltage "Low" Level	V_{IL}		0		V_{DD} X 0.3	V
Pull-down Resistor	R_{IL}	$V_I = V_{DD}$	10	30	90	KΩ
Input Leakage current	I_{LI}	$V_I = V_{DD}$ or V_{SS}			+/- 10	μA

Input/Output LVCMOS Level : NIRQ, A[01:11], D[00:15], NLB, NUB, NCS, NRD, NWR, DP, SCTS, STXD, AFERST ATXD, BTXD, ASPCLK, BSPCLK, CLKOUT, DBGMOD, TDO, EYECLK, EYEDAT						
Input Voltage "High" Level	V_{IH}		V_{DD} X 0.7		V_{DD}	V
Input Voltage "Low" Level	V_{IL}		0		V_{DD} X 0.3	V
Output Voltage "High" Level	V_{OH}	I_{OH} = -4.0mA $V_I = V_{DD}$ or V_{SS}	V_{DD} X 0.8			V
Output Voltage "Low" Level	V_{OL}	I_{OL} = 4.0mA $V_I = V_{DD}$ or V_{SS}			V_{DD} X 0.2	V
Output Leakage Current	I_{LO}	V_O = Hi-Z Condition $V_I = V_{DD}$ or V_{SS} $V_O = V_{DD}$ or V_{SS}			+/-10	μA

[Table 12-1]

Item	Symbol	Condition	Permissible Range			Unit
			Min	Standard	Max	
Input/Output LVCMOS Level (with Summit) : ABITCLK, BBITCLK						
Input Voltage "High" Level	V_{IH}		V_{DD} X 0.8		V_{DD}	V
Input Voltage "Low" Level	V_{IL}		0		V_{DD} X 0.2	V
Output Voltage "High" Level	V_{OH}	I_{OH} = -4.0mA V_I = V_{DD} or V_{SS}	V_{DD} X 0.8			V
Output Voltage "Low" Level	V_{OL}	I_{OL} = 4.0mA V_I = V_{DD} or V_{SS}			V_{DD} X 0.2	V
Output Leakage Current	I_{LO}	V_O = Hi-Z Condition V_I = V_{DD} or V_{SS} V_O = V_{DD} or V_{SS}			+/-10	µA

[Table 12-2]

4. Power Consumption Control

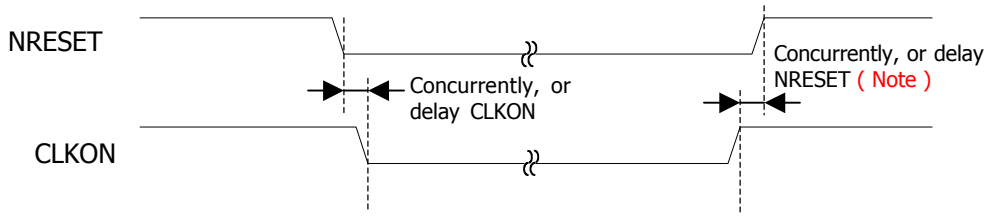
The table below lists the methods available for controlling power consumption.

No.	CLKON pin	NRESET pin	Status	Operable blocks
(A)	L	L	Power consumption due to internal logic leak current	All circuits shut down
(B)	H	L	Power consumption due to (A) , oscillator circuit and PLL circuit	Quartz oscillator circuit functioning Internal PLL VCO oscillating (PLL inoperable)
(C)	H	H	Normal operation	All circuits shut down

[Table 13] Power Consumption Control

Power consumption increases in the order of (A) -> (B) -> (C).
Internal PLL starts operation after reset of condition (C).
When PLL becomes stable after recovering RESET, reboot the modem operation.

A control timing chart is given in Figure 2.



Note : In case Crystal Oscillator is used, there is no problem to release NRSET and CLKON concurrently. However, in case Crystal resonator is used, NRESET should be released after stabilizing the oscillation circuit, otherwise wrong operation may occur due to CLKOUT signal is not stabilized. (Oscillation circuit may stabilize after several decades msec. Please confirm with parts supplier or actual unit)

[Figure 2] Power Consumption Control Timing

5. Serial Interface Section

Serial communication has been performed to Host CPU when DSP mode or Serial Mode has been selected.

On DSP mode, 4 signal lines (SRXD, STXD, SCTS and SRTS) assigned for serial communication pins can be used to perform standard serial communication. Normally 9 signal lines is assigned for modem control, but proper FAX/DATA modem operation can be performed by using these 4 signal lines.

On Serial mode, in addition to above 4 signal lines, other signal lines (CI, DTR DRS, and DCD) assigned for common communication pins can be used to perform EIA-232-E asynchronous communication.

*More details explanations for Serial Mode, please refer "6.2 Serial Interface Mode".

Main features for this "Serial Interface" are :

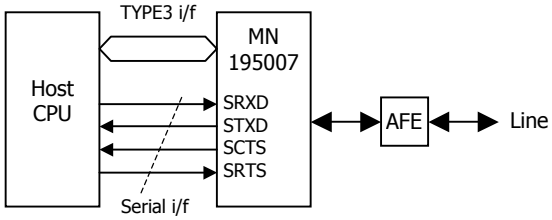
a) Support automatic configuration such as Automatic Speed Recognition, Automatic Format Recognition.
b) Support 2400bps ~ 460.8Kbps. (2400, 4800, 7200, 9600, 14.4K, 19.2K, 38.4K, 57.6K, 76.8K, 115.2K, 230.4K, 460.8K)
c) Implement 32K bytes FIFO for Transmitting/Receiving Data, so that automatic flow operation can be performed by FIFO condition.
d) Support EIA-232-E driver/receiver, so that PC's serial port can be connected.

The Serial communication of DSP Mode is shown following paragraphs

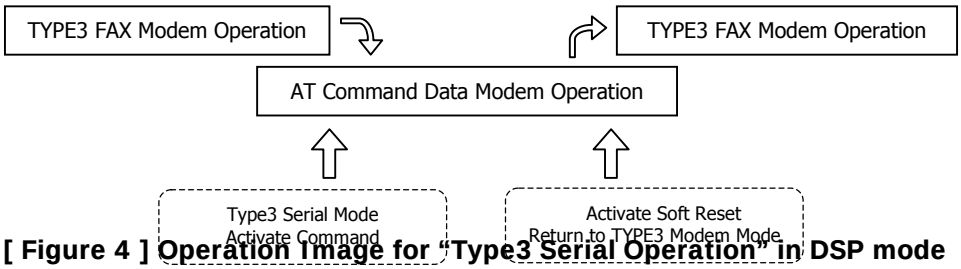
5.1 Type 3 Serial Operation

"Type3 Serial Operation" is performed Serial communication with DSP mode.
To use this "Type3 Serial Operation", set the mode selection pins to "DSP mode" and perform the "Type3 Serial Boot Command" from Host CPU, so that serial communication is performed even in DSP mode.
"Type3 Serial Operation" can be performed to switch "Type 3 command controlled FAX modem" and "AT command controlled DATA modem" without changing the hardware design.

Refer [Figure 3] for Block Diagram and [Figure 4] for Operation Image



[Figure 3] "Type3 Serial Operation" Connection Block Diagram in DSP Mode



[Figure 4] Operation Image for "Type3 Serial Operation" in DSP mode

5.2 Operatable Functions

Outline of operatable functions in each mode is mentioned in [Table 14].

In DSP mode, Type 3 command control (*) is used for modem operation. During this period, serial interface is not operatable. Also, "Error correction" and "Data Compression" functions such as V.42/V.42bis, MNP is not supported in Data communication.

Operatable Functions		DSP Mode	Serial Mode	Type3 Serial
DPRAM i/f		O	×	Δ
Serial i/f		×	O	●
FAX Communication		Type3 Command Control	Class1 Control	Class1 Control
DATA Communication	Correction/Compression	× (Implement in Host CPU)	O	O
	Control Command	× (Implement in Host CPU)	AT Command Control	AT Command Control

O : Operatable
● : Not support for DSR and DTR (Limited with AT Command)
Δ : Possible for parameter setting
×: Impossible

[Table 14] Operatable Functions in each mode

5.3 Usage for Type 3 Serial Mode

For FAX communication, the detail parameter setting is required and Type 3 command control is suitable to use. Also, for DATA communication, AT command control is popular to use. Therefore, it is the best suited for both FAX and DATA communication by connecting MN195007 to Host CPU with DSP mode and operating with Type 3 serial mode.

6. Function Explanation in each Mode

6.1 DSP Mode

6.1.1 Dual Port Memory Brock

Physical interface between Host CPU, is used 2Kbytes dual port memory (DPRAM) and both 16 and 8 bit access is available.

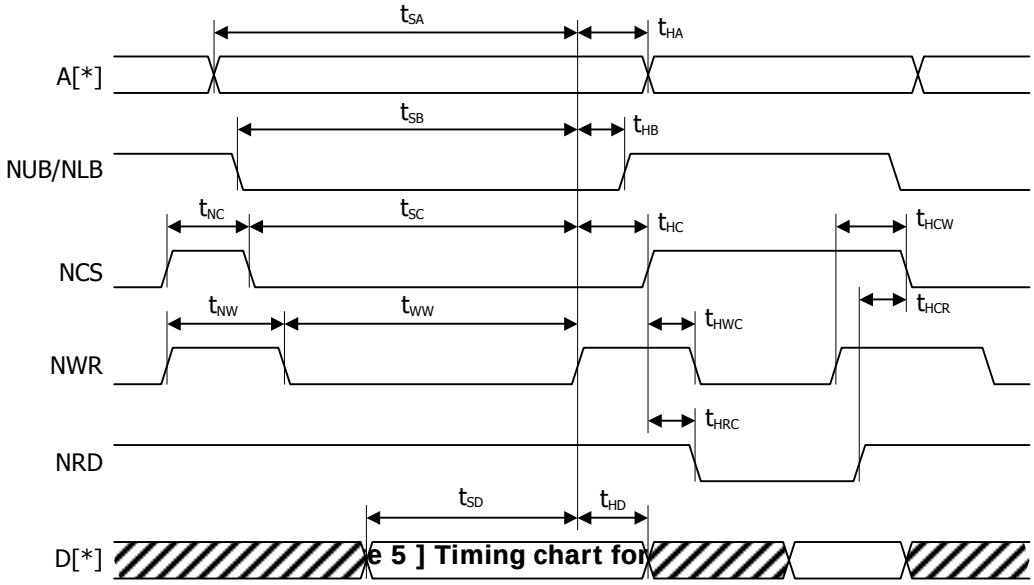
6.1.1.1 Access Timing

Assess timing is mentioned in [Figure 6] and [Figure 7].
It is the common timing to access DPRAM and Type 3 interface register (Refer to "6.1.2 Type 3 Interface Register")

Item	Symbol	Normal timing		If NDPWR is delayed after NUB, NLB		Unit
		Min	Max	Min	Max	
DPA set-up	t_{SA}	30		40		ns
DPA Hold	t_{HA}	0		-10		ns
DPD Set-up	t_{SD}	30		40		ns
DPD Hold	t_{HD}	0		-10		ns
NDPCS Set-up	t_{SC}	30		40		ns
NDPCS Hold	t_{HC}	0		-10		ns
NUB, NLB Set-up	t_{SB}	30		40		ns
NUB, NLB Hold	t_{HB}	0		-10		ns
NDPCS Negation Period	t_{NC}	20		20		ns
NDPWR Hold during NDPCS Negation	t_{HWC}	3		3		ns
NDPRD Hold during NDPCS Negation	t_{HRC}	3		3		ns
NDPWR Pulse Width	t_{WW}	40		40		ns
NDPWR Negation Period	t_{NW}	20		20		ns
NDPCS Hold during NDPWR Negation	t_{HCW}	3		3		ns
NDPRD Pulse Width	t_{WR}	100		100		ns
NDPCS Hold during NDPRD Negation	t_{HCW}	3		3		ns
NDPRD Negation Period	t_{NR}	20		20		ns
NDPRD Access Time	t_{AR}		100		100	ns
DPA Access Time	t_{AA}		100		100	ns
NDPCS Access Time	t_{AC}		100		100	ns
NUB, NLB Access Time	t_{AB}		100		100	ns
DPD Output Hold Time	t_{HRD}	5		5		ns

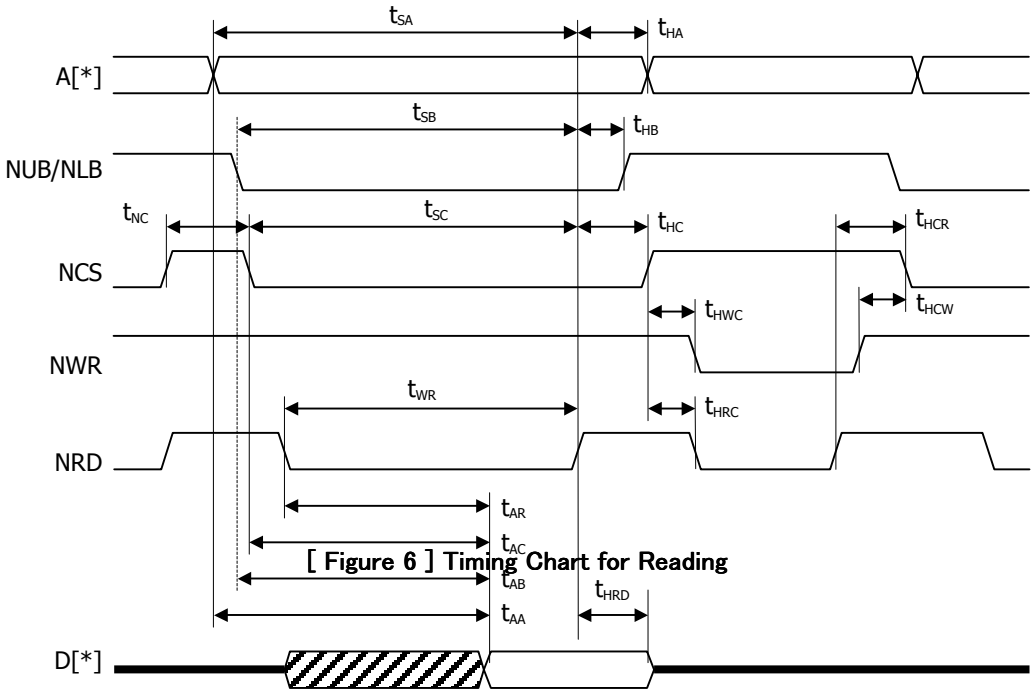
[Table 15] DPRAM Access Time

6.1.1.1 Write Timing



[Figure 5] Timing chart for

6.1.1.3 Read Timing



[Figure 6] Timing Chart for Reading

6.1.2 Type 3 Interface register

Type 3 interface register is a physical interface between Host CPU and modem program. These registers constructed with 15 lines of 8 bit register and are connected with odd addresses.

Register map is mentioned in [Table 16].

Address	Register Name	R/W	Description
000 | 7FF	DPRAM Area	---	
800	RXDR	R	Receive Data Register
802	TXDR	R/W	Transmit Data Register
804	CMDR1	R/W	Command Register 1
806	CMDR2	R/W	Command Register 2
808	STSR1	R	Status Register 1
80A	EGSL1	R/W	Interrupt Edge Control Register for Status Register 1
80C	T3IRQ1EN	R/W	Interrupt Control Register for Status Register 1
80E	T3IRQ1DET	R/W	Interrupt Accept Register for Status Register 1
810	STSR2	R	Status Register 2
814	T3IRQ2EN	R/W	Interrupt Control Register for Status Register 2
816	T3IRQ2DET	R	Interrupt Accept Register for Status Register 2
818	STSR3	R	Status Register 3
81A	EGSL3	R/W	Interrupt Edge Control Register for Status Register 3
81C	T3IRQ3EN	R/W	Interrupt Control Register for Status Register 3
81E	T3IRQ3DET	R/W	Interrupt Accept Register for Status Register 3

[Table 16] Type 3 interface Register Map

6.2 Serial Interface Mode

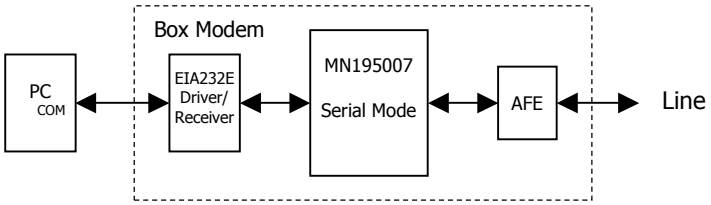
The EIA-232-E asynchronous Serial Interface is supported to use 4 dedicated signal lines (SRXD, STXD, SCTS and SRTS) and 4 common signal lines (CI, DTR DRS, and DCD).

The Box modem for connect with the Serial port of PC, can be created to connect with the EIA-232-E Driver/Receiver IC as shown in [Figure 7]. Also, embedded serial modem can be created to connect with serial port of Host CPU as shown in [Figure 8].

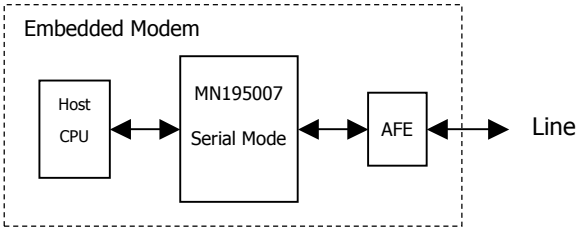
* Not supported for voice processing function

[Features]

a) Support automatic configuration such as Automatic Speed Recognition, Automatic Format Recognition.
b) Support 2400bps ~ 460.8Kbps. (2400, 4800, 7200, 9600, 14.4K, 19.2K, 38.4K, 57.6K, 76.8K, 115.2K, 230.4K, 460.8K)
c) Implement 32K bytes FIFO for Transmitting/Receiving Data, so that automatic flow operation can be performed by FIFO condition.



[Table 7] Box Modem Block Diagram



[Table 8] Embedded Modem Block Diagram

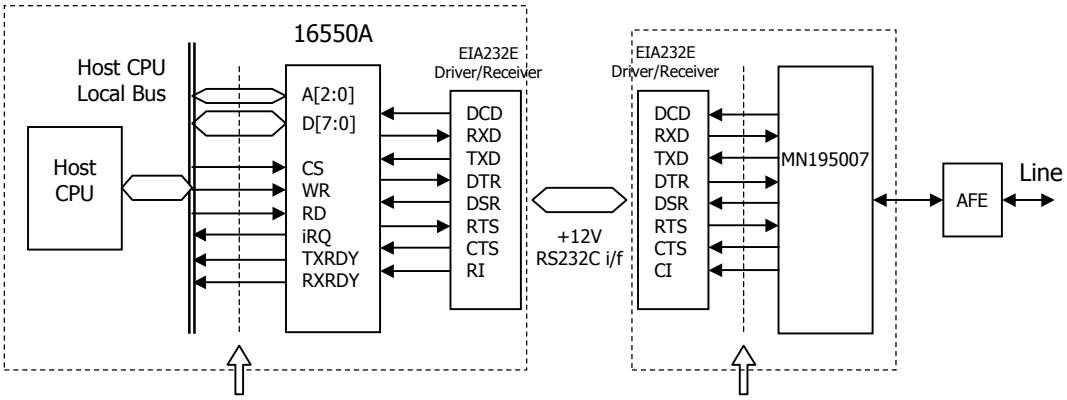
* Refer " MN195007 AT Command Specifications" for mode details of AT command.

6.3 Parallel Interface Mode

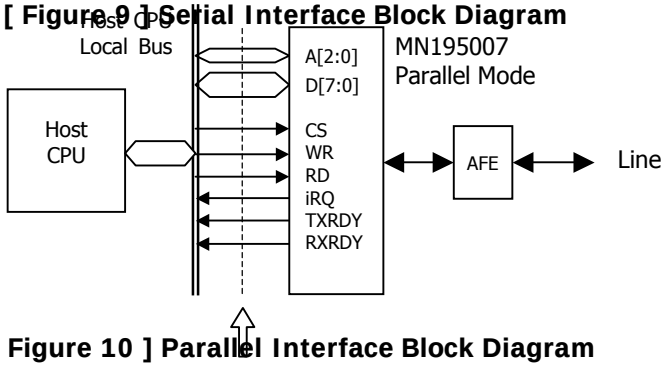
MN195997 is implemented 16550A common register with is used as PC standard serial interface. Parallel Interface mode is bus connection interface by using these registers.

The reference serial interface block diagram is shown in [Figure 9].
The local bus of Host CPU is connected common asynchronous receiver/transmitter 16550A which is converted from parallel data to serial data, and connected to EIA232E Driver/receiver. MN195997 is connected via EIA232E Driver/Receiver and communicates to Host CPU with Serial communication. The interface point of MN195007 Serial mode is shown in [Figure 9] a).

For the connection of Parallel interface, interface point with Host CPU is shown in [Figure 9] b) and connection diagram is shown in [Figure 10]. Host CPU can be access directly to MN195007 16550 compatible register, so efficient AT command modem can be created without any speed limitation like as the serial interface.
* Not supported for voice processing function



[Figure 9] Serial Interface Block Diagram

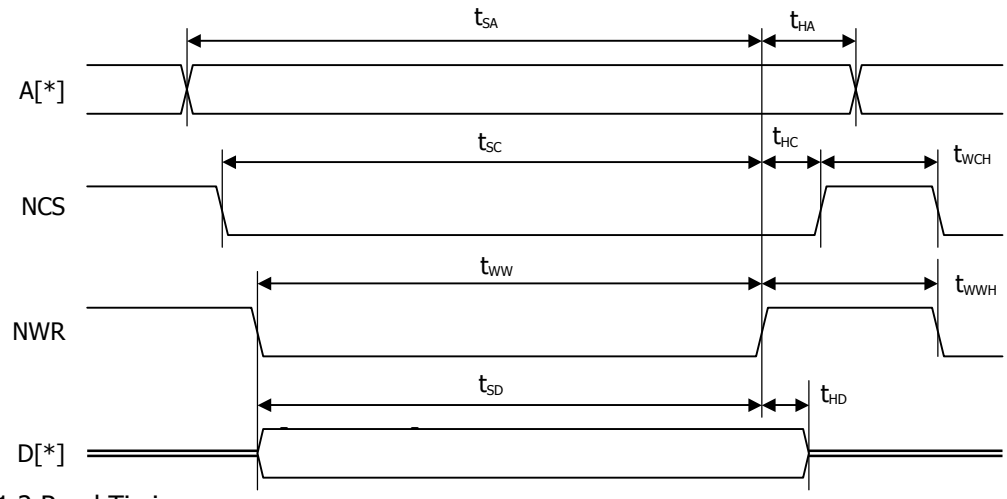


[Figure 10] Parallel Interface Block Diagram

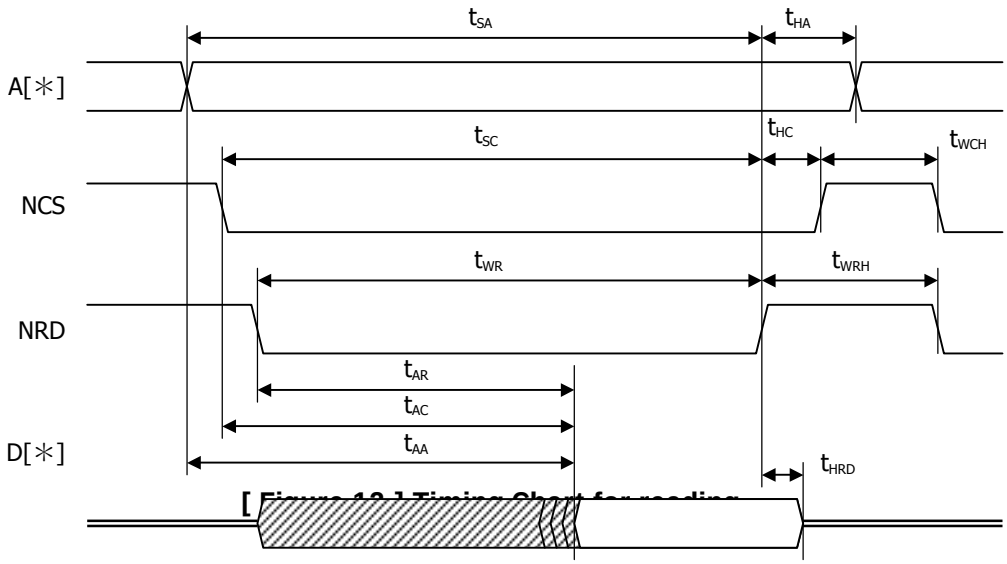
6.3.1 Access Timing

Access timing is shown in [Figure 11] and [Figure 12].

6.3.1.1 Write Timing



.3.1.2 Read Timing



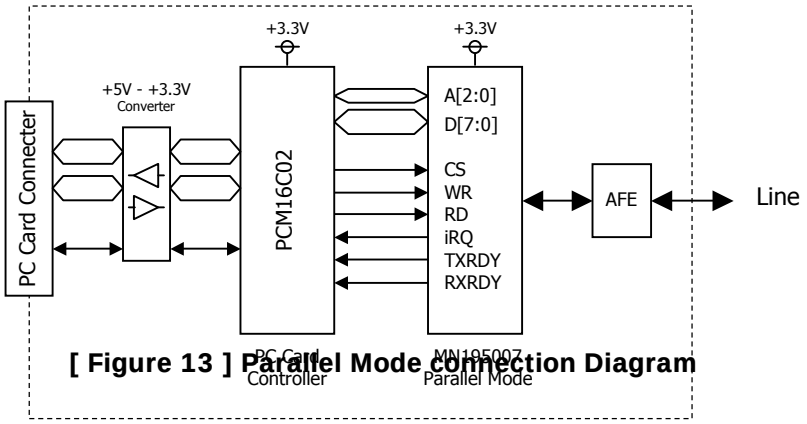
6.3.1.3 Operation Condition

Items	Symbol	Min	Max	Unit
Address Set-up	t_{SA}	t_{SC} + 5 or t_{WW} + 5	---	ns
Address Hold	t_{HA}	5	---	ns
Chip Select Set-up	t_{SC}	35	---	ns
Chip Select Hold	t_{HC}	0	---	ns
H Level Period for Chip Select	t_{WCH}	20	---	ns
Data Set-up	t_{SD}	35	---	ns
Data Hold	t_{HD}	0	---	ns
Write Pulse Width	t_{WW}	35	---	ns
Write H Level Period	t_{WWH}	20	---	ns
Read H Level period	t_{WRH}	20	---	ns
Address Access	t_{AA}	---	t_{AC} + 5 or t_{AR} + 5	ns
Chip Select Access	t_{AC}	---	35	ns
Read Access	t_{AR}	---	35	ns
Read Data Hold	t_{HRD}	2	---	ns

[Table 17] DPRAM Access Time

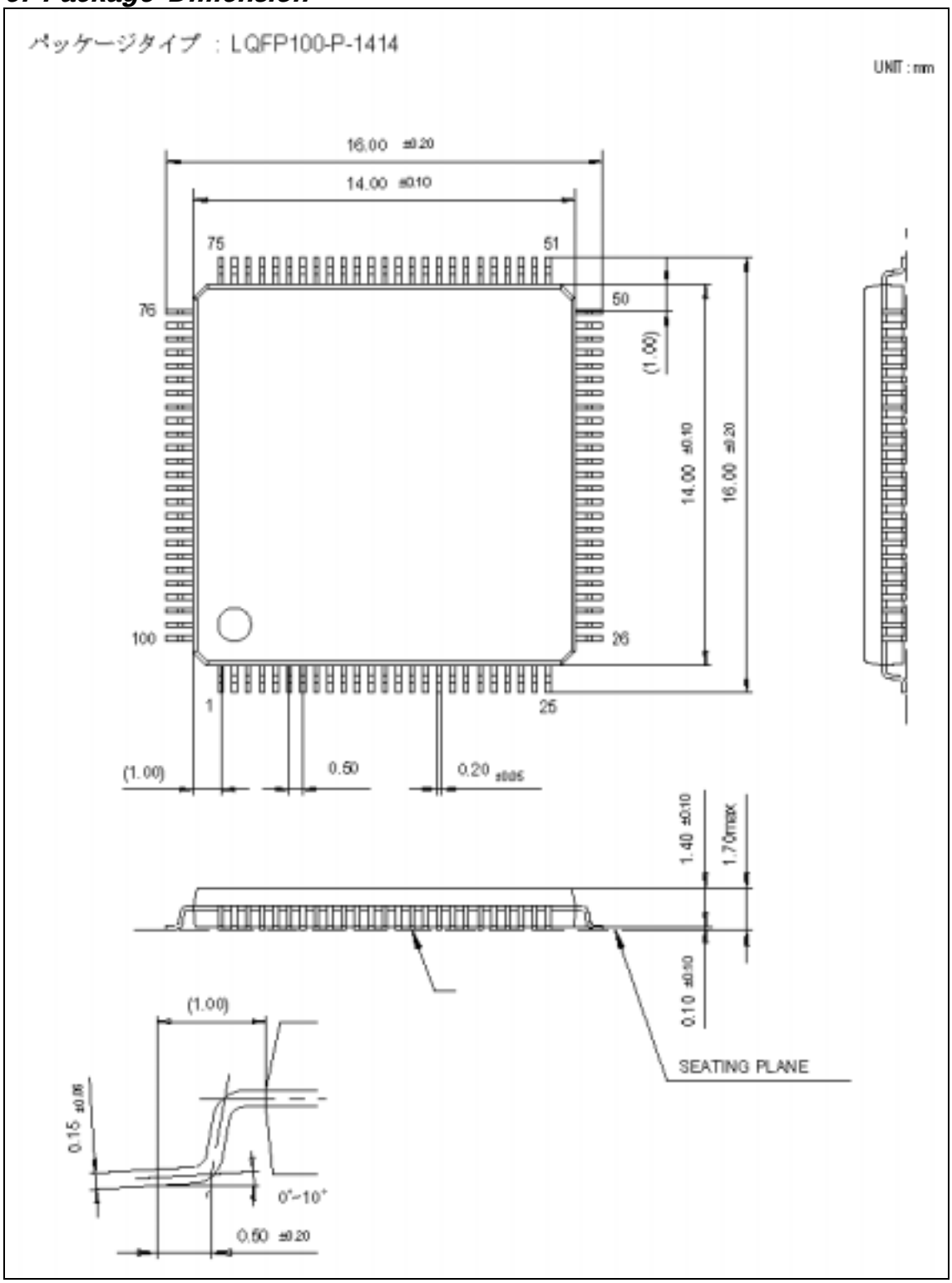
6.3.1 Connection Reference

MN195507 has operation experience PC Modem which used PC card interface IC.



[Figure 13] Parallel Mode connection Diagram

6. Package Dimension



[Table 14] Package Dimensions