Laser Controller

Description

The U8600B is a monolithic integrated circuit using TEMIC's advanced UHF technology. The IC is a very high-speed, mixed–signal laser driver circuit for re-writable optical systems.

It comprises a servo amplifier to drive the laser diode, a high-frequency modulator for noise reduction, power and pulse-width generators as well as several operation control and safety functions.

Features

- Single + 5 V power supply
- Data transfer rates up to 16 Mb/s
- Servo system
  – High bandwidth: 100 MHz
  – High dc gain: 110 dB
  – High LD drive current: typ. 100 mA, max. 180 mA
  – High slew rate: 5 ns rise/ fall time
  – Servo gain adjustable
- Noise reduction by servo loop and weak high-frequency modulation
- On-chip generation of power levels for read, erase, and write operations
- On-chip generation of write and off-pulse widths: 15 to 90 ns, 5 ns steps
- Digital control of power and pulse parameters via a serial 3-wire interface
- Basic power level adjustable
- Supervision of power supply, laser current and laser power
- Laser shutdown to prevent laser damage and data loss

Package:

44-lead shrinked small-outline IC (SSO44)
Thermal resistance: R_{thJC} = 22°C/W

Block Diagram

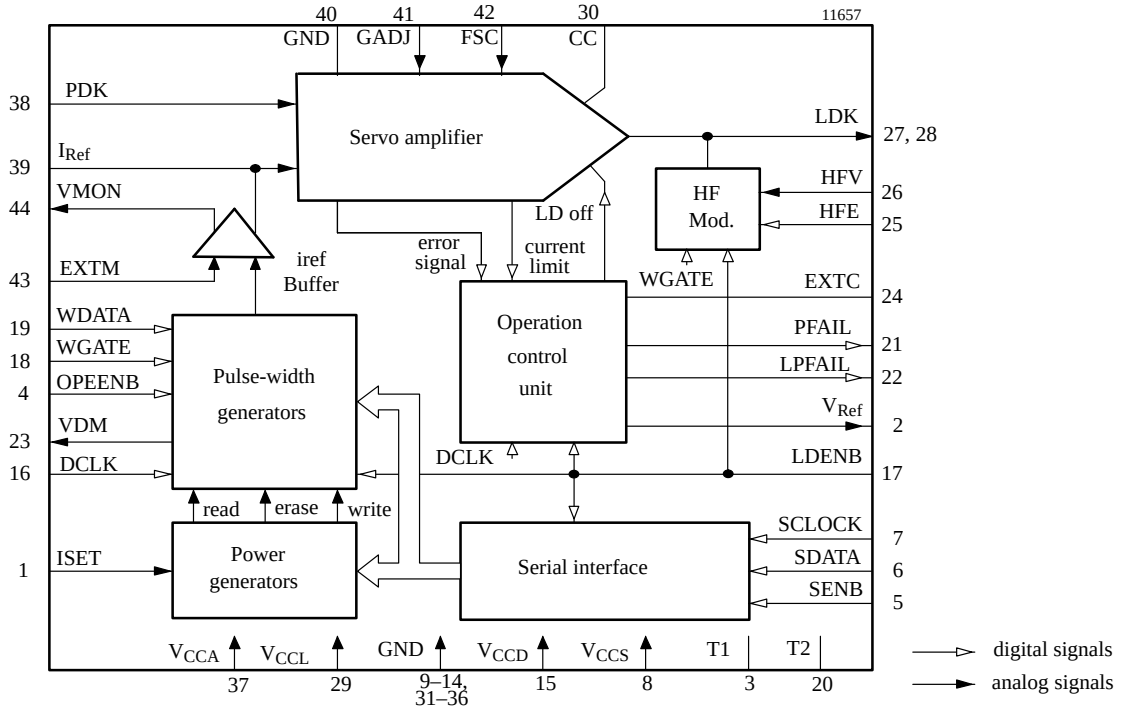


Figure 1.

General Description

U8600B is a very high-speed, mixed-signal laser driver circuit for re-writable optical disk systems. It comprises servo amplifier, high-frequency modulator, power generators, pulse-width generators, serial interface, and operation control unit.

The wideband and high-gain **servo amplifier** drives the laser diode up to 180 mA. It performs noise reduction of the laser by a feedback loop via an optical path and a monitor diode. The reference input current for the servo loop is digitally-controlled by power and pulse-width generators.

For reduction of laser mode hopping noise during read mode, the **high-frequency modulator** adds a weak modulation current of 300 MHz and a maximum swing of 5 mA.

Three **power generators** define read, erase, and write power levels with a 4-bit resolution each.

In write mode, two **pulse-width generators** generate the widths of write pulse and off pulse in the range between 15 and 90 ns with 5-ns resolution.

Read and write actions are controlled by write gate (WGATE), write data (WDATA), and off-pulse enable (OPENB) signals.

The pulse-width and power parameters are programmed via the **serial interface**. Data packets of 16-bit length can be received with a maximum clock rate of 10 MHz. The information is stored within five 4-bit registers.

The **operation control unit** supervises the power supply voltage, servo amplifier error signal, current limiter status, and manages the laser shutdown and slow start.

Pin Description

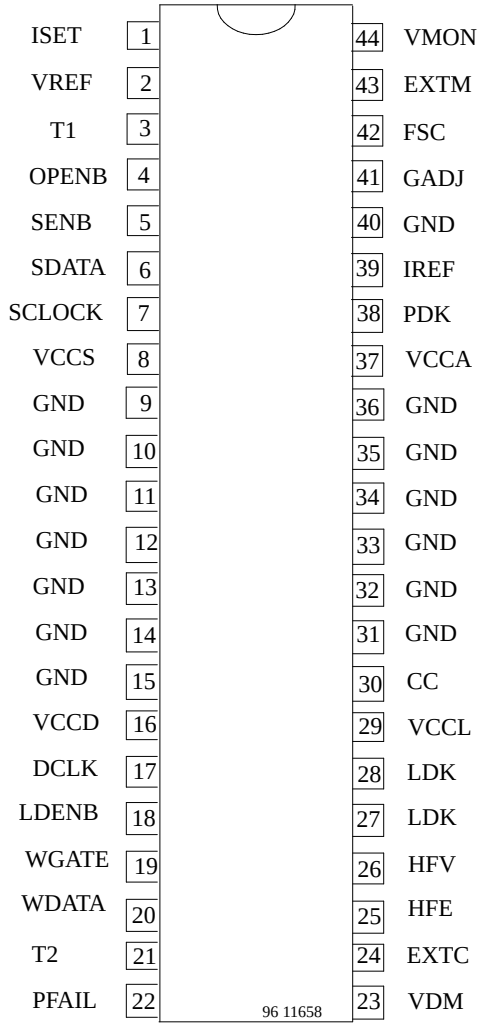


Figure 2.

Pin	Symbol	Function
1	ISET	Set input for basic power level
2	VREF	Reference voltage output
3	T1	Temperature test diode 1
4	OPENB	Off-pulse enable input
5	SENB	Serial port enable input
6	SDATA	Serial data input
7	SCLOCK	Serial clock input
8	VCCS	Power supply
9–14, 31–36, 40	GND	Ground
15	VCCD	Power supply
16	DCLK	Reference clock input
17	LDENB	LD control enable input
18	WGATE	Write mode gate input
19	WDATA	Write data pulse input
20	T2	Temperature test diode 2
21	PFAIL	Power supply fail signal
22	LPFAIL	Light power fail signal
23	VDM	Monitor voltage, delay adjustment
24	EXTC	External slow starter capacitor
25	HFE	HFM enable input
26	HFV	HFM power-control input
27, 28	LDK	LD cathode, servo-amplifier output
29	VCCL	Power supply
30	CC	Connection to int. low-pass filter
37	VCCA	Power supply
38	PDK	PD cathode, servo-amplifier input
39	IREF	Connection to servo-reference input
40	GND	Analog ground
41	GADJ	Gain adjust for error amplifier
42	FSC	Frequency slope-control input
43	EXTM	External modulation-signal input
44	VMON	Monitor current, servo reference

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage	V_{CC}	–0.5 to +6.0	V
Supply voltage differences	ΔV_{CC}	± 0.1	V
Input voltage at any input	V_{in}	–0.5 to VCC +0.5	V
LD drive current	I(LDK)	200	mA
Power dissipation	P_{max}	1	W
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	–65 to +125	°C

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply voltage range	V_{CC}	4.75 to 5.25	V
Operating temperature range	T_{amb}	0 to +75	°C

DC Characteristics

$V_{CCA} = V_{CCL} = V_{CCD} = V_{CCS}$ = 5 V, T_{amb} = 25°C, unless otherwise specified

Parameter	Test Conditions /Pin	Symbol	Min.	Typ.	Max.	Unit
Power supply						
Test circuit	VH = 5 V, VE = 0 V, WGATE = low, HFE = low, fDCLK = 2 MHz, rdata = 9					
Supply current, V_{CCA}	Pin 37	I(V_{CCA})	22		42	mA
Supply current, V_{CCL}	Pin 29	I(V_{CCL})	10		25	mA
Supply current, V_{CCD} & V_{CCS}	Pins 15 and 8	I(V_{CCDS})	20		38	mA
Typical parameters	fDCLK = 9.83 MHz, RSET = 11.2 kΩ					
Supply current, V_{CCA}	Pin 37	I(V_{CCA})		37		mA
Supply current, V_{CCL}	Pin 29, LDENB = low	I(V_{CCL})off		11		mA
Supply current, V_{CCL}	Pin 29, ILDK = 100 mA	I(V_{CCL})on		24		mA
Supply current, V_{CCD}	Pin 15	I(V_{CCD})		26		mA
Supply current, V_{CCS}	Pin 8	I(V_{CCS})		12		mA
Supply current vs. iset	Pin 37	ΔI(V_{CCA})		4.4		mA/mA
Supply current vs. iset	Pin 8	ΔI(V_{CCS})		11		mA/mA
Supply current vs. I(LDK)	Pin 29, I(LDK) > 50 mA	ΔI(V_{CCL})		0,04		mA/mA
Supply current vs. VDM	Pin 15	ΔI(V_{CCD})		4.3		mA/V
Servo amplifier						
Bias voltage	Pin 38, figure 15	V(PDK)	2.5		4.0	V
Bias voltage	Pin 39	V(I_{Ref})	2.5		4.0	V
Offset voltage	Pins 38 and 39	V(PDK)– V(I_{Ref})	–5		5	mV
Temperature drift	Pin 38, I_{Ref} = 50 µA	ΔV(PDK)		0.8		mV/°C
Temperature drift	Pin 38, I_{Ref} = 1000 µA	ΔV(PDK)		2		mV/°C
Bias voltage	Pin 30	V(CC)		2.5		V
Limiting current	Pins 27 and 28	I(LDK)lim	220		300	mA
Voltage compliance	Pins 27 and 28	V(LDK)	1.0			V
Input voltage range	Pin 41	V(GADJ)	1.5		3.0	V
Input voltage range	Pin 42	V(FSC)	1.5		3.0	V

DC Characteristics (continued)

$V_{CCA} = V_{CCL} = V_{CCD} = V_{CCS} = 5$ V, $T_{amb} = 25°C$, unless otherwise specified

Parameter	Test Conditions /Pin	Symbol	Min.	Typ.	Max.	Unit
I_{Ref} buffer						
Voltage compliance	Pin 44	V(VMON)	3.5			V
Bias voltage	Pin 43, I(EXTM) = 1 mA	V(EXTM)		0.8		V
Input current	Pin 43	I(EXTM)			2	mA
RF modulator						
Bias voltage	Pin 26	V(HFV)		1.6		V
Output current	Pin 27	I(LDK)hfm			5	mA
Current ratio, control input		I(LDK)hfm / I(HFV)		6		–
Pulse width generators						
Output voltage	Pin 23	V(VDM)	1.9		3.9	V
Power generators						
Offset voltage	Pins 1 and 2	V(ISET)– $V(V_{Ref})$	–3		3	mV
External resistor	Pin 1, offset < 3 mV	RSET		11.2		kΩ
External resistor	Pin 1, offset < 50 mV	RSETmin	7			kΩ
Gain error, read level	Pin 44	GEr	–1.5		1.5	LSB
Non-linearity error, read level	Pin 44	NLEr	–0.3		0.3	LSB
Offset error, read level	Pin 44	OEr			0.1	LSB
Gain error, erase level	Pin 44	GEe	–1.5		1.5	LSB
Non-linearity, erase level	Pin 44	NLe	–0.3		0.3	LSB
Offset, erase level	Pin 44	OEe			0.1	LSB
Gain error, write level	Pins 27 and 28	GEw	–1.5		1.5	LSB
Non-linearity, write level	Pins 27 and 28	NLw	–0.5		0.5	LSB
Ratio, erase/ read level	Pin 44, preset levels	ie/ir	3.7		4.3	–
Ratio, write/ read level	Pin 44, preset levels	iw/ir		7		–
Reference voltage						
Output voltage	Pin 2	$V(V_{Ref})$	2.37	2.5	2.63	V
Temperature drift	Pin 2, T_{amb} = 0 to 75°C	$TD(V_{Ref})$	–200		200	µV/°C
Power supply rejection ratio	Pin 2, V_{CC} = 4.5 to 5.5 V	PSRR	–20		20	mV/V
Source resistance	Pin 2	$r(V_{Ref})$			10	
Limiting current	Pin 2	$I(V_{Ref})$lim	3		10	mA
Operation control unit						
Lower supply threshold voltage		V_{CC}thl	4.5		4.7	V
Upper supply threshold voltage		V_{CC}thh	5.3		5.5	V
Supply voltage for power supply fail detection		V_{CC}fail	1.5		7	V
Threshold for current limit switch-off		I(LDK)swoff	200		280	mA
Slow starter						
Bias voltage, high status	Pin 24	V(EXTC)hi		3.0		V
Saturation voltage, low status	Pin 24, Iload = 4 mA	V(EXTC)lo	2.1	2.9		V
Charge current	Pin 24	I(EXTC)	9	17		µA

DC Characteristics (continued)

$V_{CCA} = V_{CCL} = V_{CCD} = V_{CCS} = 5$ V, $T_{amb} = 25°C$, unless otherwise specified

Parameter	Test Conditions /Pin	Symbol	Min.	Typ.	Max.	Unit
Digital inputs HFE, WDATA, WGATE, OPENB, DCLK, SENB, SDATA, SCLOCK, LDENB						
L-input voltage		V_{IL}			0.8	V
H-input voltage		V_{IH}	3.5			V
Threshold voltage		V_{th}		2.5		V
L-input current		I_{IL}	–70			µA
H-input current		I_{IH}			70	µA
Open collector outputs PFAIL, LPFAIL						
L-output voltage	I_{OL} = 2 mA	V_{OL}			0.4	V
L-output current		I_{OL}			2	mA
Output leakage current		I_{OH}			10	µA
Temperature test diodes T1, T2						
Diode voltage	Id = 100 µA	Vd		750		mV
Temperature dependancy		$\Delta Vd/\Delta\delta$		1.5		mV/°C
Bias current		Id			300	µA

AC Characteristics

$V_{CCA} = V_{CCL} = V_{CCD} = V_{CCS} = 5$ V, $T_{amb} = 25$ C, unless otherwise specified

Parameter	Test Conditions /Pin	Symbol	Min.	Typ.	Max.	Unit
Servo amplifier						
Open loop parameters	without LD, I(LDK)sa = 100 mA					
DC gain	V(GADJ) = V(FSC) = 2.5V	gDC		110		dB
Low frequency pole	V(FSC) = 2.5 V	fpLF		60		kHz
High frequency pole	V(GADJ) = 2.5 V	fpHF		10		MHz
High frequency gain	V(GADJ) = 2.5 V f = 100 MHz	gHF		42		dB
Phase margin	V(GADJ) = 2.5 V C(PDK) = CREF = 10 pF f = 100 MHz	$\Delta\varphi$		75		°
Gain adjust range	V(GADJ) = 1.5 to 2.5 V, figure 10	Δg		14		dB
Low frequency gain adjust range	V(FSC) = 1.5 to 2.5 V, figure 11	ΔgLF		10		dB
Shift range of low frequency slope	V(FSC) = 1.5 to 2.5 V, figure 7	$\Delta fpLF$		3		–

AC Characteristics (continued)

$V_{CCA} = V_{CCL} = V_{CCD} = V_{CCS} = 5$ V, $T_{amb} = 25$ C, unless otherwise specified

Parameter	Test Conditions /Pin	Symbol	Min.	Typ.	Max.	Unit
Noise						
Output voltage	Pins 27, 28; (*), $V_{CC} = 4.5$ V	vn1		15		mVpp
Output voltage	Pins 27, 28; (*), $V_{CC} = 5.5$ V	vn2		20		mVpp
Circuit parameters						
Impedance	Pin 30	r(CC)		312 /50		Ω//pF
Series inductance	Pin 30	l(CC)		6		nH
Input dynamic range	10% compression for max., figure 14	iref	15		1000	µA
Optical pulse parameters	V(GADJ) and V(FSC) adjusted for optimal pulse shape					
Rise time	10%, 90%	Tr		5		ns
Fall time	90%, 10%	Tf		5		ns
Settling time to 5%		Tset		20		ns
Overshoot		Aos		15		%
HF modulator						
Modulation frequency		fmod	250		350	MHz
Output current swing	I(HFV) = 833 µA	I(LDK)pp		5		mA
Switch-off attenuation		aoff	30			dB
Attenuation of spurious		aspur	30			dB
LDENB	Figure 1, CEXT = 10 nF					
Slow starter delay		Tpon		1.5		ms
Switch-off delay		Tpof			100	ns
Delay time WGATE		Tdwg	200			ns
Hold time WGATE		Thlde	0			ns
WGATE	Figure 2					
Adjust time, 1st adjustment		Tadj1	7			µs
Adjust time, following adjustments		Tadj2	1			µs
Writing time		Twrt			980	µs
WDATA	Figure 3					
Leading time of WGATE	(1), fDCLK = 9.83 MHz, wpwdata = opwdata = 15	Tdw	340			ns
Hold time of WGATE	(2), fDCLK = 9.83 MHz, wpwdata = opwdata = 15	Thwg	200			ns
WDATA pulse width, high		Twph	15			ns
WDATA pulse width, low		Twpl	15			ns
WDATA period	(3), wpwdata = opwdata = 5	Twd	100			ns
WDATA period	(3), wpwdata = 2, opwdata = 0	Twd	63			ns
Delay time erase level		Te			30	ns
Delay time write pulse		Tw			30	ns
Jitter		ΔTw			0.5	ns

AC Characteristics (continued)

$V_{CCA} = V_{CCL} = V_{CCD} = V_{CCS} = 5$ V, $T_{amb} = 25°C$, unless otherwise specified

Parameter	Test Conditions /Pin	Symbol	Min.	Typ.	Max.	Unit
Pulse widths	50% of pulse amplitude					
Write pulse width, wpwdata = 0	OPENB = 0	Twp0	13		17	ns
Write pulse width, wpwdata = 5	OPENB = 0	Twp5	36		44	ns
Write pulse width, wpwdata = F	OPENB = 0	Twp15	81		99	ns
Write pulse width increment	OPENB = 0	ΔTwp	3.5		6	ns
Off pulse width, opwdata = 0	wpwdata = 0	Top0	13		17	ns
Off pulse width, opwdata = 5	wpwdata = 0	Top5	36		44	ns
Off pulse width, opwdata = F	wpwdata = 0	Top15	81		99	ns
Off pulse width increment	wpwdata = 0	ΔTop	3.5		6	ns
Temperature drift	pulse width: 40 ns	ΔTp/Δδ		14		ps/°C
Operation control unit	Figure 4					
Fail period		Tfail	2.6		3.5	µs
Serial interface	Figure 5					
SCLOCK pulse cycle		TcySCK	100			ns
SCLOCK pulse width high		TwhSCK	40			ns
SCLOCK pulse width low		TwlSCK	40			ns
SENB set up time		TsSEN	20			ns
SENB hold time		ThSEN	20			ns
SDATA set up time		TsDSA	15			ns
SDATA hold time		ThDSA	15			ns
Data change delay time	Figure 6	Tdcha			1.5	µs

(*) Test circuit with electrical feedback on page 10. Measurement with sampling head with 300 ps sampling time. Peak-to-peak value of 1200 measurements, each measurement represents the average of 64 samples. These noise values ensure a stable operation of the servo amplifier for $T_{amb} = 0$ to 75°C.

(1) Tdwd depends on DCLK frequency and write pulse width: Tdwd = 2/fDCLK + Twp + 38 ns

(2) Tdwg depends on write pulse width and off pulse width: Tdwg = Twp + Top

(3) Twd depends on write pulse width and off pulse width: Twd = Twp + Top + 12 ns

Timing Diagrams

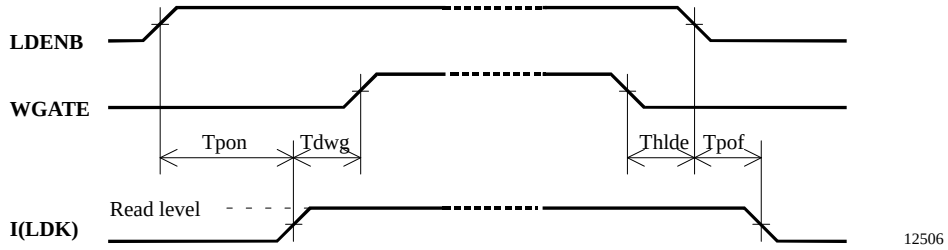


Figure 3. LDENB

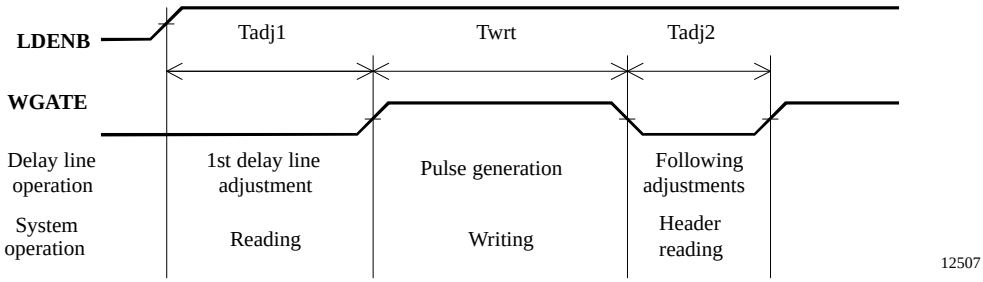


Figure 4. WGATE

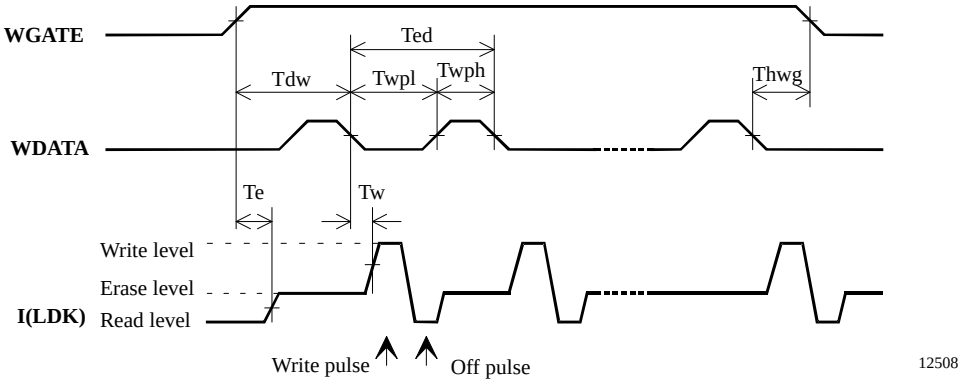


Figure 5. WDATA

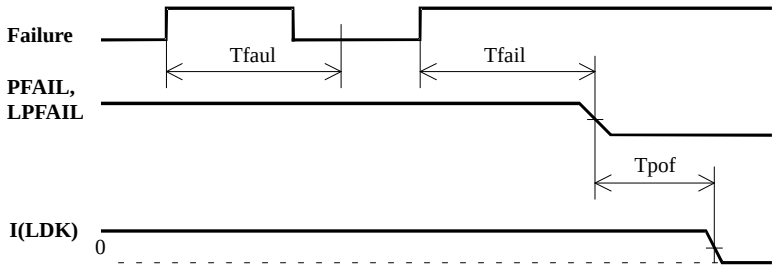


Figure 6. Power supply fail and laser power fail

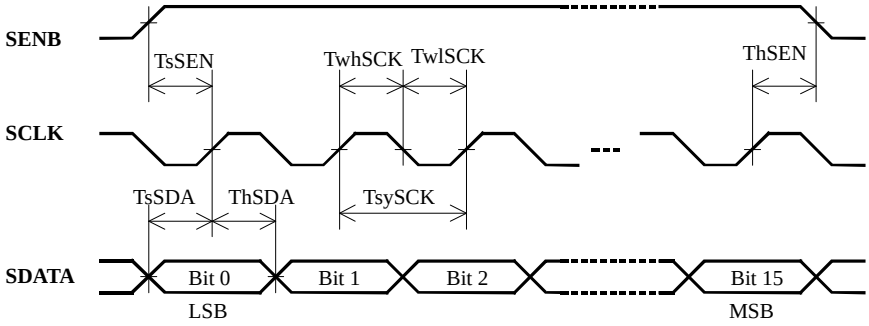


Figure 7. Serial interface

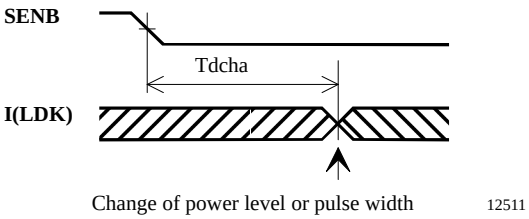


Figure 8. Data change

Typical Operating Circuit

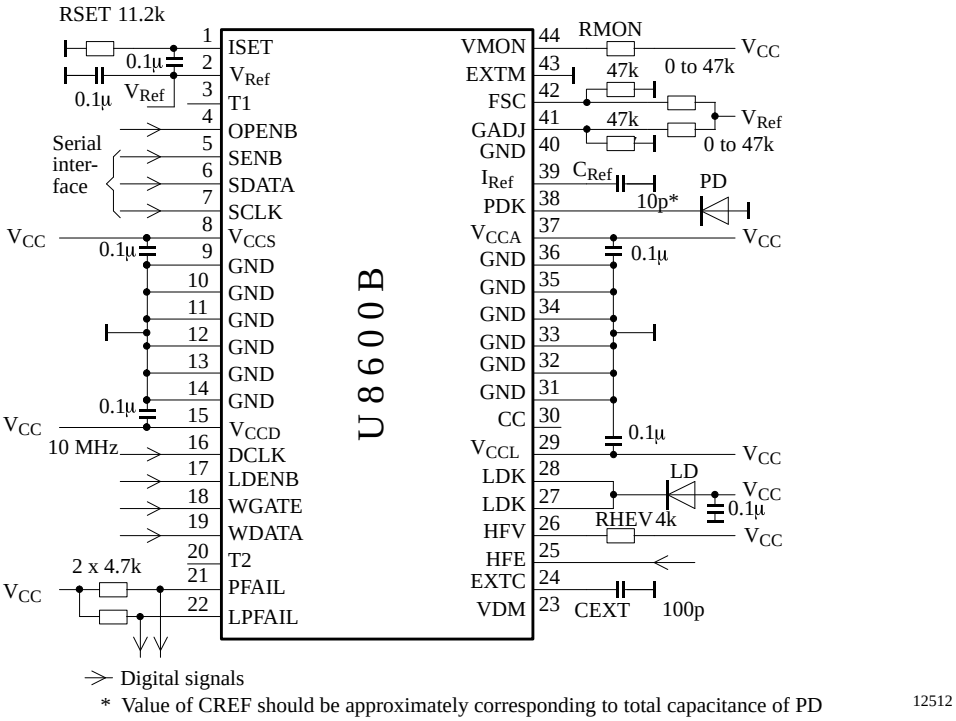


Figure 9.

Test Circuit (Electrical Feedback)

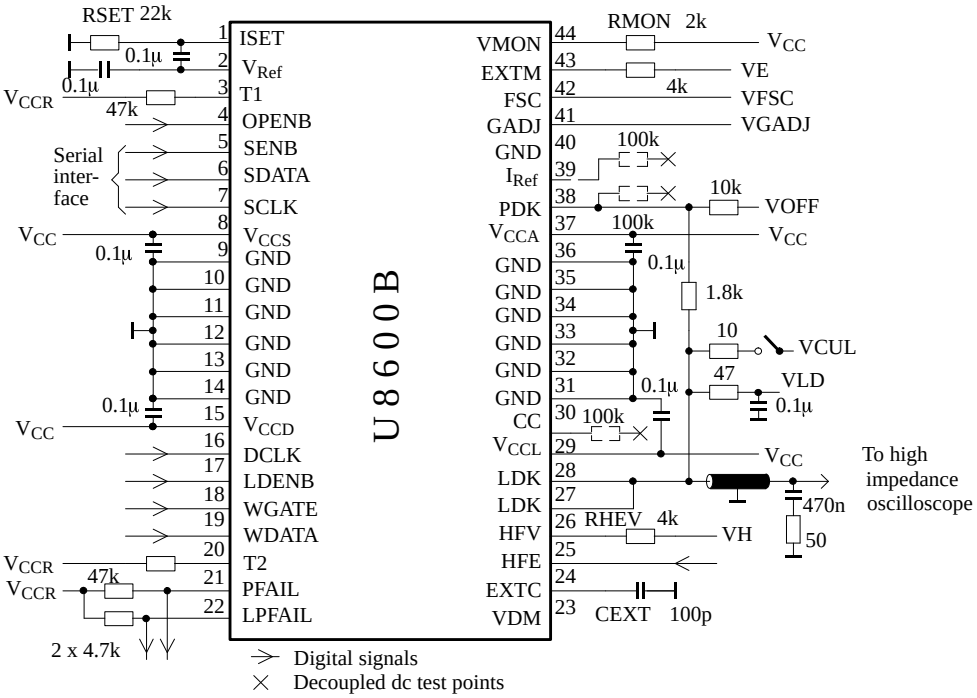
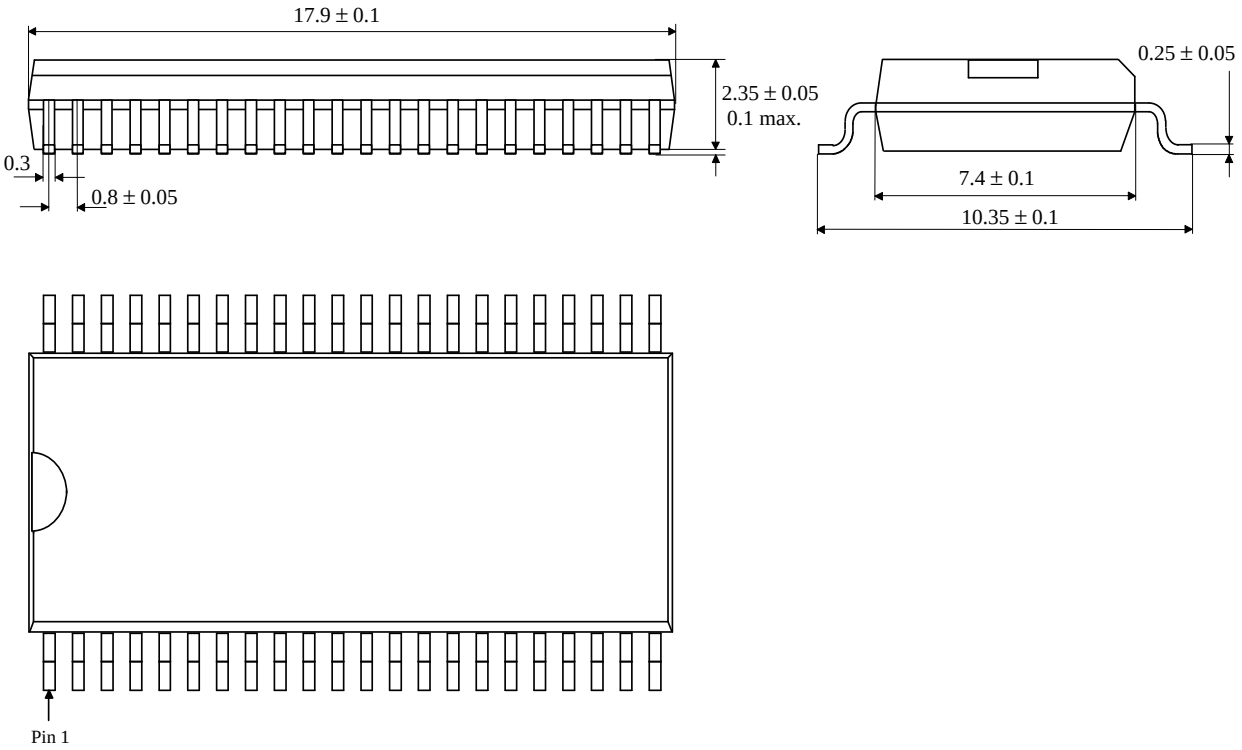


Figure 10.

Package Information

Package: SSO44
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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