

1 PRODUCT OVERVIEW

KS88-SERIES MICROCONTROLLERS

Samsung's KS88 series of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Among the major CPU features are:

- Efficient register-oriented architecture
- Selectable CPU clock sources
- Idle and Stop power-down mode release by interrupt
- Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum of four CPU clocks) can be assigned to specific interrupt levels.

KS88C2416/P2416/C2432/P2432 MICROCONTROLLER

The KS88C2416/P2416/C2432/P2432 single-chip CMOS microcontroller are fabricated using the highly advanced CMOS process, based on Samsung's newest CPU architecture.

The KS88C2416 is a microcontroller with a 16-Kbyte mask-programmable ROM embedded.

The KS88C2432 is a microcontroller with a 32-Kbyte mask-programmable ROM embedded.

The KS88P2416 is a microcontroller with a 16-Kbyte one-time-programmable ROM embedded.

The KS88P2432 is a microcontroller with a 32-Kbyte one-time-programmable ROM embedded.

Using a proven modular design approach, Samsung engineers have successfully developed the KS88 C2416/P2416/C2432/P2432 by integrating the following peripheral modules with the powerful SAM8 core:

- Six programmable I/O ports, including five 8-bit ports and one 5-bit port, for a total of 45 pins.
- Eight bit-programmable pins for external interrupts.
- One 8-bit basic timer for oscillation stabilization and watchdog functions (system reset).
- Two 8-bit timer/counter and two 16-bit timer/counter with selectable operating modes.
- Watch timer for real time.
- 8-input A/D converter
- Serial I/O interface

The KS88C2416/P2416/C2432/P2432 is versatile microcontroller for camera, LCD and ADC application, etc. They are currently available in 80-pin TQFP and 80-pin QFP package

OTP

The KS88P2416/P2432 are OTP (One Time Programmable) version of the KS88C2416/C2432 microcontroller. The KS88P2416 microcontroller has an on-chip 16-Kbyte one-time-programmable EPROM instead of a masked ROM. The KS88P2432 microcontroller has an on-chip 32-Kbyte one-time-programmable EPROM instead of a masked ROM. The KS88P2416 is comparable to the KS88C2416, both in function and in pin configuration. The KS88P2432 is comparable to the KS88C2432, both in function and in pin configuration.

FEATURES

Memory

- ROM: 32-Kbyte (KS88C2432/P2432)
- ROM: 16-Kbyte (KS88C2416/P2416)
- RAM: 1056-Byte (KS88C2432/P2432, KS88C2424/P2424)
- RAM: 544-Byte (KS88C2416/P2416, KS88C2408/P2408)
- Data memory mapped I/O

Oscillation Sources

- Crystal, ceramic, RC (main)
- Crystal for subsystem clock
- Main system clock frequency 1-10 MHz (3 MHz at 1.8 V, 10 MHz at 2.7 V)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider (1/1, 1/2, 1/8, 1/16)

Two Power-Down Modes

- Idle (only CPU clock stops)
- Stop (System clock stops)

Interrupts

- 6 level 8 vector 8 internal interrupt
- 2 level 8 vector 8 external interrupt

45 I/O Pins

- 45 configurable I/O pins

Basic Timer

- Overflow signal makes a system reset.
- Watchdog function

8-Bit Timer/Counter A

- Programmable 8-bit timer
- Interval, capture, PWM mode
- Match/capture, overflow interrupt

8-Bit Timer/Counter B

- Programmable 8-bit timer
- Carrier frequency generator

16-Bit Timer/Counter 0

- Programmable 16-bit timer
- Match interrupt generates

16-Bit Timer/Counter 1

- Programmable 16-bit timer
- Interval, capture, PWM mode
- Match/capture, overflow interrupt

Watch Timer

- Real-time and interval time measurement
- Clock generation for LCD
- Four frequency outputs for buzzer sound

LCD Controller/Driver

- Maximum 16-digit LCD direct drive capability
- Display modes: static, 1/2 duty (1/2 bias)
- 1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)

A/D Converter

- Eight analog input channels
- 50 μ s conversion speed at 1 MHz f_{ADC} clock
- 10-bit conversion resolution

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first/MSB-first transmission selectable
- Internal/external clock source

Voltage Booster

- LCD display voltage supply
- S/W control en/disable
- 3.0 V drive

Voltage Detector

- Programmable detection voltage (2.2 V, 2.4 V, 3.0 V, 4.0 V)
- En/Disable S/W selectable

Instruction Execution Times

- 400 ns at 10 MHz (main)
- 122 μ s at 32.768 kHz (subsystem)

Operating Temperature Range

- -40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V

Package Type

- 80-pin QFP
- 80-pin TQFP

KS88C2432's ROM version device

- KS88C2424 (ROM 24 Kbyte)

KS88C2416's ROM version device

- KS88C2408 (ROM 8 Kbyte)

BLOCK DIAGRAM

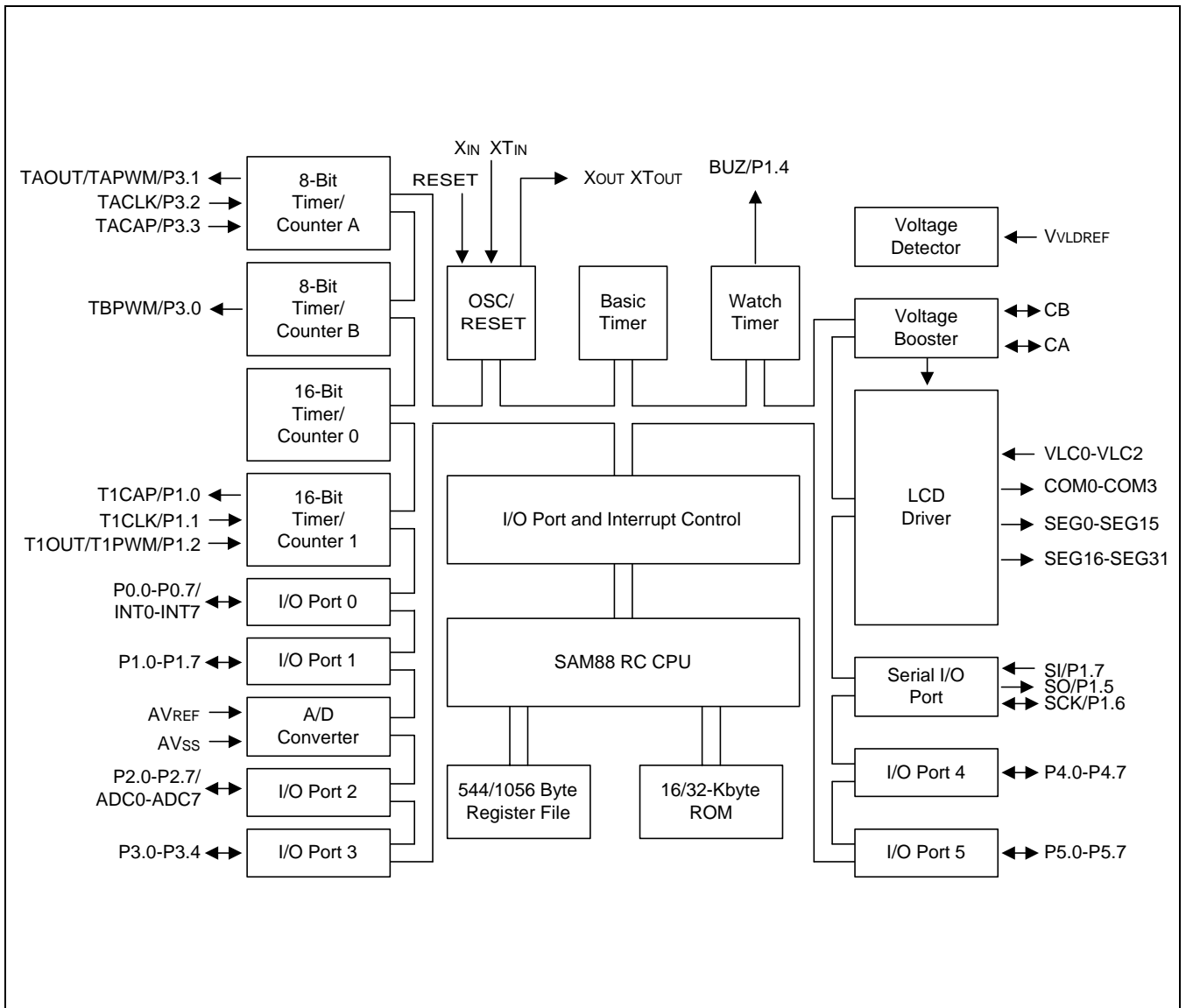


Figure 1-1. KS88C2416/2432 Block Diagram

PIN ASSIGNMENT

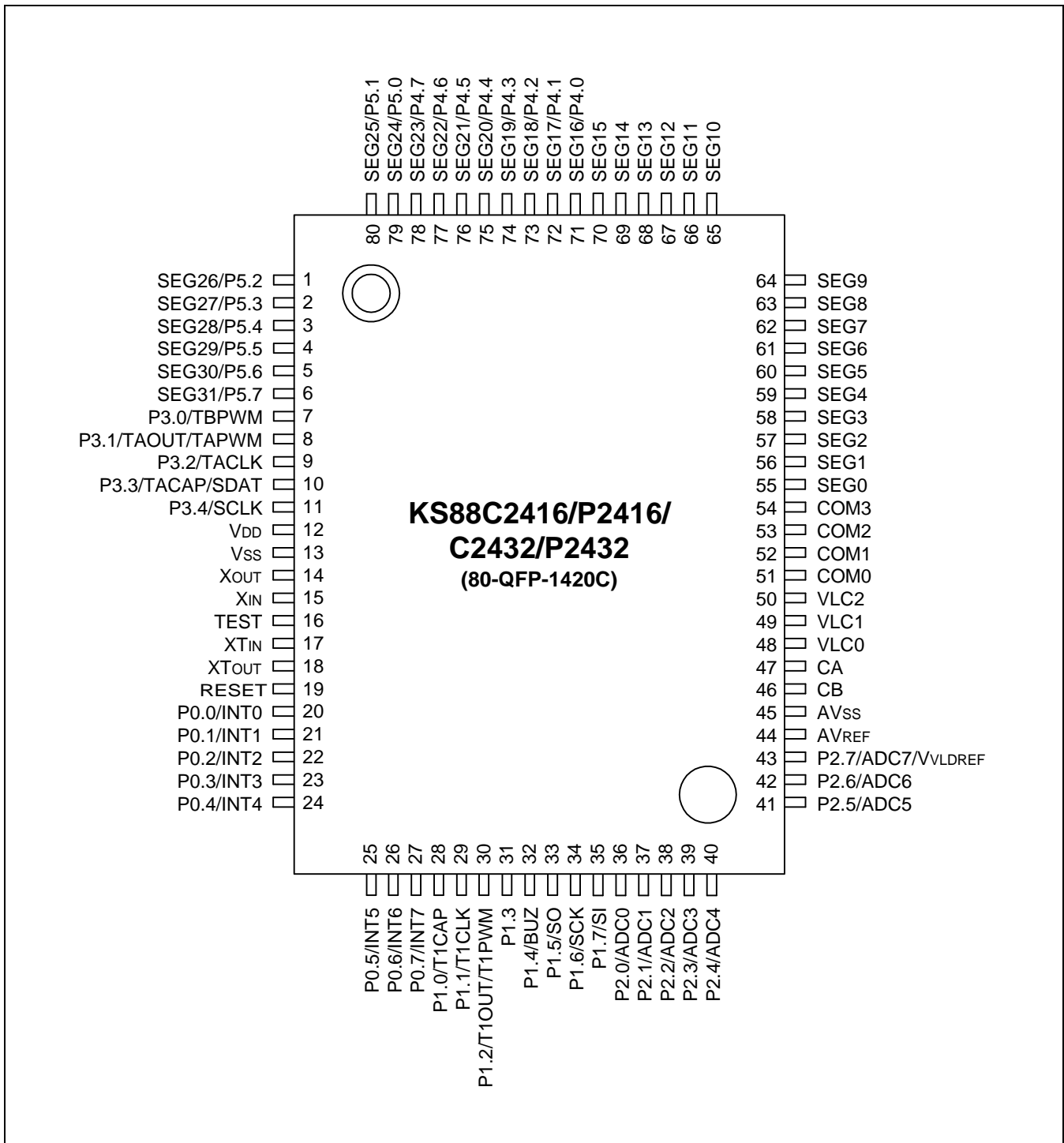


Figure 1-2. KS88C2416/2432 Pin Assignment (80-QFP)

PIN DESCRIPTIONS

Table 1-1. KS88C2416/2432 Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Type	Pin Numbers (note)	Share Pins
P0.0–P0.7	I/O	I/O port with bit programmable pins; Schmitt trigger input or output mode selected by software; software assignable pull-up. P0.0–P0.7 can be used as inputs for external interrupts INT0–INT7 (with noise filter and interrupt control).	D–4	20–27	INT0–INT7
P1.0–1.7	I/O	I/O port with bit programmable pins; Input or output mode selected by software; Open-drain output mode can be selected by software; software assignable pull-up. Alternately P1.0–P1.7 can be used as SI, SO, SCK, BUZ, T1CAP, T1CLK, T1OUT, T1PWM	E–2	28-35	SI, SO, SCK, BUZ, T1CAP T1CLK T1OUT T1PWM
P2.0–P2.7	I/O	I/O port with bit programmable pins; normal input and AD input or output mode selected by software; software assignable pull-up.	F–10 F–18	36–42, 43	ADC0–ADC6 V _{VLDREF} (ADC7)
P3.0–P3.4	I/O	I/O port with bit programmable pins. Input or push-pull output with software assignable pull-up. Alternately P3.0–P3.3 can be used as TACAP, TACLK, TAOUT, TAPWM, TBPWM	D–2	7–11	TACAP TACLK TAOUT TAPWM TBPWM
P4.0–P4.7	I/O	I/O port with bit programmable pins. Push-pull or open drain output and input with software assignable pull-up. P4.0–P4.7 can alternately be used as outputs for LCD SEG	H–14	71–78	SEG16–SEG23
P5.0–P5.7	I/O	Have the same characteristic as port 4	H–14	79–6	SEG24–SEG31

Table 1-1. KS88C2416/2432 Pin Descriptions (Continued)

Pin Names	Pin Type	Pin Description	Circuit Type	Pin Numbers (note)	Share Pins
ADC0–ADC6 ADC7	I	A/D converter analog input channels	F–10 F–18	36–42 43	P2.0–P2.6 P2.7
AV _{REF}	–	A/D converter reference voltage	–	44	–
AV _{SS}	–	A/D converter ground	–	45	–
INT0–INT7	I	External interrupt input pins	D–4	20–27	P0.0–P0.7
RESET	I	System reset pin (pull-up resistor: 250 kΩ)	B	19	–
TEST	I	0 V: Normal MCU operating 5 V: Test mode 12 V: for OTP writing	–	16	–
SDAT, SCLK	O	Serial OTP interface pins; serial data and clock	D–2	10, 11	P3.3, P3.4
V _{DD} , V _{SS}	–	Power input pins for CPU operation (internal) and Power input for OTP Writing	–	12, 13	–
X _{OUT} , X _{IN}	–	Main oscillator pins	–	14, 15	–
SCK, SO, SI	I/O	Serial I/O interface clock signal	E–2	33–35	P1.5–P1.7
V _{VLDREF}	I	Voltage detector reference voltage input	F–18	43	P2.7
TACAP	I	Timer A Capture input	D–2	10	P3.3
TACLK	I	Timer A External clock input	D–2	9	P3.2
TAOUT/TAPWM	O	Timer A output and PWM output	D–2	8	P3.1
TBPWM	O	Timer B PWM output	D–2	7	P3.0
T1CAP	I	Timer 1 Capture input	E–2	28	P1.0
T1CLK	I	Timer 1 External clock input	E–2	29	P1.1
T1OUT/T1PWM	O	Timer 1 output and PWM output	E–2	30	P1.2
COM0–COM3	O	LCD common signal output	H	51–54	–
SEG0–SEG15	O	LCD segment output	H	55–70	–
SEG16–SEG23	O	LCD segment output	H–14	71–78	P4.0–P4.7
SEG24–SEG31	O	LCD Segment output	H–14	79–6	P5.0–P5.7
V _{LC0} –V _{LC2}	O	LCD power supply	–	48–50	–
BUZ	O	0.5, 1, 2 or 4 kHz frequency output for buzzer sound with 4.19 MHz main system clock or 32768 Hz subsystem clock	E–2	32	P1.4
CA, CB	–	Capacitor terminal for voltage booster	–	46–47	–

PIN CIRCUITS

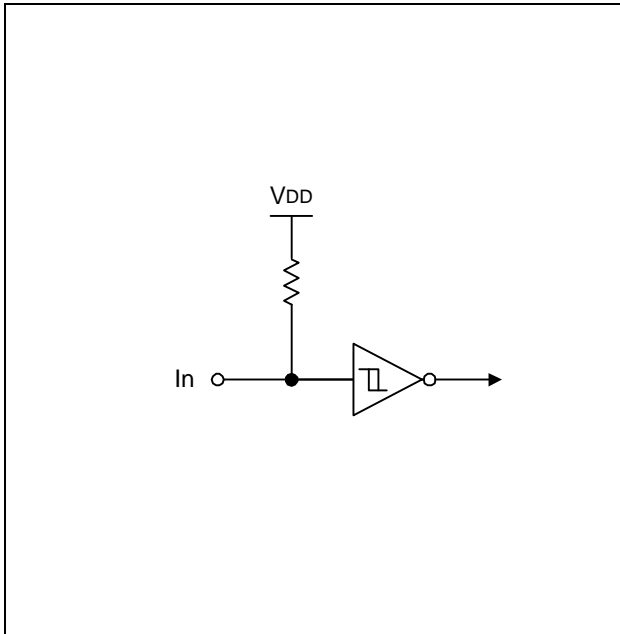


Figure 1-3. Pin Circuit Type B (RESET)

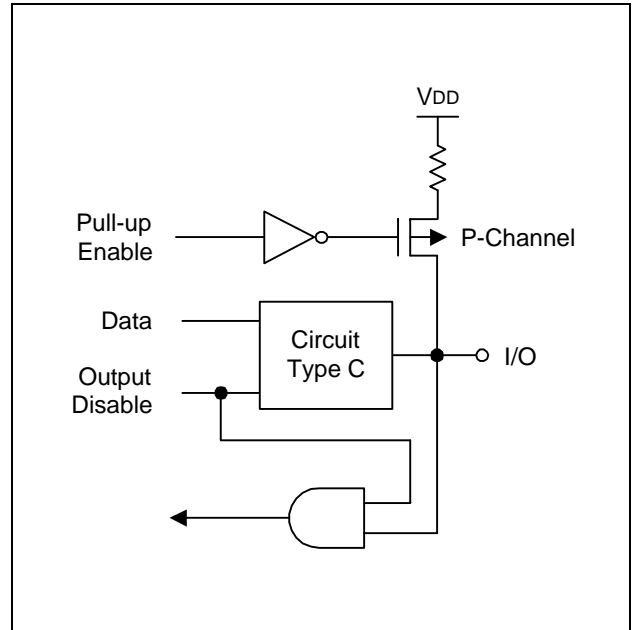


Figure 1-5. Pin Circuit Type D-2 (P3)

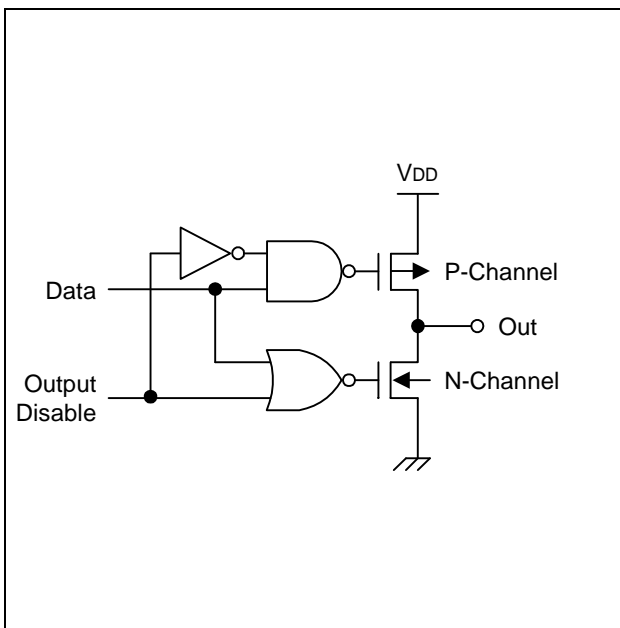


Figure 1-4. Pin Circuit Type C

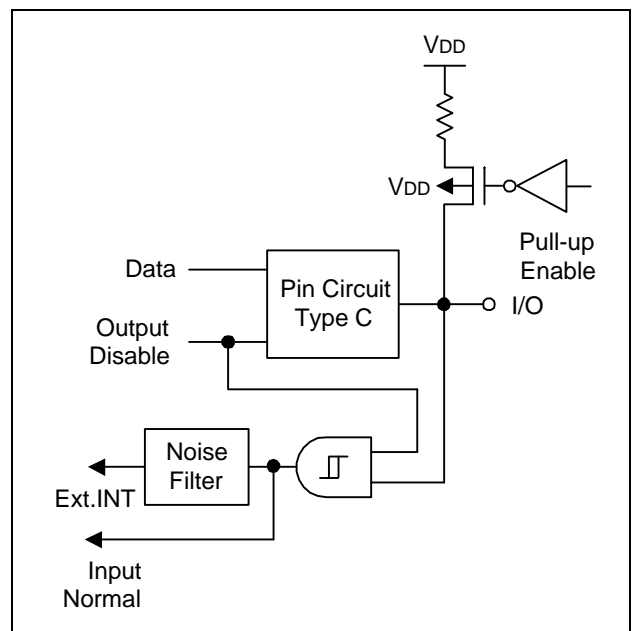


Figure 1-6. Pin Circuit Type D-4 (P0)

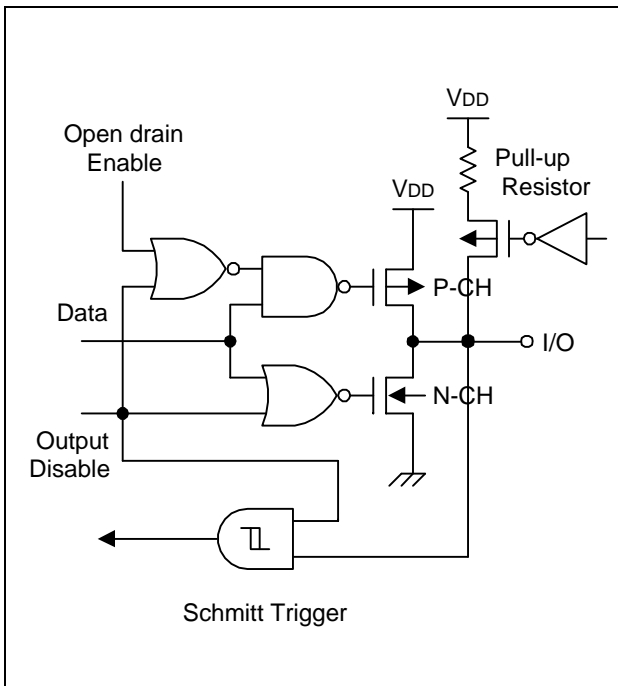


Figure 1-7. Pin Circuit Type E-2 (P1)

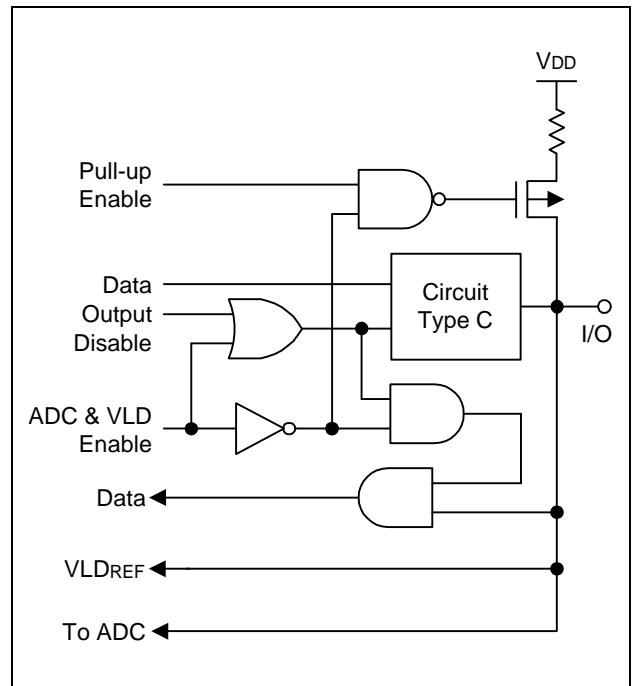


Figure 1-9. Pin Circuit Type F-18 (P2.7/VLD_{REF})

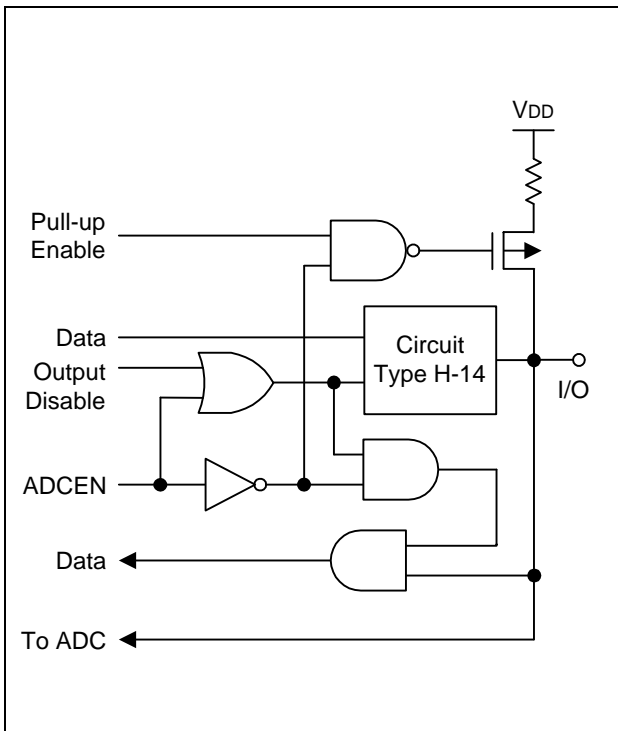


Figure 1-8. Pin Circuit Type F-10 (P2.0-P2.6)

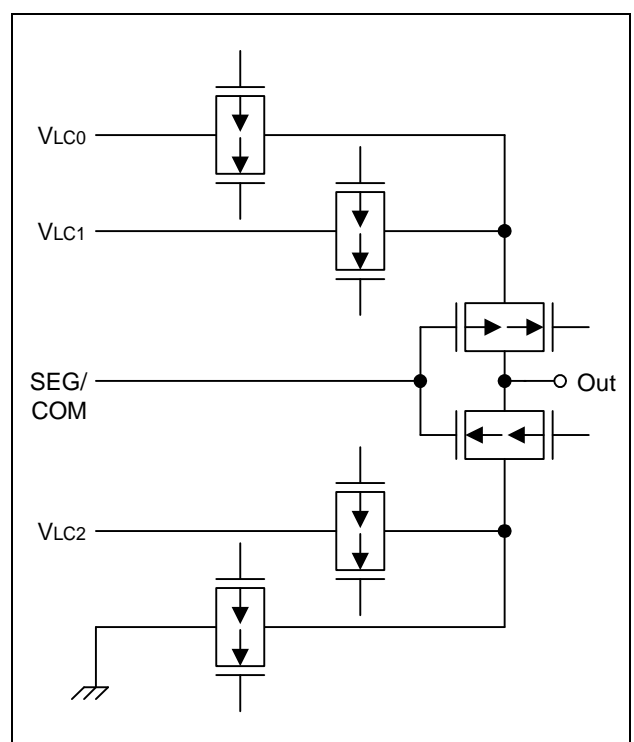


Figure 1-10. Pin Circuit Type H (SEG/COM)

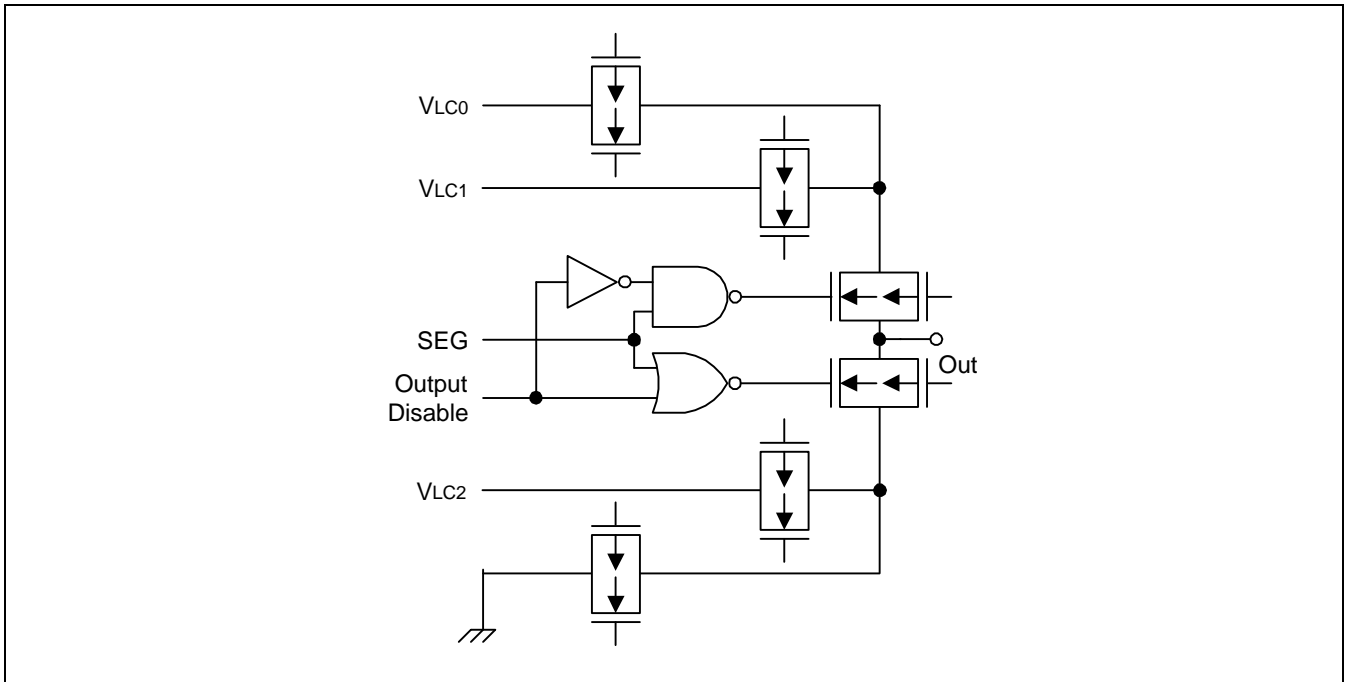


Figure 1-11. Pin Circuit Type H-4

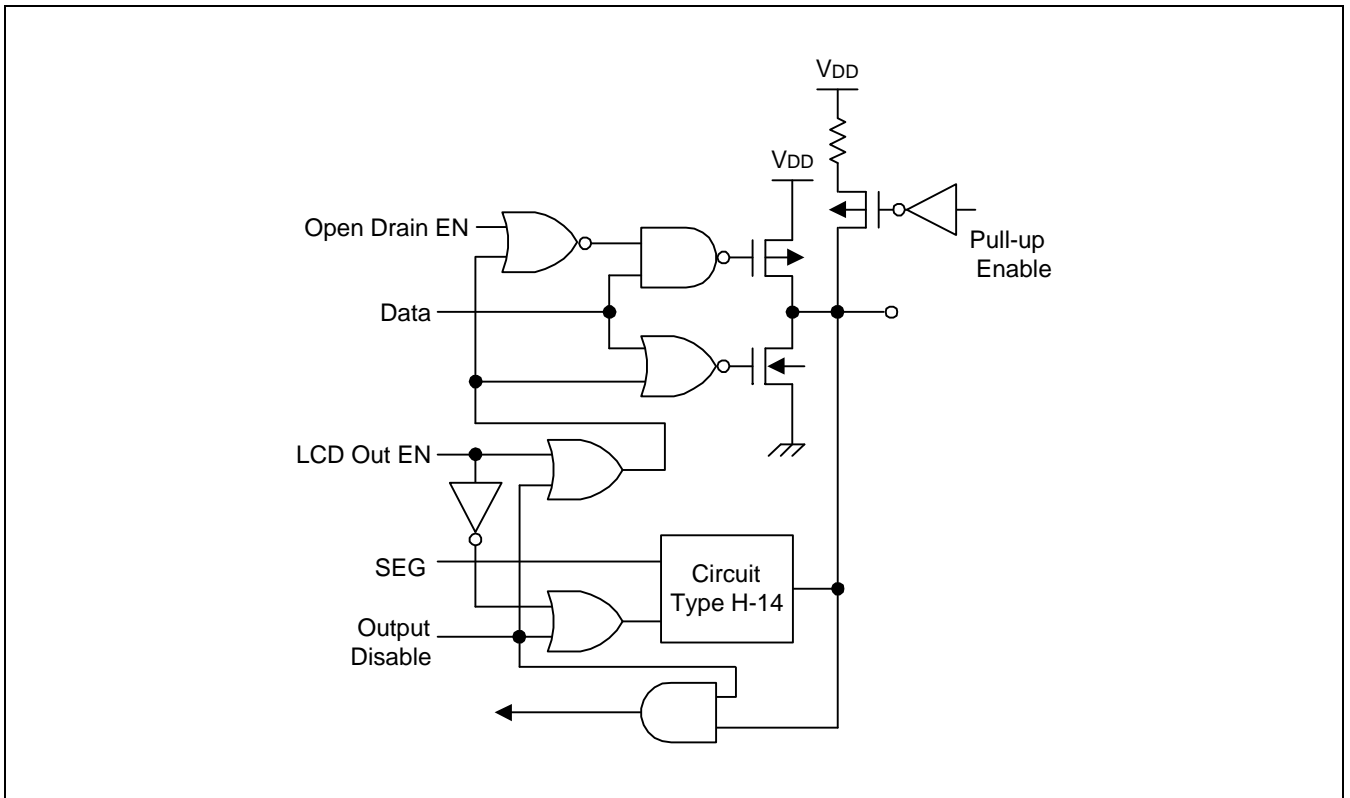


Figure 1-12. Pin Circuit Type H-14 (P4, P5)

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ELECTRICAL DATA

OVERVIEW

In this chapter, KS88C2416/C2432 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

- Absolute maximum ratings
- Input/output capacitance
- D.C. electrical characteristics
- A.C. electrical characteristics
- Oscillation characteristics
- Oscillation stabilization time
- Data retention supply voltage in stop mode
- Serial I/O timing characteristics
- A/D converter electrical characteristics

Table 19-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V _{DD}		- 0.3 to +6.5	V
Input voltage	V _I		- 0.3 to V _{DD} + 0.3	
Output voltage	V _O		- 0.3 to V _{DD} + 0.3	
Output current high	I _{OH}	One I/O pin active	- 18	mA
		All I/O pins active	- 60	
Output current low	I _{OL}	One I/O pin active	+ 30	
		Total pin current for port	+ 100	
Operating temperature	T _A		- 40 to + 85	°C
Storage temperature	T _{STG}		- 65 to + 150	

Table 19-2. D.C. Electrical Characteristics

(T_A = -40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating voltage	V _{DD}	f _{CPU} = 10 MHz	2.7	-	5.5	V
		f _{CPU} = 3 MHz	1.8	-	5.5	
Input high voltage	V _{IH1}	All input pins except V _{IH2}	0.8 V _{DD}	-	V _{DD}	
	V _{IH2}	X _{IN} , XT _{IN}	V _{DD} -0.1	-		
Input low voltage	V _{IL1}	All input pins except V _{IL2}	-	-	0.2 V _{DD}	
	V _{IL2}	X _{IN} , XT _{IN}			0.1	

Table 19-2. D.C. Electrical Characteristics (Continued)

(T_A = -40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output high voltage	V _{OH}	V _{DD} = 5 V; I _{OH} = -1 mA All output pins	V _{DD} -1.0	-	-	V
Output low voltage	V _{OL}	V _{DD} = 5 V; I _{OL} = 2 mA All output pins	-	-	0.4	
Input high leakage current	I _{LIH1}	V _{IN} = V _{DD} All input pins except I _{LIH2}	-	-	3	μA
	I _{LIH2}	V _{IN} = V _{DD} , X _{IN} , XT _{IN}			20	
Input low leakage current	I _{LIL1}	V _{IN} = 0 V All input pins except I _{LIL2}	-	-	-3	
	I _{LIL2}	V _{IN} = 0 V, X _{IN} , XT _{IN} , RESET			-20	
Output high leakage current	I _{LOH}	V _{OUT} = V _{DD} All I/O pins and output pins	-	-	3	
Output low leakage current	I _{LOL}	V _{OUT} = 0 V All I/O pins and output pins	-	-	-3	
Oscillator feed back resistors	R _{osc1}	V _{DD} = 5.0 V T _A = 25 °C X _{IN} = V _{DD} , X _{OUT} = 0 V	800	1000	1200	kΩ
Pull-up resistor	R _{L1}	V _{IN} = 0 V; V _{DD} = 5 V ±10 % Port 0,1,2,3,4,5 T _A = 25 °C	25	50	100	
	R _{L2}	V _{IN} = 0 V; V _{DD} = 5 V ±10% T _A =25 °C, RESET only	110	210	310	
V _{LC0} out voltage (Booster run mode)	V _{LC0}	T _A = 25 °C, (1/3 bias mode)	0.9	1.0	1.1	V
		T _A = 25 °C, (1/2 bias mode)	1.4	1.5	1.7	
V _{LC1} out voltage (Booster run mode)	V _{LC1}	T _A = 25 °C (1/2 and 1/3 bias mode)	2V _{LC0} - 0.1	-	2V _{LC0} + 0.1	
V _{LC2} out voltage (Booster run mode)	V _{LC2}	T _A = 25 °C (1/3 bias mode)	3V _{LC0} - 0.1	-	3V _{LC0} + 0.1	
COM output voltage deviation	V _{DC}	V _{DD} = V _{LC2} = 3 V (V _{LCD} -COMi) IO = ± 15 μA (i = 0-3)	-	± 60	± 120	mV
SEG output voltage deviation	V _{Ds}	V _{DD} = V _{LC2} = 3 V (V _{LCD} -SEGi) IO = ± 15 μA (i = 0-31)	-	± 60	± 120	

Table 19-2. D.C. Electrical Characteristics (Concluded)

(T_A = -40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current (1)	I _{DD1} (2)	V _{DD} = 5 V ± 10 % 10 MHz crystal oscillator	-	12	25	mA
		3 MHz crystal oscillator		4	10	
		V _{DD} = 3 V ± 10 % 10 MHz crystal oscillator		3	8	
		3 MHz crystal oscillator		1	5	
	I _{DD2}	Idle mode: V _{DD} = 5 V ± 10 % 10 MHz crystal oscillator	-	3	10	
		3 MHz crystal oscillator		1.5	4	
		Idle mode: V _{DD} = 3 V ± 10 % 10 MHz crystal oscillator		1.2	3	
		3 MHz crystal oscillator		0.5	1.5	
	I _{DD3}	Sub operating: main-osc stop V _{DD} = 3 V ± 10 % 32768 Hz crystal oscillator	-	20	40	uA
	I _{DD4}	Sub idle mode: main-osc stop V _{DD} = 3 V ± 10 % 32768 Hz crystal oscillator	-	7	14	
	I _{DD5}	Main stop mode : sub-osc stop V _{DD} = 5 V ± 10 %	-	1	3	
		V _{DD} = 3 V ± 10 %		0.5	2	

NOTES:

- Supply current does not include current drawn through internal pull-up resistors or external output current loads.
- I_{DD1} and I_{DD2} include a power consumption of subsystem oscillator.
- I_{DD3} and I_{DD4} are the current when the main system clock oscillation stop and the subsystem clock is used.
And does not include the LCD and Voltage booster and voltage level detector
- I_{DD5} is the current when the main and subsystem clock oscillation stop.
- Voltage booster's operating voltage range is 2.0 V to 5.5 V. The range of 1.8 V to 2.0 V could be referenced in page 17-4.

In case of KS88C2416, the characteristic of V_{OH} and V_{OL} is differ with the characteristic of KS88C2432 like as bellow. Other characteristics are same each other.

Table 19-3. D.C Electrical Characteristics of KS88C2416

($T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output high voltage	V_{OH1}	$V_{DD} = 5\text{ V}$; $I_{OH} = -1\text{ mA}$ All output pins except V_{OH2}	$V_{DD}-1.0$	–	–	V
	V_{OH2}	$V_{DD} = 5\text{ V}$; $I_{OH} = -6\text{ mA}$ Port 3.0 only in KS88C2416	$V_{DD}-0.7$			
Output low voltage	V_{OL1}	$V_{DD} = 5\text{ V}$; $I_{OL} = 2\text{ mA}$ All output pins except V_{OL2}	–	–	0.4	
	V_{OL2}	$V_{DD} = 5\text{ V}$; $I_{OH} = 12\text{ mA}$ Port 3.0 only in KS88C2416			0.7	

Table 19-4. A.C. Electrical Characteristics

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input high, low width (P0.0–P0.7)	t _{INTH} , t _{INTL}	P0.0–P0.7, V _{DD} = 5 V	200	–		ns
RESET input low width	t _{RSL}	V _{DD} = 5 V	1	–	–	us

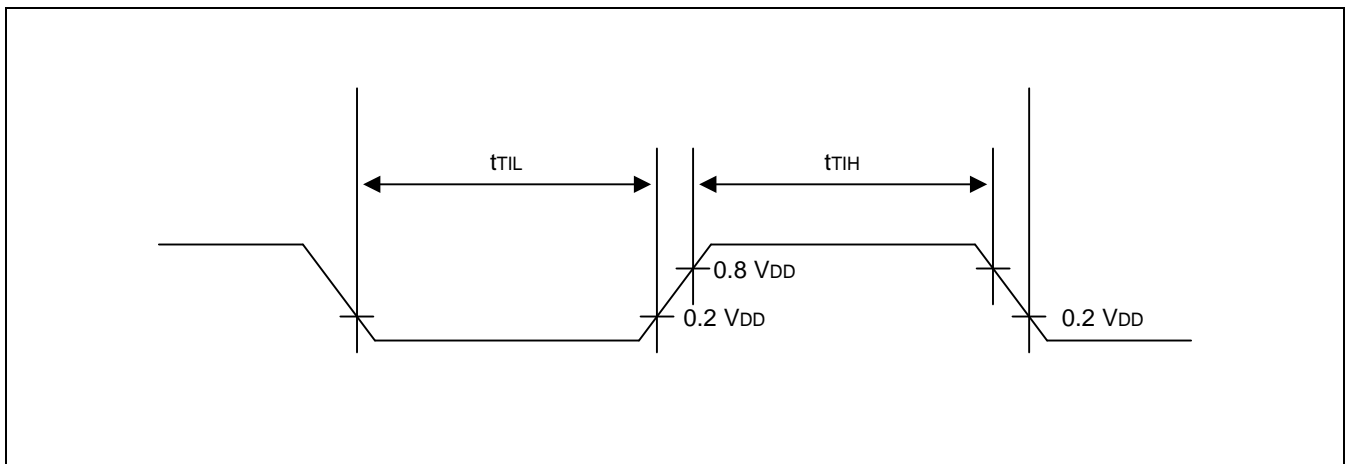
NOTE: User must keep more large value then min value.

Figure 19-1. Input Timing for External Interrupts (Ports 0)

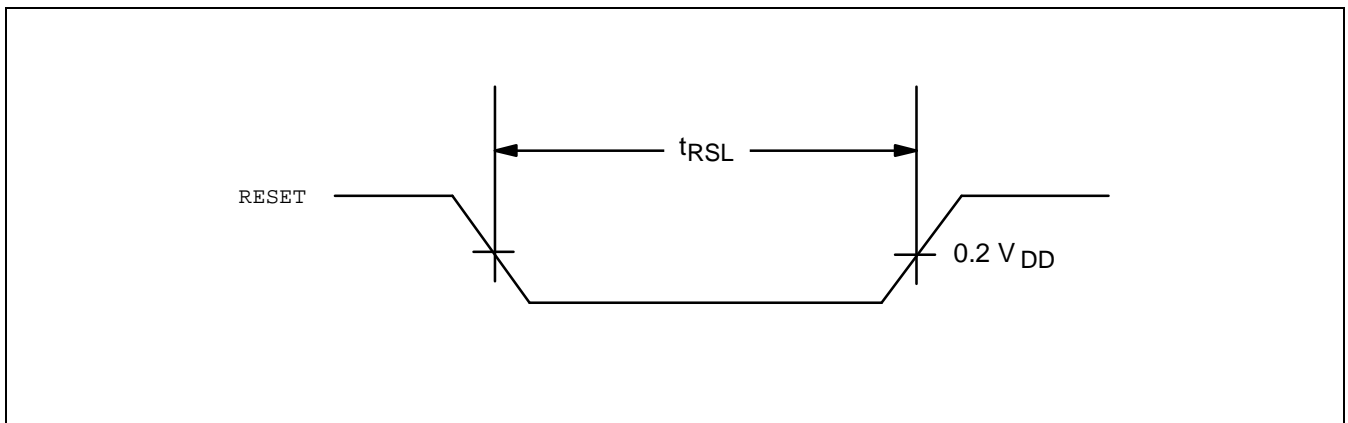


Figure 19-2. Input Timing for RESET

Table 19-5. Input/Output Capacitance

($T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	$f = 1\text{ MHz}$; unmeasured pins are returned to V_{SS}	-	-	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

Table 19-6. Data Retention Supply Voltage in Stop Mode

($T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}		2	-	5.5	V
Data retention supply current	I_{DDDR}	$V_{DDDR} = 2\text{ V}$	-	-	3	uA

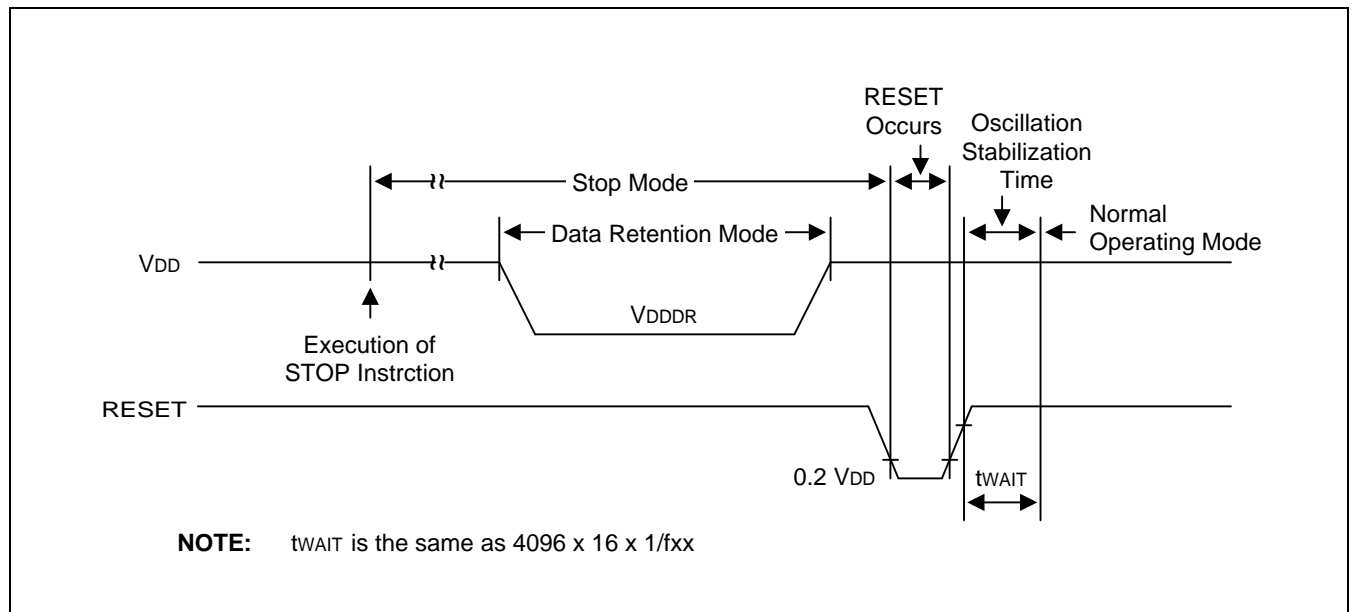


Figure 19-3. Stop Mode Release Timing Initiated by RESET

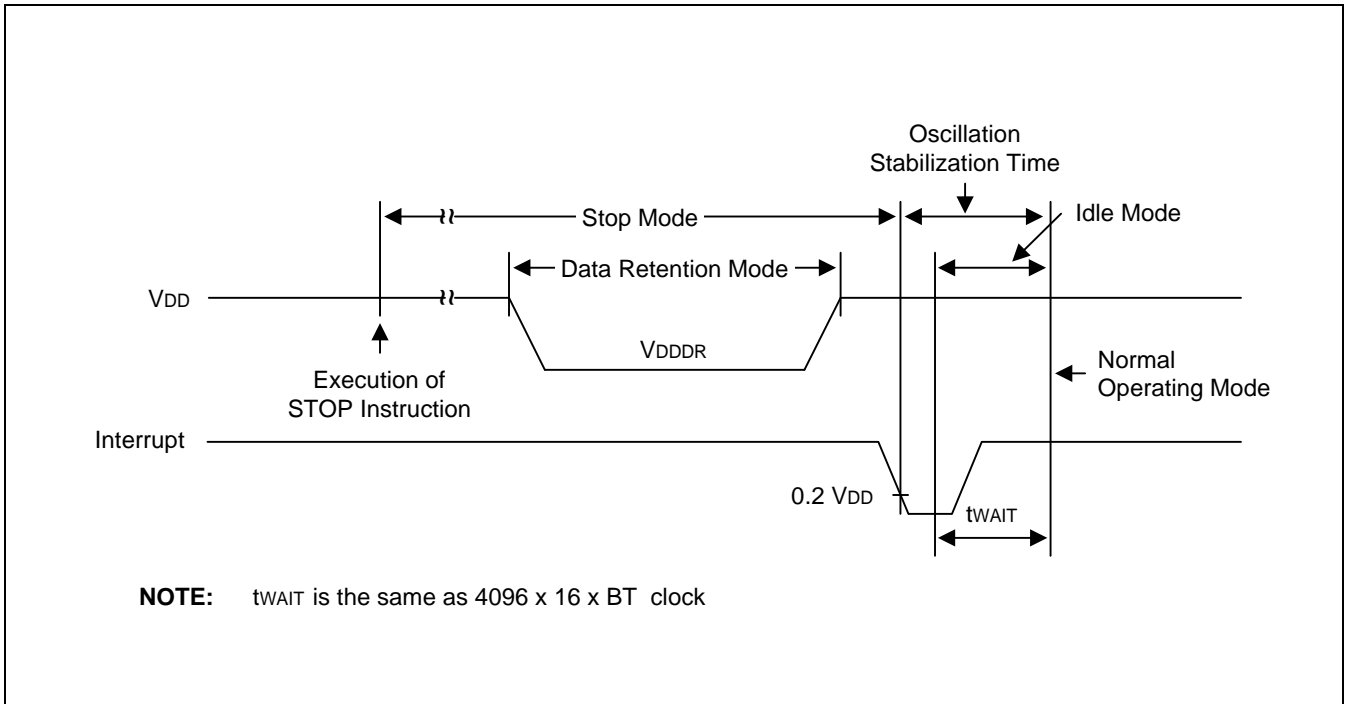


Figure 19-4. Stop Mode(main) Release Timing Initiated by Interrupts

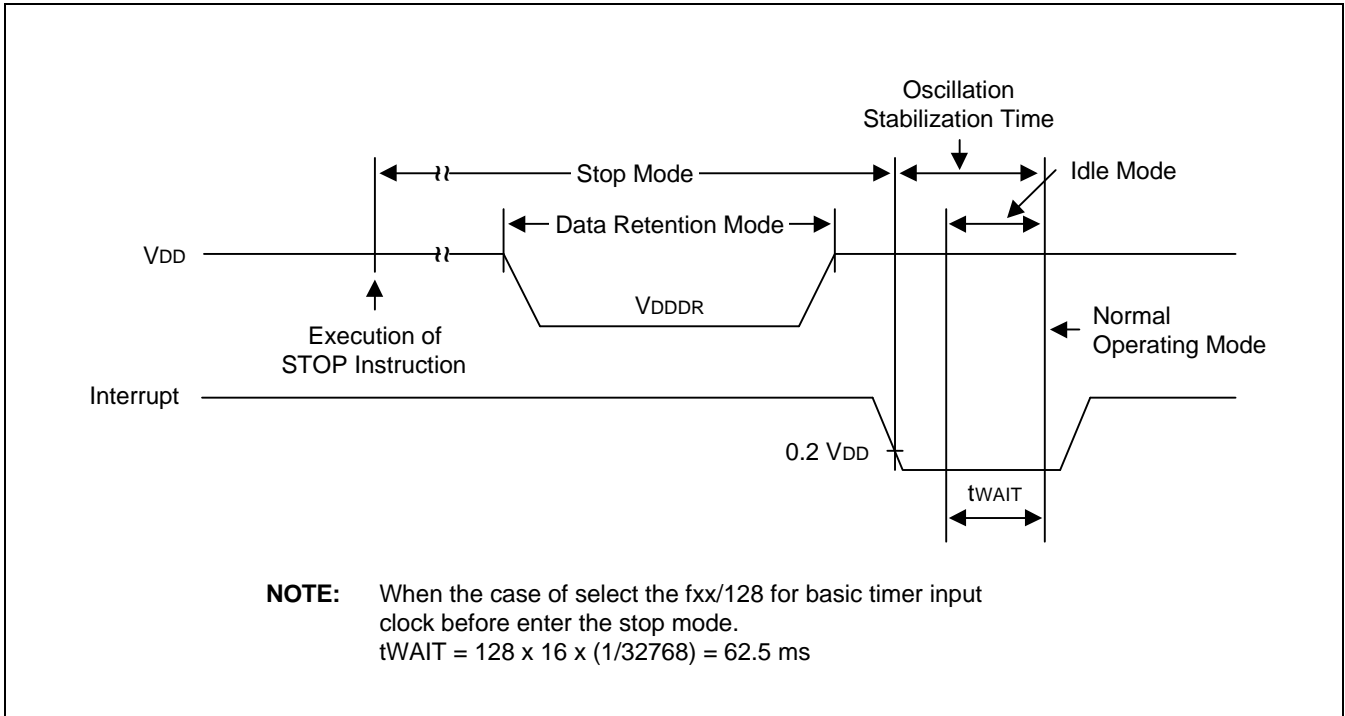


Figure 19-5. Stop Mode(sub) Release Timing Initiated by Interrupts

Table19-7. A/D Converter Electrical Characteristics

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution			–	10	–	bit
Total accuracy		V _{DD} = 5 V AV _{REF} = 5 V AV _{SS} = 0 V	–	–	±3	LSB
Integral Linearity Error	ILE			–	±2	
Differential Linearity Error	DLE			–	±1	
Offset Error of Top	EOT			±1	±3	
Offset Error of Bottom	EOB			±0.5	±2	
Conversion time ⁽¹⁾	t _{CON}	–	–	40	–	fx
Analog input voltage	V _{IAN}	–	AV _{SS}	–	AV _{REF}	V
Analog input impedance	R _{AN}	–	2	1000	–	Mohm
Analog reference voltage	AV _{REF}	–	2.5	–	V _{DD}	V
Analog ground	AV _{SS}	–	V _{SS}	–	V _{SS} + 0.3	
Analog input current	I _{ADIN}	AV _{REF} = V _{DD} = 5 V	–	–	10	uA
Analog block current ⁽²⁾	I _{ADC}	AV _{REF} = V _{DD} = 5 V	–	1	3	mA
		AV _{REF} = V _{DD} = 3 V		0.5	1.5	
		AV _{REF} = V _{DD} = 5 V When power down mode		100	500	nA

NOTES:

- 'Conversion time' is the time required from the moment a conversion operation starts until it ends.
- I_{ADC} is an operating current during A/D conversion.

Table 19-8. Synchronous SIO Electrical Characteristics

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V, V_{SS} = 0 V, f_{xx} = 10 MHz oscillator)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SCK Cycle time	t _{CYC}	–	200	–	–	ns
Serial Clock High Width	t _{SCKH}	–	60	–	–	
Serial Clock Low Width	t _{SCKL}	–	60	–	–	
Serial Output data delay time	t _{OD}	–	–	–	50	
Serial Input data setup time	t _{ID}	–	40	–	–	
Serial Input data Hold time	t _{IH}	–	100	–	–	

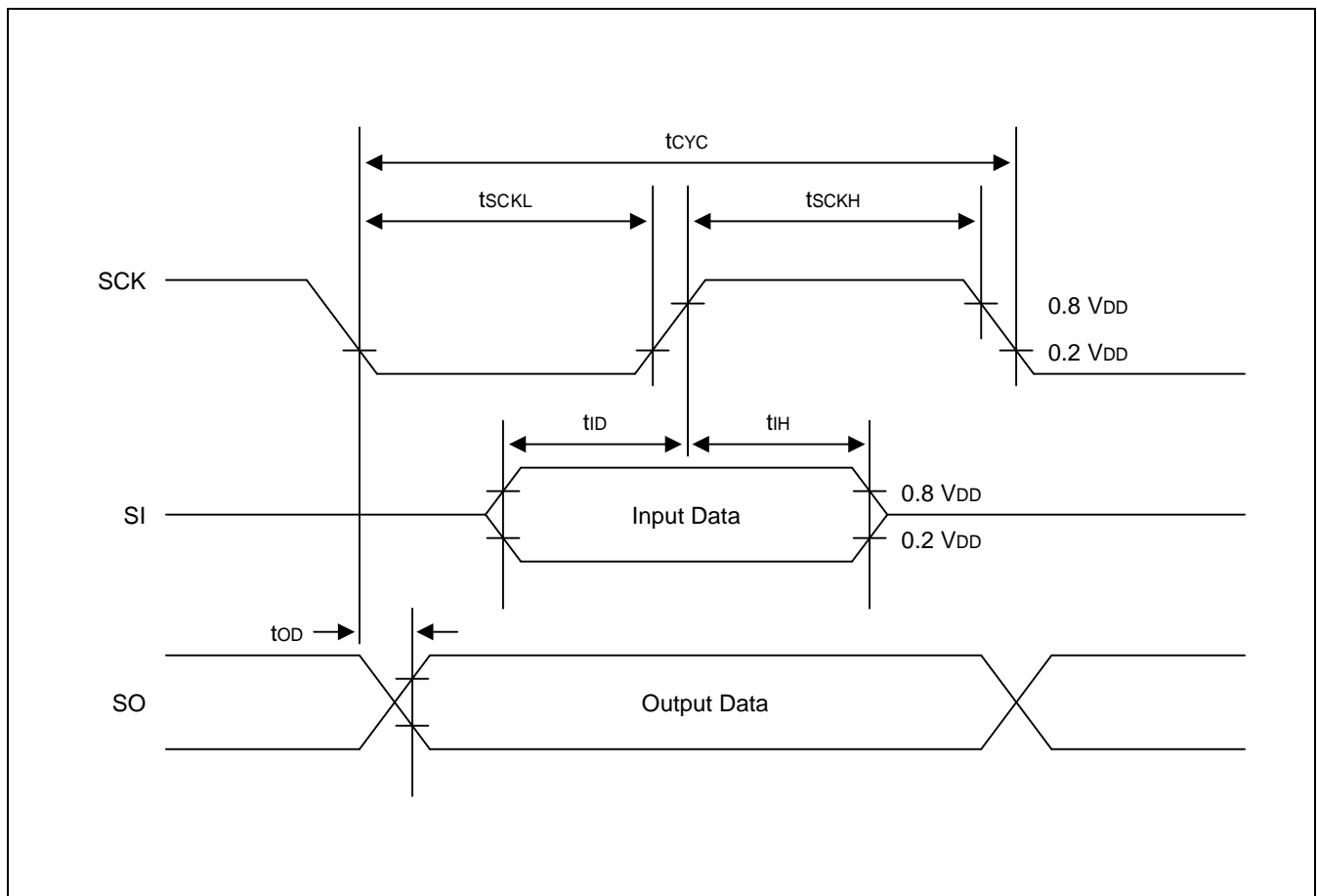


Figure 19-6. Serial Data Transfer Timing

Table 19-9. Main Oscillator Frequency (f_{OSC1})(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

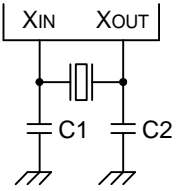
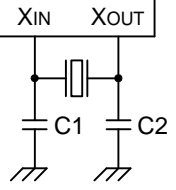
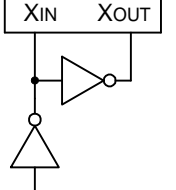
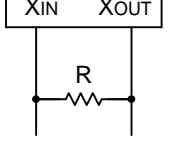
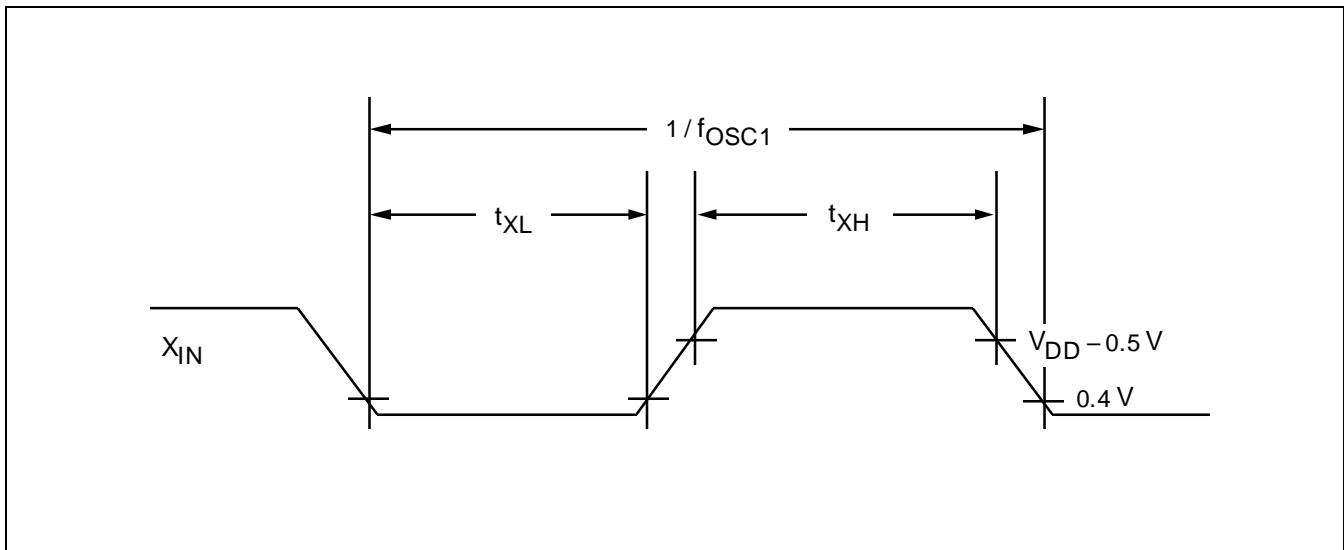
Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Crystal		Crystal oscillation frequency	1	–	10	MHz
Ceramic		Ceramic oscillation frequency	1	–	10	MHz
External clock		X _{IN} input frequency	1	–	10	MHz
RC		r = 35 kΩ, V _{DD} = 5 V		2		MHz

Table 19-10. Main Oscillator Clock Stabilization Time (t_{ST1})(T_A = -40 °C to +85 °C, V_{DD} = 4.5 V to 5.5 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Crystal	V _{DD} = 4.5 V to 5.5 V	–	–	10	ms
Ceramic	Stabilization occurs when V _{DD} is equal to the minimum oscillator voltage range.	–	–	4	ms
External clock	X _{IN} input high and low level width (t _{XH} , t _{XL})	50	–	–	ns

NOTE: Oscillation stabilization time (t_{ST1}) is the time required for the CPU clock to return to its normal oscillation frequency after a power-on occurs, or when Stop mode is ended by a RESET signal. The RESET should therefore be held at low level until the t_{ST1} time has elapsed

Figure 19-7. Clock Timing Measurement at X_{IN} Table 19-11. Sub Oscillator Frequency (f_{OSC2})

($T_A = -40\text{ }^{\circ}\text{C} + 85\text{ }^{\circ}\text{C}$, $V_{DD} = 1.8\text{ V to } 5.5\text{ V}$)

Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Crystal		Crystal oscillation frequency $C1 = 22\text{ pF}$, $C2 = 33\text{ pF}$ $R = 39\text{ Kohm}$ XT_{IN} and XT_{OUT} are connected with R and C by soldering.	32	32.768	35	kHz

Table 19-12. Sub Oscillator(crystal) Stabilization Time (t_{ST2})

($T_A = 25\text{ }^{\circ}\text{C}$)

Oscillator	Test Condition	Min	Typ	Max	Unit
normal mode	$V_{DD} = 4.5\text{ V to } 5.5\text{ V}$	–	250	500	ms
	$V_{DD} = 1.8\text{ V to } 3.0\text{ V}$	–	–	2	s
strong mode	$V_{DD} = 4.5\text{ V to } 5.5\text{ V}$	–	–	2	s
	$V_{DD} = 1.8\text{ V to } 3.0\text{ V}$	–	250	500	ms

NOTE: Oscillation stabilization time (t_{ST2}) is the time required for the oscillator to its normal oscillation when stop mode is released by interrupts. The value Typ and Max are measured by buzzer output signal after stop release. For example in voltage range of 4.5 V to 5.5 V of normal mode, we can see the buzzer output signal within 400 ms at our test condition.

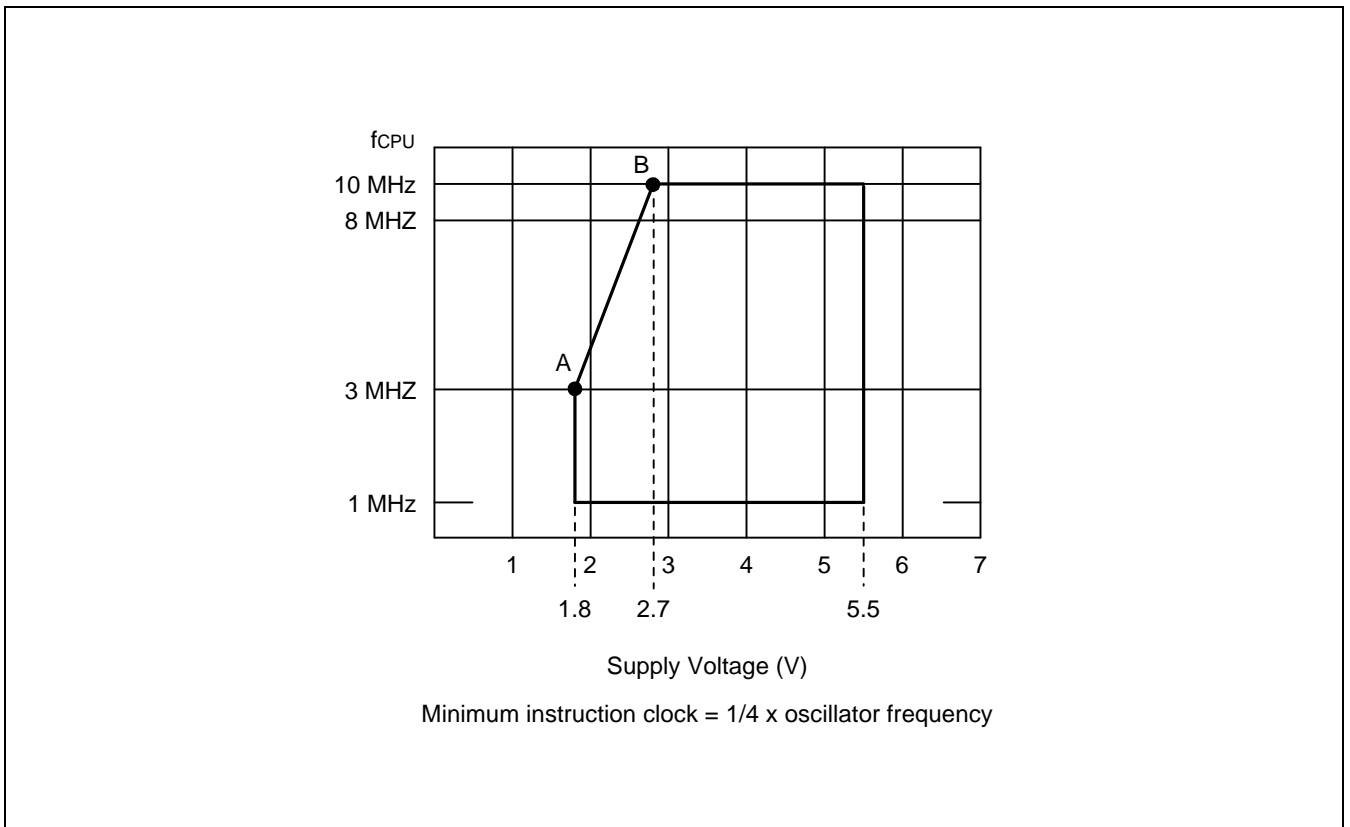


Figure 19-8. Operating Voltage Range

20 MECHANICAL DATA

OVERVIEW

The KS88C2416/C2432 microcontroller is currently available in 80-pin QFP package.

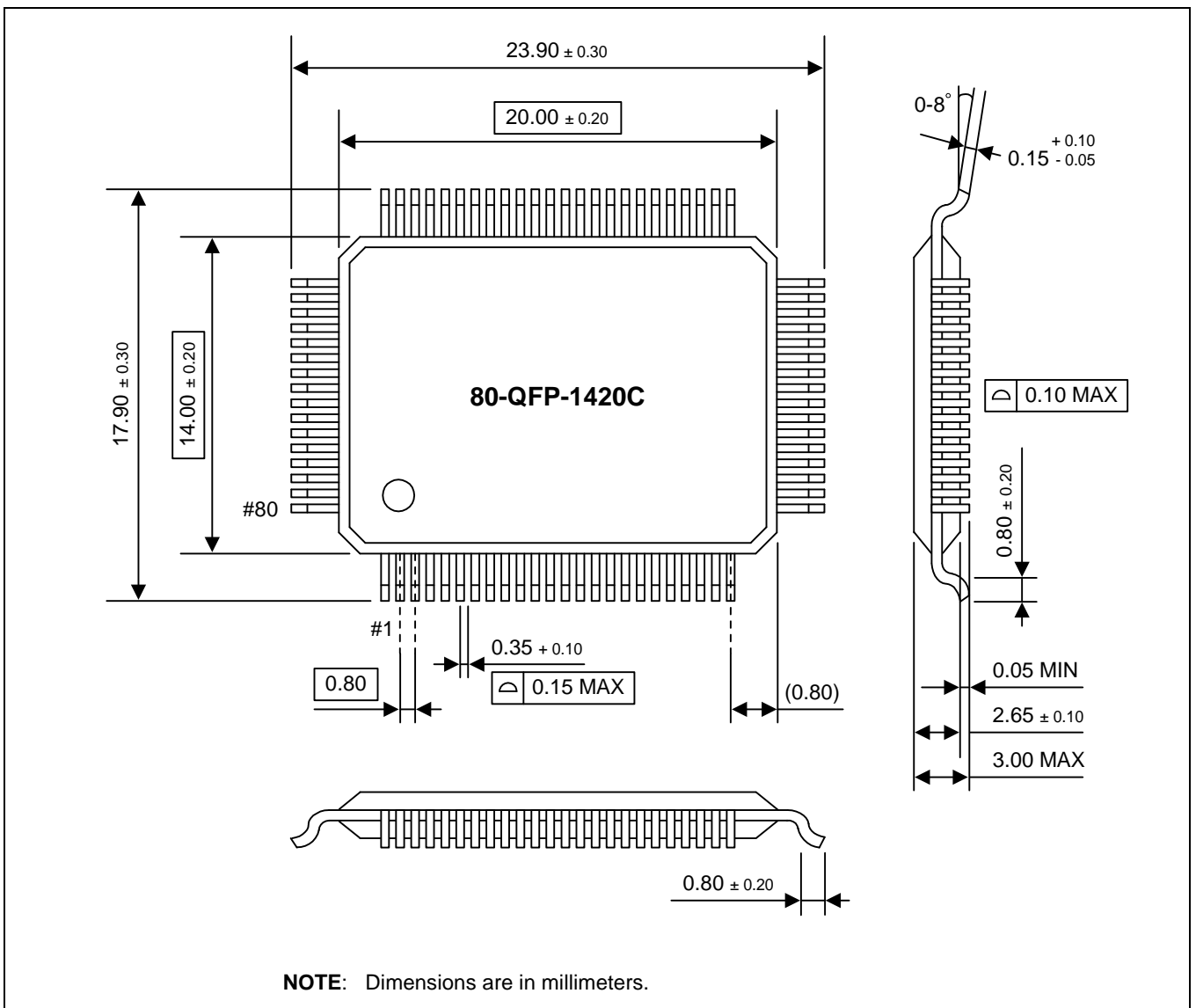


Figure 20-1. 80-Pin QFP 1420C Package Dimensions

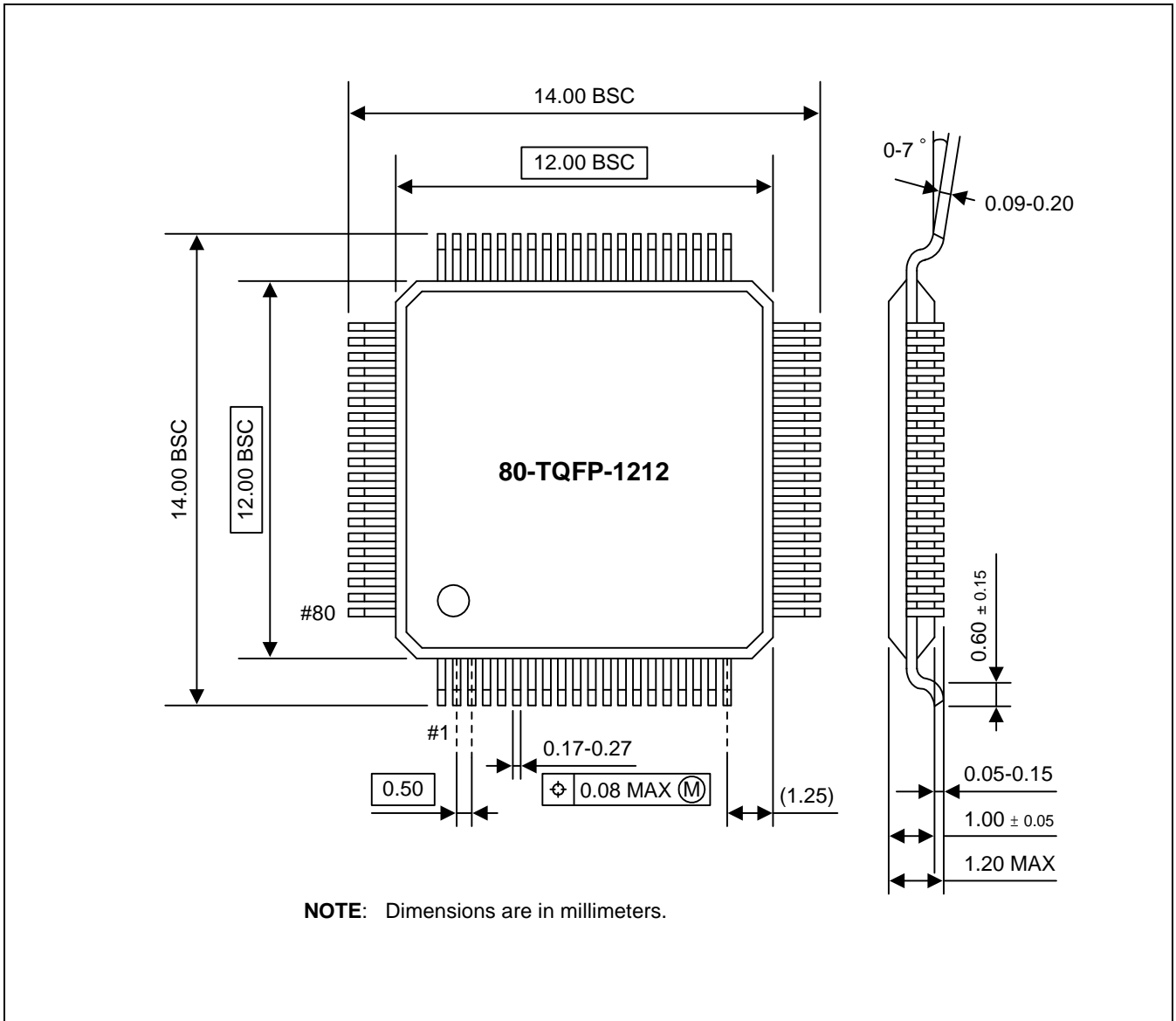


Figure 20-2. 80-Pin TQFP 1212 Package Dimensions

21

KS88P2416/P2432 OTP

OVERVIEW

The KS88P2416/P2432 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the KS88C2416/C2432 microcontroller. It has an on-chip OTP ROM instead of a masked ROM. The EPROM is accessed by serial data format.

The KS88P2416/P2432 is fully compatible with the KS88C2416/C2432, both in function and in pin configuration. Because of its simple programming requirements, the KS88P2416/P2432 is ideal as an evaluation chip for the KS88C2416/C2432.

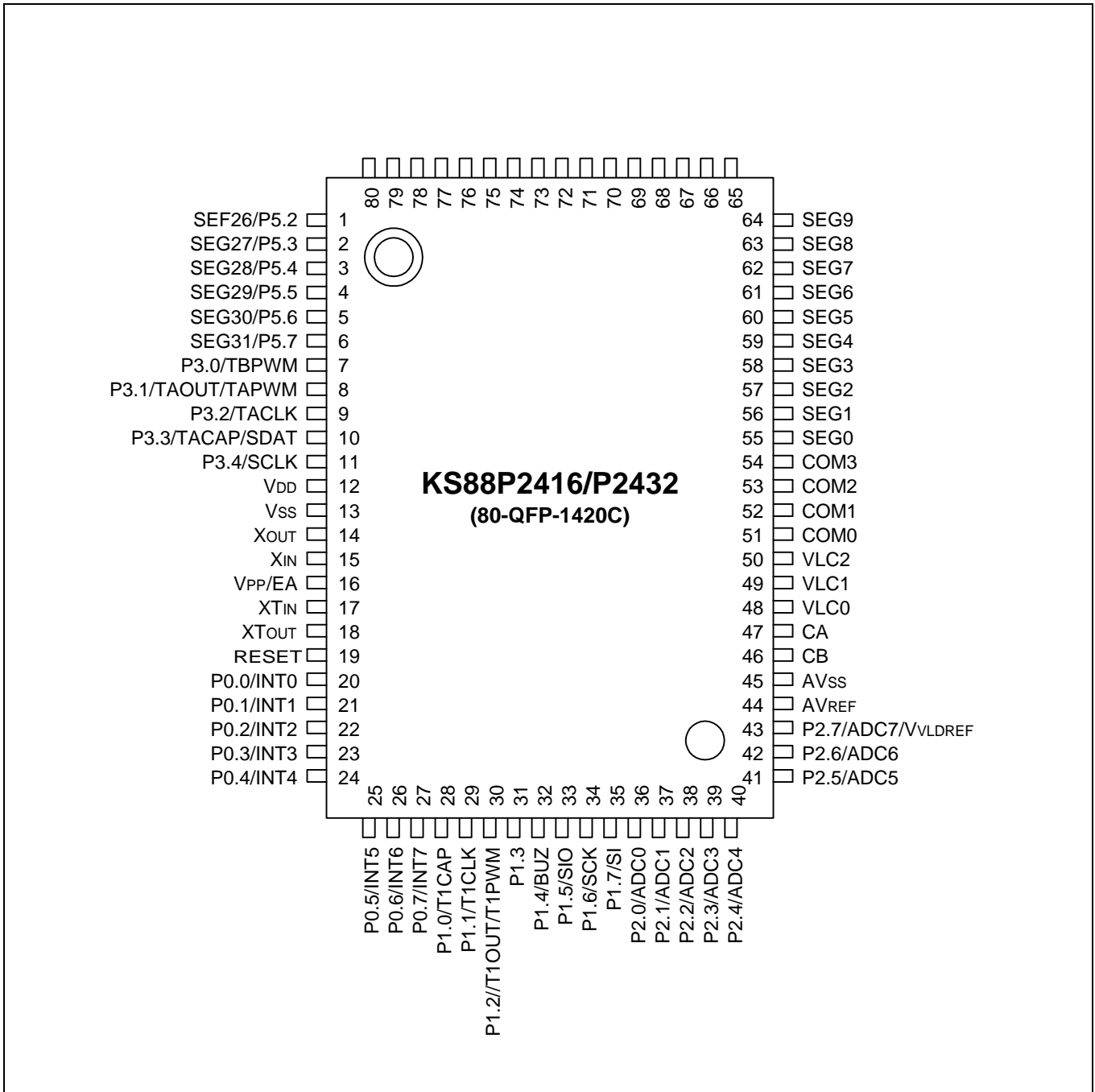


Figure 21-1. KS88P2416/P2432 Pin Assignments (80-QFP Package)

Table 21-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P2.0	SDAT	10	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P2.1	SCLK	11	I/O	Serial clock pin. Input only pin.
V _{PP}	TEST	16	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	19	I	Chip Initialization
V _{DD1} /V _{SS1}	V _{DD1} /V _{SS1}	12/13	–	Logic power supply pin. V _{DD} should be tied to +5 V during programming.

Table 21-2. Comparison of KS88P2416/P2432 and KS88C2416/C2432 Features

Characteristic	KS88P2416/P2432	KS88C2416/C2432
Program Memory	16 K/32 Kbyte EPROM	16 K/32 Kbyte mask ROM
Operating Voltage (V _{DD})	1.8 V to 5.5 V	1.8 V to 5.5 V
OTP Programming Mode	V _{DD} = 5 V, V _{PP} (TEST) = 12.5 V	
Pin Configuration	80 QFP/80 TQFP	80 QFP/80 TQFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (TEST) pin of the KS88P2416/P2432, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 21-3 below.

Table 21-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG/ MEM	Address (A15–A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

Table 21-4. D.C Electrical Characteristics

($T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating voltage	V_{DD}	$f_{CPU} = 10\text{ MHz}$	2.7	–	5.5	V
		All input pins except $V_{IH2, 3}$	1.8	–	5.5	
Input high voltage	V_{IH1}	Port 4,5 $V_{LCD2} \geq V_{DD}$	$0.8 V_{DD}$	–	V_{DD}	
	V_{IH2}	X_{IN}, XT_{IN}	$0.8 V_{DD}$	–	V_{DD}	
	V_{IH3}	All input pins except V_{IL2}	$V_{DD} - 0.1$	–	V_{DD}	
Input low voltage	V_{IL1}	X_{IN}, XT_{IN}	–	–	$0.2 V_{DD}$	
	V_{IL2}	$V_{DD} = 5\text{ V}; I_{OH} = -1\text{ mA}$ All output pins			0.1	
Output high voltage	V_{OH}	$V_{DD} = 5\text{ V}; I_{OL} = 2\text{ mA}$ All output pins	$V_{DD} - 1.0$	–	–	
Output low voltage	V_{OL}		–	–	0.4	

Table 21-4. D.C. Electrical Characteristics (Continued)

(T_A = -40 °C to +85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high leakage current	I _{LIH1}	V _{IN} = V _{DD} All input pins except I _{LIH2}	-	-	3	uA
	I _{LIH2}	V _{IN} = V _{DD} X _{IN} , XT _{IN}			20	
Input low leakage current	I _{LIL1}	V _{IN} = 0 V All input pins except I _{LIL2}	-	-	-3	
	I _{LIL2}	V _{IN} = 0 V X _{IN} , XT _{IN} , RESET			-20	
Output high leakage current	I _{LOH}	V _{OUT} = V _{DD} All I/O pins and Output pins	-	-	3	
Output low leakage current	I _{LOL}	V _{OUT} = 0 V All I/O pins and Output pins	-	-	-3	
Oscillator feed back resistors	R _{osc1}	V _{DD} = 5.0 V T _A = 25 °C X _{IN} = V _{DD} , X _{OUT} = 0 V	800	1000	1200	
Pull-up resistor	R _{L1}	V _{IN} = 0 V; V _{DD} = 5 V ±10 % Port 0,1,2,3,4,5 T _A = 25 °C	25	50	100	
	R _{L2}	V _{IN} = 0 V; V _{DD} = 5 V ±10% T _A =25 °C, RESET only	110	210	310	
V _{LC0} out voltage (Booster run mode)	V _{LC0}	T _A = 25 °C (1/3 bias mode)	0.9	1.0	1.1	V
		T _A = 25 °C (1/2 bias mode)	1.4	1.5	1.7	
V _{LC1} out voltage (Booster run mode)	V _{LC1}	T _A = 25 °C	2V _{LC0} - 0.1	-	2V _{LC0} + 0.1	
V _{LC2} out voltage (Booster run mode)	V _{LC2}	T _A = 25 °C	3V _{LC0} - 0.1	-	3V _{LC0} + 0.1	
COM output voltage deviation	V _{DC}	V _{DD} = V _{LC2} = 3 V (V _{LC} -COMi) IO = ± 15 μA (1 = 0-3)	-	± 60	± 120	mV
SEG output voltage deviation	V _{Ds}	V _{DD} = V _{LC2} = 3 V (V _{LC} -COMi) IO = ± 15 μA (1 = 0-3)	-	± 60	± 120	

Table 21-4. D.C. Electrical Characteristics (Concluded)

(T_A = -40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
Supply current ⁽¹⁾	I _{DD1} ⁽²⁾	V _{DD} = 5 V ± 10 % 10 MHz crystal oscillator	-	12	25	mA	
		3 MHz crystal oscillator		4	10		
		V _{DD} = 3 V ± 10 % 10 MHz crystal oscillator		3	8		
		3 MHz crystal oscillator		1	5		
	I _{DD2}	Idle mode: V _{DD} = 5 V ± 10 % 10 MHz crystal oscillator	-	3	10		
		3 MHz crystal oscillator		1.5	4		
		Idle mode: V _{DD} = 3 V ± 10 % 10 MHz crystal oscillator		1.2	3		
		3 MHz crystal oscillator		0.5	1.5		
	I _{DD3}	Sub operating: main-osc stop V _{DD} = 3 V ± 10 % 32768 Hz crystal oscillator	-	-	20	40	uA
	I _{DD4}	Sub idle mode: main-osc stop V _{DD} = 3 V ± 10 % 32768 Hz crystal oscillator	-	-	7	14	
I _{DD5}	Main stop mode : sub-osc stop V _{DD} = 5 V ± 10 %	-	-	1	3		
				V _{DD} = 3 V ± 10 %	0.5		2

NOTES:

- Supply current does not include current drawn through internal pull-up resistors or external output current loads.
- I_{DD} and I_{DD2} include a power consumption of subsystem oscillator.
- I_{DD3} and I_{DD4} are the current when the mainsystem clock oscillation stop and the subsystem clock is used.
- I_{DD5} is the current when the main and subsystem clock oscillation stop.

case of KS88P2416, the characteristic of V_{OH} and V_{OL} is differ with the characteristic of KS88P2432 like as bellow. Other characteristics are same each other.

Table 21-5. D.C Electrical Characteristics of KS88C2416

($T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output high voltage	V_{OH1}	$V_{DD} = 5\text{ V}$; $I_{OH} = -1\text{ mA}$ All output pins except V_{OH2}	$V_{DD}-1.0$	–	–	V
	V_{OH2}	$V_{DD} = 5\text{ V}$; $I_{OH} = -6\text{ mA}$ Port 3.0 only in KS88P2416	$V_{DD}-0.7$			
Output low voltage	V_{OL1}	$V_{DD} = 5\text{ V}$; $I_{OL} = 2\text{ Ma}$ All output pins except V_{OL2}	–	–	0.4	
	V_{OL2}	$V_{DD} = 5\text{ V}$; $I_{OH} = 12\text{ mA}$ Port 3.0 only in KS88P2416			0.7	

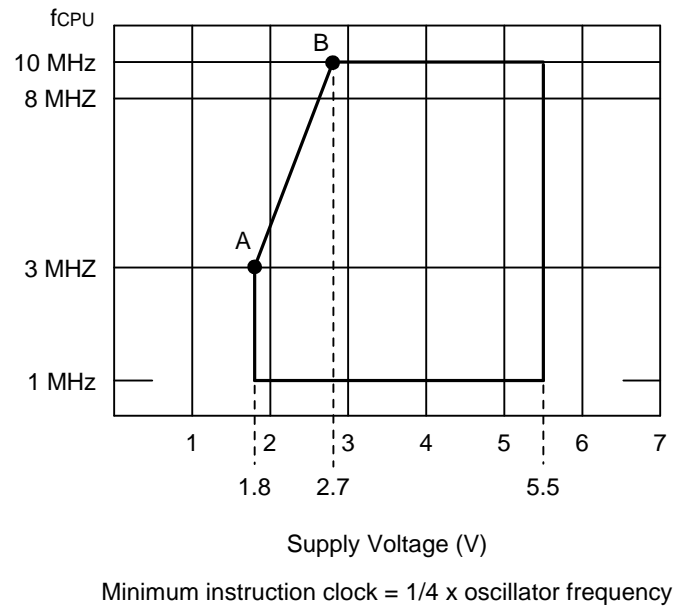


Figure 21-2. Operating Voltage Range