



High Performance Communication Buffer

General Description

The **ICS91309** is a high performance, low skew, low jitter zero delay buffer. It uses a phase lock loop (PLL) technology to align, in both phase and frequency, the REF input with the CLKOUT signal. It is designed to distribute high speed clocks in communication systems operating at speeds from 10 to 133 MHz.

The **ICS91309** provides synchronization between the input and output. The synchronization is established via CLKOUT feed back to the input of the PLL. Since the skew between the input and output is less than +/- 350 pS, the part acts as a zero delay buffer.

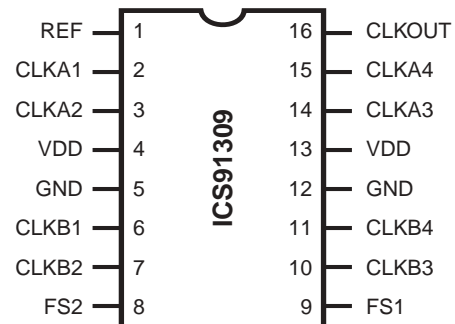
ICS91309 has two banks of four outputs controlled by two address lines. Depending on the selected address line, bank B or both banks can be put in a tri-state mode. In this mode, the PLL is still running and only the output buffers are put in a high impedance mode. The test mode shuts off the PLL and connects the input directly to the output buffers (see table below for functionality).

ICS91309 comes in a 16-pin 150 mil SOIC, SSOP or 4.40mm TSSOP package. In the absence of REF input, the device will enter a powerdown mode. In this mode, the PLL is turned off and the output buffers are pulled low. Power down mode provides the lowest power consumption for a standby condition.

Features

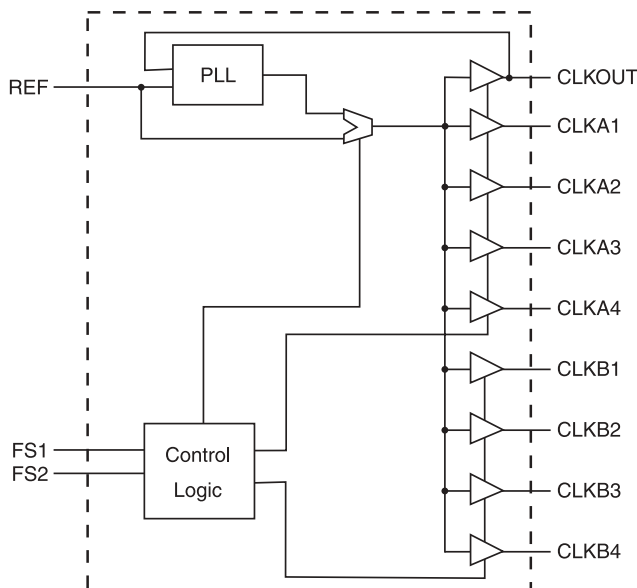
- Zero input - output delay
- Frequency range 10 - 133 MHz (3.3V)
- 5V tolerant input REF
- High loop filter bandwidth ideal for Spread Spectrum applications.
- Less than 125 ps cycle to cycle Jitter
- Skew controlled outputs
- Available in 16 pin, 150 mil SSOP, SOIC & 4.40mm TSSOP packages
- Skew: Group-to-Group: <215 ps
- Skew within Group: <100 ps
- Commercial temperature range: 0°C to +70°C

Pin Configuration



16 pin SSOP, SOIC & TSSOP

Block Diagram



Functionality

| FS2 | FS1 | CLKA(1:4) | CLKB(1:4) | CLKOUT | Ouput Source | PLL Shutdown |
|-----|-----|-----------------|-----------------|-----------------|--------------|--------------|
| 0 | 0 | Tristate | Tristate | Driven | PLL | N |
| 0 | 1 | Driven | Tristate | Driven | PLL | N |
| 1 | 0 | PLL Bypass Mode | PLL Bypass Mode | PLL Bypass Mode | REF | Y |
| 1 | 1 | Driven | Driven | Driven | PLL | N |



Pin Descriptions

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|---------------------|----------|--|
| 1 | REF ¹ | IN | Input reference frequency, 5V tolerant input |
| 2 | CLKA1 ² | OUT | Buffered clock output, Bank A |
| 3 | CLKA2 ² | OUT | Buffered clock output, Bank A |
| 4, 13 | VDD | PWR | Power Supply |
| 5, 12 | GND | PWR | Ground |
| 6 | CLKB1 ² | OUT | Buffered clock output, Bank B |
| 7 | CLKB2 ² | OUT | Buffered clock output, Bank B |
| 8 | FS2 ³ | IN | Function select input, bit 2 |
| 9 | FS1 ³ | IN | Function select input, bit 1 |
| 10 | CLKB3 ² | OUT | Buffered clock output, Bank B |
| 11 | CLKB4 ² | OUT | Buffered clock output, Bank B |
| 14 | CLKA3 ² | OUT | Buffered clock output, Bank A |
| 15 | CLKA4 ² | OUT | Buffered clock output, Bank A |
| 16 | CLKOUT ² | OUT | Buffered clock output, internal feedback |

Notes:

1. Weak pull-down
2. Weak pull-down on all outputs
3. Weak pull-ups on these inputs



Absolute Maximum Ratings

- Supply Voltage 7.0 V
- Logic Inputs (Except REF) GND -0.5 V to V_{DD} + 0.5 V
- Logic Input REF GND -0.5 V to GND + 5.5 V
- Ambient Operating Temperature 0°C to +70°C
- Storage Temperature -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input & Supply

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-10%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-----------------|-----------------------------------|-----|-----|-----|-------|
| Input High Voltage | V _{IH} | | 2 | | | V |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | | 0.1 | 100 | uA |
| Input Low Current | I _{IL} | V _{IN} = 0 V | | 19 | 50 | uA |
| Output High Voltage | V _{OH} | I _{OH} = -12 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 12 mA | | | 0.4 | V |
| Operating Supply Current | I _{DD} | Outputs Unloaded; REF = 66 MHz | | 30 | 45 | mA |
| Powerdown Current | I _{DD} | REF = 0 Mhz | | 0.3 | 12 | uA |
| Input Frequency | F _i | | 10 | | 133 | MHz |
| Input Capacitance ¹ | C _{IN} | | | | 5 | pF |

NOTES:

1. Guaranteed by design and characterization, not 100% tested in production.



Electrical Characteristics - Outputs

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 10\%$; $C_L = 30\text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|---------------|--|------|-----|-----|-------|
| Output High Voltage | V_{OH} | $I_{OH} = -12\text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL} | $I_{OL} = 12\text{ mA}$ | | | 0.4 | V |
| Rise Time ¹ | t_r | Measure between 0.8 V and 2.0 V | | 1.2 | 1.5 | ns |
| Fall Time ¹ | t_f | Measure between 2.0 V and 0.8 V | | 1.2 | 1.5 | ns |
| PLL Lock Time ¹ | T_{LOCK} | Stable V_{DD} , valid clock on REF | | | 1 | mS |
| Output Frequency | f_i | $C_L = 30\text{ pF}$ | 10 | | 100 | MHz |
| | f_i | $C_L = 10\text{ pF}$ | 10 | | 133 | MHz |
| Duty Cycle ¹ | Dt1 | Measured at 1.4 V, $F_{out} = 66.7\text{ MHz}$ | 40 | 50 | 60 | % |
| | Dt2 | Measured at $V_{DD}/2$, $F_{out} < 50.0\text{ MHz}$ | 45 | 50 | 55 | % |
| Jitter, Cycle-to-cycle ¹ | $t_{jcy-cyc}$ | Measured at 66.7 MHz, loaded outputs | | | 125 | ps |
| Jitter, Absolute ¹ | Tjabs | 10,000 cycles, $C_L = 30\text{ pF}$ | -100 | 70 | 100 | ps |
| Jitter, 1-Sigma ¹ | Tj1s | 10,000 cycles, $C_L = 30\text{ pF}$ | | 14 | 30 | ps |
| Skew, Group-to-Group ¹ | Tsk | Measured at 1.4 V | | | 215 | ps |
| Skew, Output-to-Output ¹ | Tsk | Measured at 1.4 V, within a group | | | 100 | ps |
| Skew, Device-to-Device ¹ | Tdsk-Tdsk | Measured at $V_{DD}/2$, on CLKOUT pins | | | 700 | ps |
| Delay, Input-to-Output ¹ | Dr1 | Measured at 1.4 V | | | 700 | ps |

Notes:

1. Guaranteed by design and characterization, not 100% tested in production.



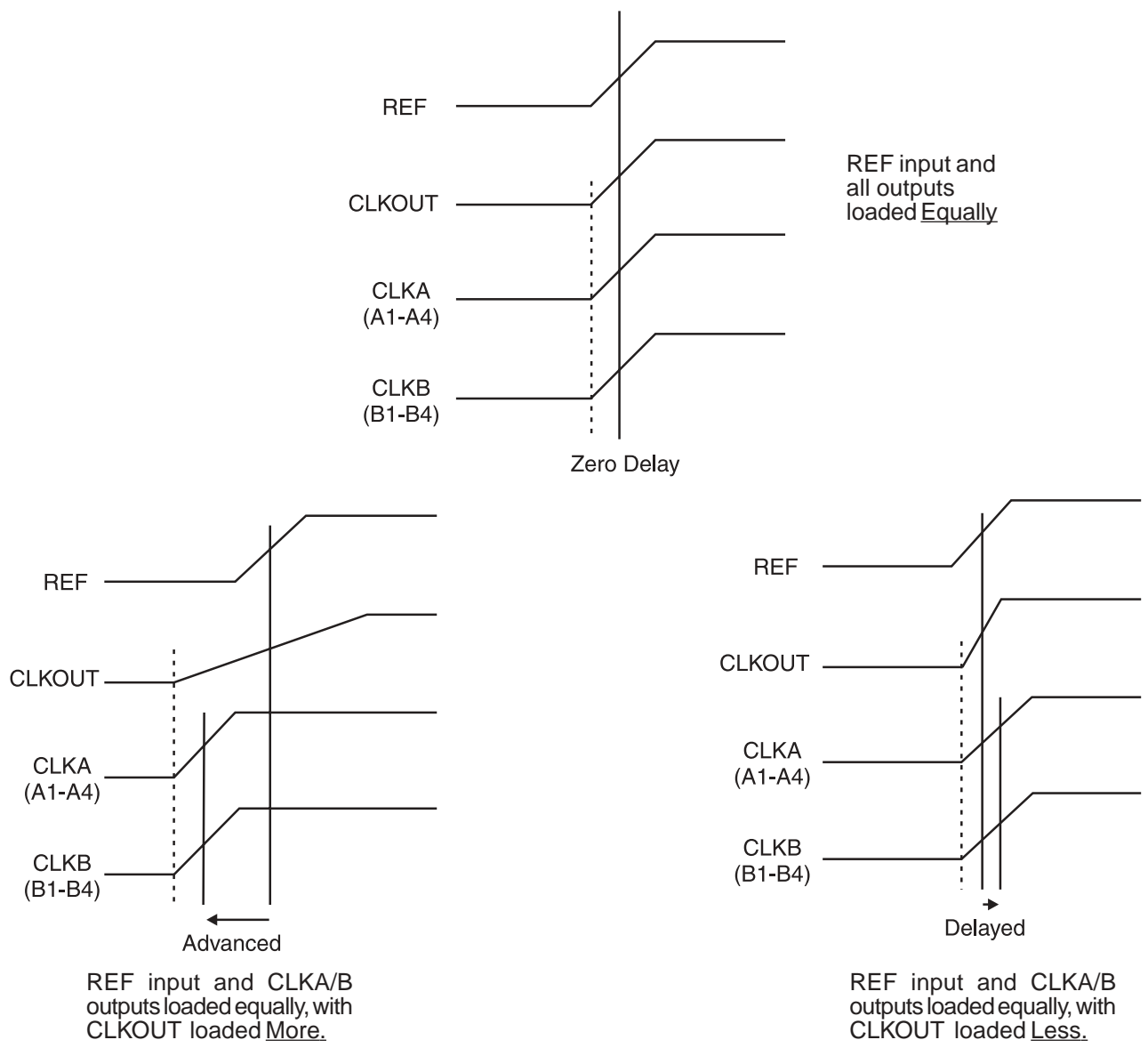
Output to Output Skew

The skew between CLKOUT and the CLKA/B outputs is not dynamically adjusted by the PLL. Since CLKOUT is one of the inputs to the PLL, zero phase difference is maintained from REF to CLKOUT. If all outputs are equally loaded, zero phase difference will be maintained from REF to all outputs.

If applications requiring zero output-to-output skew, all the outputs must be equally loaded.

If the CLKA/B outputs are less loaded than CLKOUT, CLKA/B outputs will lead it; and if the CLKA/B is more loaded than CLKOUT, CLKA/B will lag the CLKOUT.

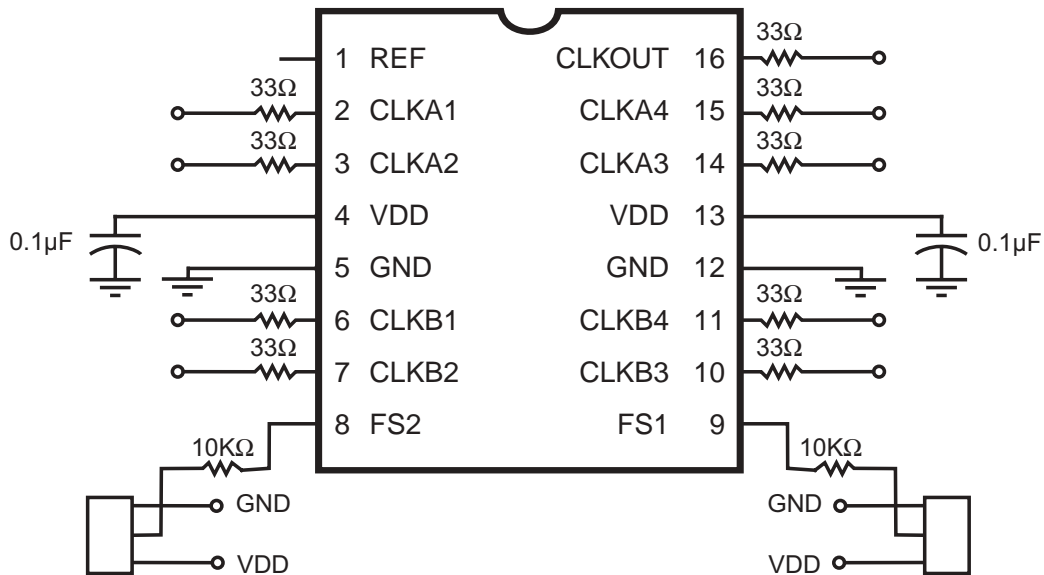
Since the CLKOUT and the CLKA/B outputs are identical, they all start at the same time, but different loads cause them to have different rise times and different times crossing the measurement thresholds.

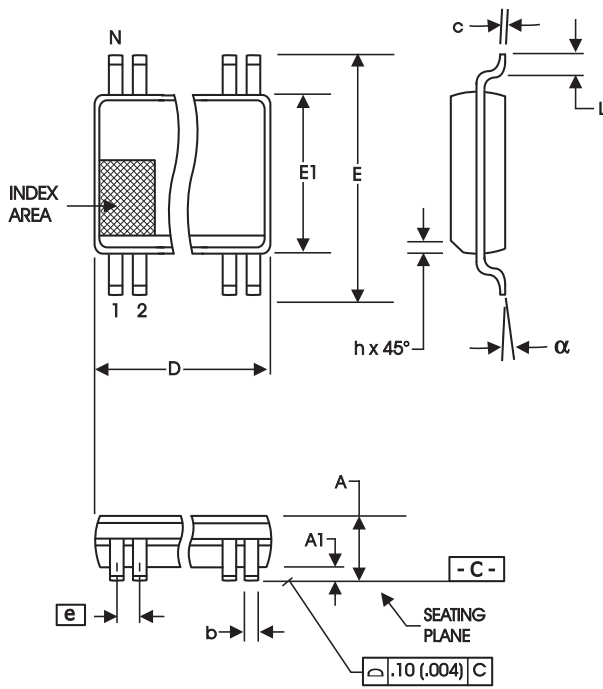




Application Suggestion:

ICS91309 is a mixed analog/digital product. The analog portion of the PLL is very sensitive to any random noise generated by charging or discharging of internal or external capacitor on the power supply pins. This type of noise will cause excess jitter to the outputs of **ICS91309**. Below is a recommended layout to alleviate any addition noise. For additional information on FT. layout, please refer to our AN07. The 0.1 uF capacitors should be connected as close as possible to power pins (4 & 13). An Isolated power plane with a 2.2 uF capacitor to ground will enhance the power line stability.





| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|--------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | .053 | .069 |
| A1 | 0.1 | 0.25 | .0040 | .010 |
| A2 | — | 1.50 | — | .059 |
| b | 0.20 | 0.30 | .008 | .012 |
| c | 0.18 | 0.25 | .007 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 5.80 | 6.20 | .228 | .244 |
| E1 | 3.80 | 4.00 | .150 | .157 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| L | 0.40 | 1.27 | .016 | .050 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| alpha | 0° | 8° | 0° | 8° |
| ZD | SEE VARIATIONS | | SEE VARIATIONS | |

VARIATIONS

| N | D mm. | | ZD | D (inch) | | ZD |
|----|-------|------|-------|----------|------|-------|
| | MIN | MAX | (Ref) | MIN | MAX | (Ref) |
| 16 | 4.80 | 5.00 | 0.23 | .189 | .197 | .009 |

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DOC# 10-0032

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REV B

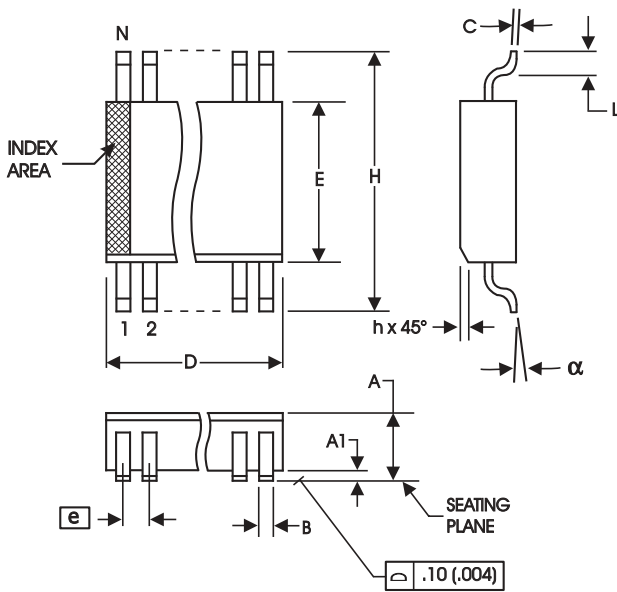
Ordering Information

ICS91309yFLF-T

Example:

ICS XXXX y F LF-T

- Designation for tape and reel packaging
- Lead Free (Optional)
- Package Type
F = SSOP
- Revision Designator (will not correlate with datasheet revision)
- Device Type
- Prefix
ICS = Standard Device



150 mil (Narrow Body) SOIC

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|--------|-------------------------------------|------|--------------------------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | .0532 | .0688 |
| A1 | 0.10 | 0.25 | .0040 | .0098 |
| B | 0.33 | 0.51 | .013 | .020 |
| C | 0.19 | 0.25 | .0075 | .0098 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 3.80 | 4.0 | .1497 | .1574 |
| e | 1.27 BASIC | | 0.050 BASIC | |
| H | 5.80 | 6.20 | .2284 | .2440 |
| h | 0.25 | 0.50 | .010 | .020 |
| L | 0.40 | 1.27 | .016 | .050 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| alpha | 0° | 8° | 0° | 8° |

VARIATIONS

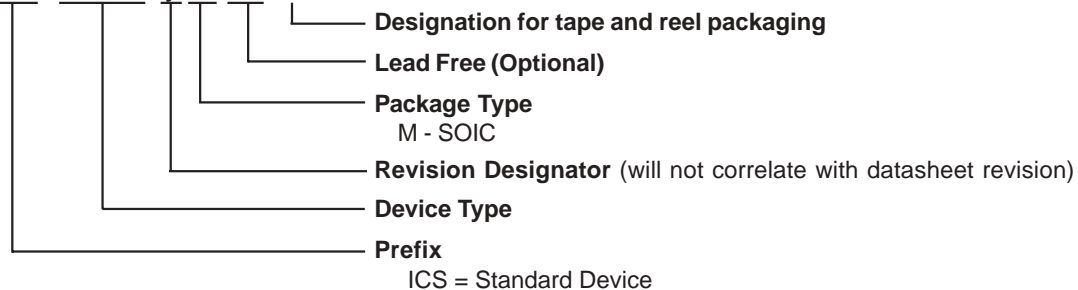
| N | D mm. | | D (inch) | |
|----|-------|-------|----------|-------|
| | MIN | MAX | MIN | MAX |
| 16 | 9.80 | 10.00 | .3859 | .3937 |

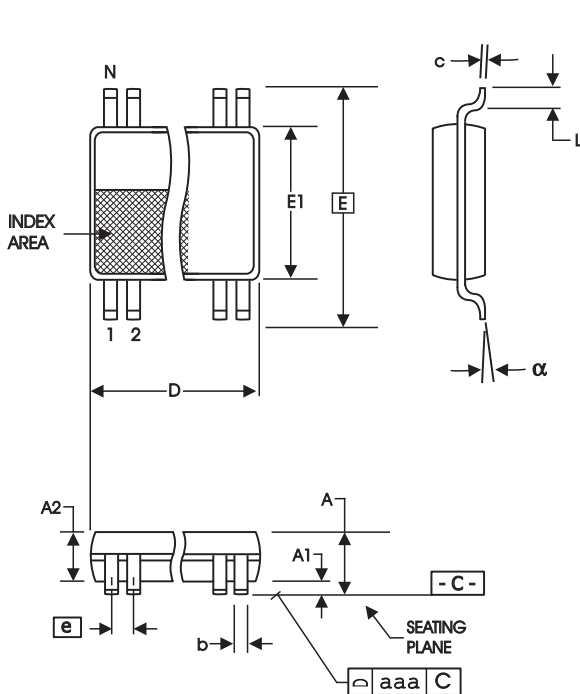
Ordering Information

ICS91309yMLF-T

Example:

ICS XXXX y M LF-T





4.40 mm. Body, 0.65 mm. Pitch TSSOP
(173 mil) (25.6 mil)

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|----------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.19 | 0.30 | .007 | .012 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|------|----------|------|
| | MIN | MAX | MIN | MAX |
| 16 | 4.90 | 5.10 | .193 | .201 |

Reference Doc.: JEDEC Publication 95, MO-153
10-0035

Ordering Information

ICS91309yGLF-T

Example:

ICS XXXX y G LF-T

