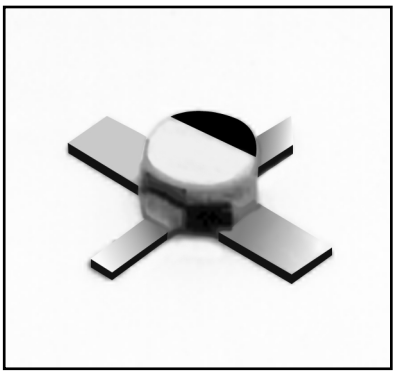
FHX35X/002
FHX35LG/002

Low Noise HEMT

DESCRIPTION

The FHX35X/002 Chip and FHX35LG/002 packaged devices are HEMT (High Electron Mobility Transistor) ones suitable for use as the front end of an optical receiver in high speed lightwave communication systems. This HEMT combines high transconductance, low gate capacitance and low leakage current; all important factors in achieving low noise preamplification. Fujitsu's stringent Quality Assurance criteria and detailed Test Procedures assure Highest Reliabiltity Performance.



LG PACKAGE

FEATURES

- High Transconductance
- Low Leakage Current
- Low Gate Capacitance
- Gold Bonding System
- Proven Reliability

ABSOLUTE MAXIMUM RATINGS (Ambient Temperature T_a=25°C)

Item	Symbol	Conditions	Ratings	Unit
Drain-Source Voltage	V_{DS}		6	V
Gate-Source Voltage	V_{GS}		-5	V
Total Power Dissipation	P_T		290	mW
Storage Temperature	T_{stg}		-65 to 175	°C
Channel Temperature	T_{ch}		+175	°C
Thermal Resistance	R_{th}	Channel to Case	150	°C/W

ELECTRICAL CHARACTERISTICS (Ambient Temperature T_a=25°C)

Item	Symbol	Conditions		Limits Min.	Limits Min.	Limits Max.	Unit
Drain Current	I_{DSS}	V_{DS}=2V, V_{GS}=0V		15	40	85	mA
Transconductance	g_m	V_{DS}=2V, I_{DS}=10mA		45	60	-	mS
Pinch-off Voltage	V_p	V_{DS}=2V, I_{DS}=1mA		-0.2	-1.0	-2.0	V
Gate-Source Leakage Current	I_{GSO}	V_{GS}=-2V		-	10	20	nA
Gate-Source Capacitance	C_{GS}	V_{DS}=3V I_{DS}=10mA	FHX35X/002	-	0.27	-	pF
			FHX35LG/002	-	0.47	-	
Gate-Drain Capacitance	C_{GD}	V_{DS}=3V, I_{DS}=10mA		-	0.035	-	pF

Fig. 1 Drain Current vs. Drain-Source Voltage

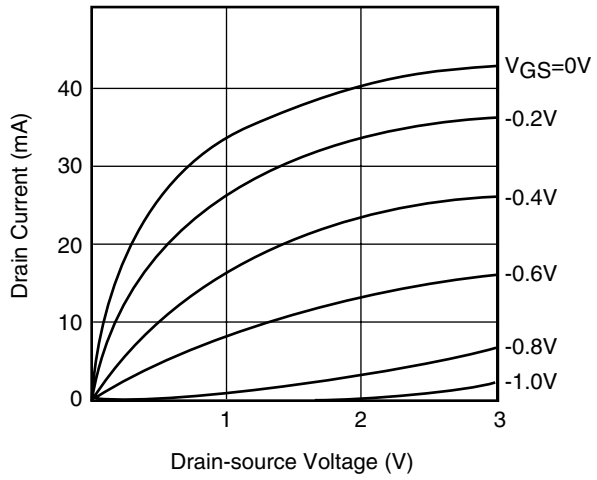


Fig. 2 Gate-Source Capacitance vs. Drain-Source Current

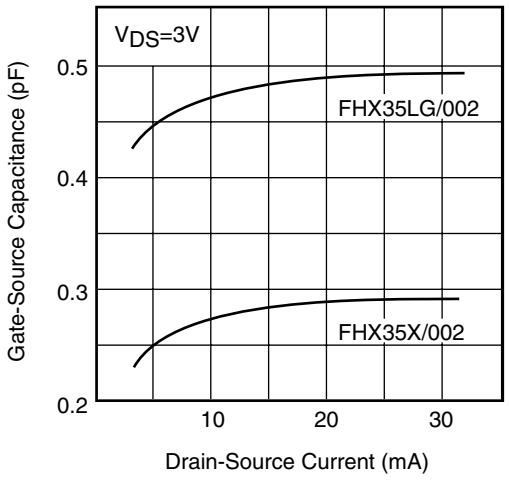


Fig. 3 Transconductance vs. Gate-Source Voltage

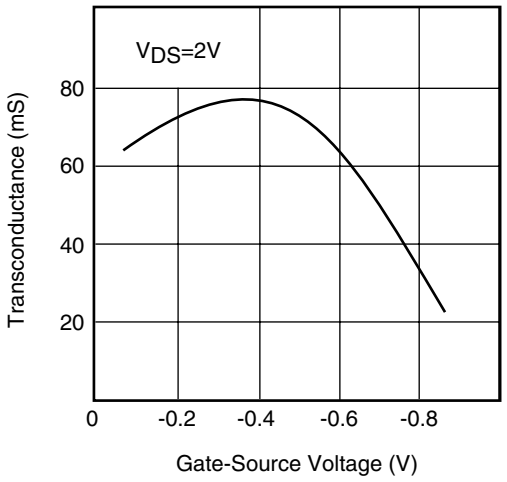
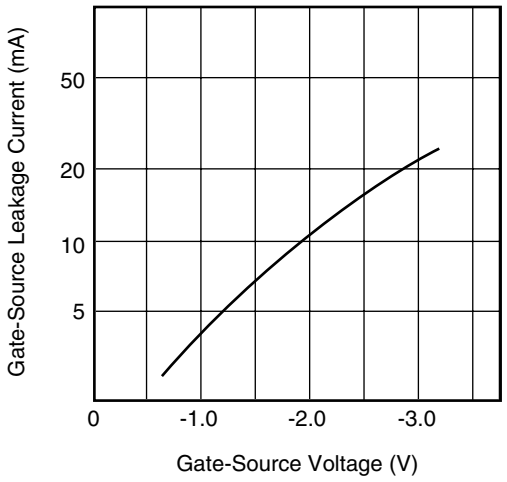


Fig. 4 Gate-Source Leakage Current vs. Gate-Source Voltage



BONDING PROCEDURE FOR FET CHIPs

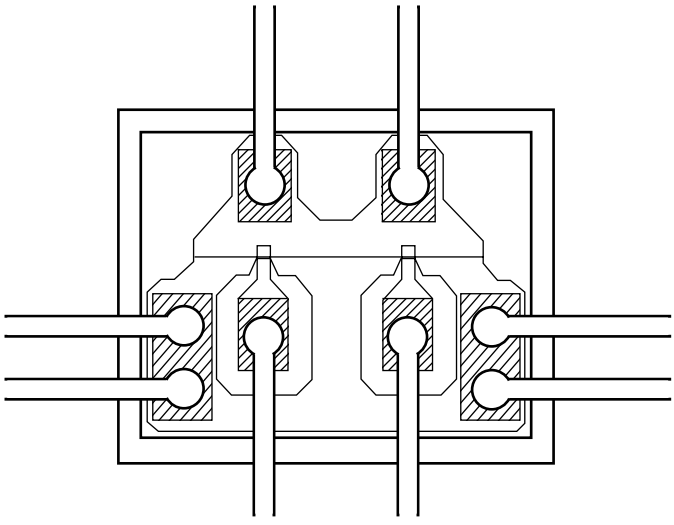
Caution must be excercised to prevent static build up by proper grounding of all equipment and personnel. All operations must be performed in a clean, dust-free and dry environment.

1. Storage Condition: Store in a clean, dry nitrogen environment.
2. Die-Attach
   - 2.1 The die-attach station must have an accurate temperature control, and an inert forming gas should be used.
   - 2.2 Chips should be kept at room temperature, except during die-attach.
   - 2.3 Place package or carrier on the heated stage.
   - 2.4 Place the solder at the position where the chip will be bonded.
   - 2.5 Lightly grasp the chip edges using tweezers and scrub the die onto the Au-Sn solder preform. The die attach conditions are: 300 to 310° for 30 to 60 seconds. The Au-Sn (80-20) solder preform volume should be about 3.2×10^{-3} mm^3 for FHX35X/002.

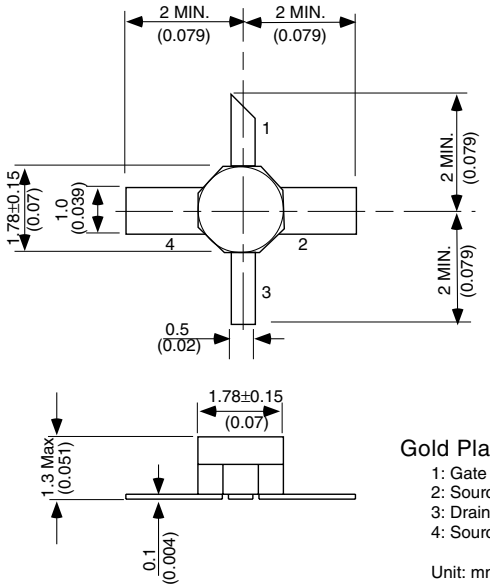
3. Wire Bonding
   - 3.1 Bonding Condition
     The bonder must be properly grounded. Wire bonding should be performed with a thermal compression bonder using 0.7 to 1.0 mil diameter, half hard, 3-8% elongation gold wire.
   - 3.2 Wire Layout
     The wire bonding should be performed as shown in the following example.

Wire Layout

FHX35X/002



Case Style "LG"
Metal-Ceramic Package



Gold Plated Leads
1: Gate
2: Source
3: Drain
4: Source

Unit: mm (Inches)

For further information please contact:

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- **Do not alter the form of this product into a gas, powder, or liquid through burning, crushing, or chemical processing as these by-products are dangerous to the human body if inhaled, ingested, or swallowed.**
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