Features

General

- High-performance, Low-power AVR® (AVR3 Core) Enhanced RISC Architecture
  - 133 Powerful Instructions (Most Executed in a Single Clock Cycle)
- Low-power Idle and Power-down Modes
- Bond Pad Locations Conforming to ISO 7816-2
- ESD Protection to ± 6000V
- Operating Range: from 2.7V to 5.5V
- Compliant with GSM, 3GPP and EMV 2000 Specifications; PC Industry Compatible
- Available in Wafers, Modules and Industry-standard Packages

Memory

- 192K Bytes of ROM Program Memory
- 64K Bytes of EEPROM, Including 128 OTP Bytes and 384-byte Bit-addressable Bytes
  - 1 to 128-byte Program/Erase
  - 2 ms Program, 2 ms Erase
  - Typically More than 300,000 Write/Erase Cycles
  - 10 Years Data Retention
- 6K Bytes of RAM

Peripherals

- ISO 7816 controller
  - Up to 625 kbs at 5 MHz
  - Compliant with T = 0 and T = 1 Protocols
- Two I/O Ports (Configurable to Support Communication Protocols Including 2-wire Interfaces)
- Programmable Internal Oscillator (Up to 16 MHz on ROM)
- Two 16-bit Timers
- Random Number Generator (RNG)
- 2-level, 8-vector Interrupt Controller
- Hardware DES and Triple DES DPA Resistant
- Checksum Accelerator
- CRC 16 Engine (Compliant with ISO/IEC 3309)
- Crypto-coprocessor (Pre-programmed Functions for Cryptography and Authentication Including RSA, DSA, Key Generation, ECC)

Security

- Dedicated Hardware for Protection Against SPA/DPA Attacks
- Advanced Protection Against Physical Attack, Including Active Shield
- Environmental Protection Systems
- Voltage Monitor
- Frequency Monitor
- Secure Memory Management/Access Protection (Supervisor Mode)

Development Tools

- Hardware Development Support on Voyager Emulation Platform (ATV1)
- Software Development Support will be on the AT90SCSIM Software Simulator (Based on IAR Systems' C-Spy® Product)
- Software Libraries and Application Notes

Description

The AT90SC19264RC is the first high-end secure microcontroller based on Atmel's new Secure AVR architecture. The AT90SC19264RC is a low-power, high-perfor-

Secure Microcontroller for Smart Cards

AT90SC19264RC

Summary

Rev. 1563DS–SMIC–08/02

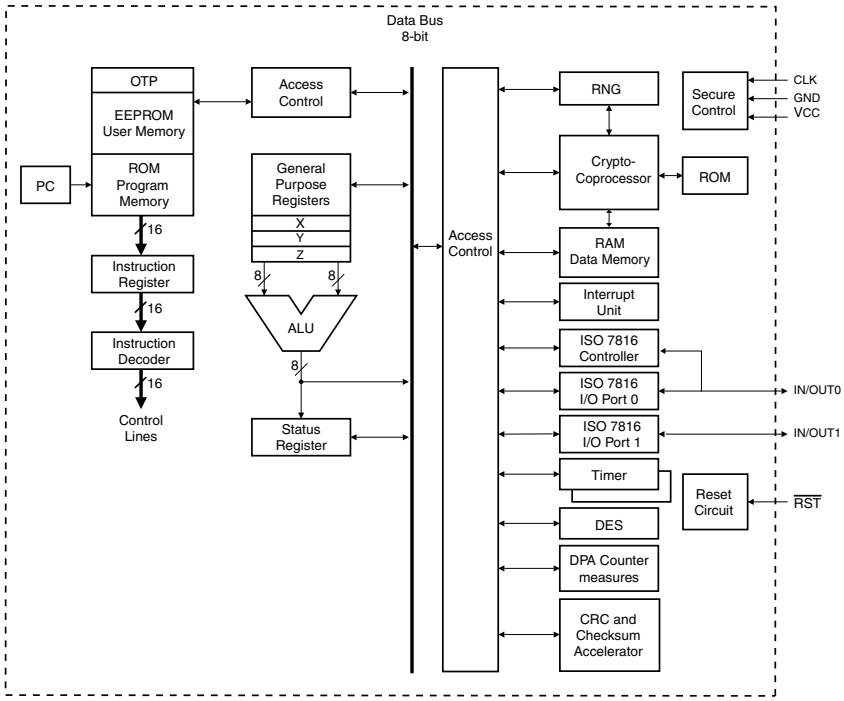
Note: This is a summary document. A complete document is available under NDA. For more information, please contact your local Atmel sales office.

mance, 8-bit microcontroller with ROM program memory, EEPROM data memory and a crypto-coprocessor, based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90SC19264RC achieves throughputs close to 1 MIPS per MHz. Its Harvard architecture includes 32 general-purpose working registers directly connected to the ALU, allowing two independent registers to be accessed in one single instruction executed in one clock cycle.

The AT90SC19264RC uses a new AVR core (core #3) that allows the linear addressing of up to 8M bytes of code and up to 16M bytes of data as well as a number of new functional and security features.

The crypto engine featured in the AT90SC series is a 16-bit processor dedicated to perform fast encryption or authentication functions. Additional security features include power and frequency protection logic, logical scrambling on program data and addresses, Power Analysis countermeasures and memory accesses controlled by a supervisor mode.

Figure 1. The AT90SC19264RC AVR Enhanced RISC Architecture



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