400KHz 2-Wire Serial E²PROM with Block Lock™

FEATURES

- **Save Critical Data with Programmable Block Lock Protection**
  - **—Block Lock (first page, first 2 pages, first 4 pages, first 8 pages, 1/4, 1/2, or all of E²PROM Array)**
  - **—Software Write Protection**
  - **—Programmable Hardware Write Protect**
- **In Circuit Programmable ROM Mode**
- **400KHz 2-Wire Serial Interface**
  - **—Schmitt Trigger Input Noise Suppression**
  - **—Output Slope Control for Ground Bounce Noise Elimination**
- **Longer Battery Life With Lower Power**
  - **—Active Read Current Less Than 1mA**
  - **—Active Write Current Less Than 3mA**
  - **—Standby Current Less Than 1μA**
- **1.8V to 3.6V, 2.5V to 5.5V and 4.5V to 5.5V Power Supply Versions**
- **64 Byte Page Write Mode**
  - **—Minimizes Total Write Time Per Word**
- **Internally Organized 32K x 8**
- **Bidirectional Data Transfer Protocol**
- **Self-Timed Write Cycle**
  - **—Typical Write Cycle Time of 5ms**
- **High Reliability**
  - **—Endurance: 100,000 Cycles**
  - **—Data Retention: 100 Years**
- **8-Lead XBGA, 8-Lead SOIC, 14-Lead TSSOP**

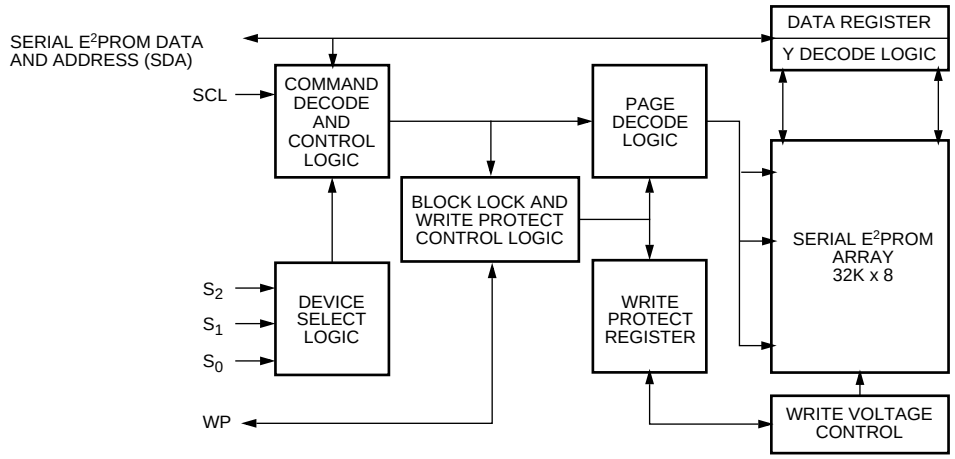
DESCRIPTION

The X24257 is a CMOS Serial E²PROM, internally organized 32K x 8. The device features a serial interface and software protocol allowing operation on a simple two wire bus.

Three device select inputs (S_0–S_2) allow up to eight devices to share a common two wire bus.

A Write Protect Register at the highest address location, FFFFh, provides three write protection features: Software Write Protect, Block Lock Protect, and Programmable Hardware Write Protect. The Software Write Protect feature prevents any nonvolatile writes to the device until the WEL bit in the Write Protect Register is set. The Block Lock Protection feature gives the user eight array block protect options, set by programming three bits in the Write Protect Register. The Programmable Hardware Write Protect feature allows the user to install the device with WP tied to V_{CC}, write to and Block Lock the desired portions of the memory array in circuit, and then enable the In Circuit Programmable ROM Mode by programming the WPEN bit HIGH in the Write Protect Register. After this, the Block Locked portions of the array, including the Write Protect Register itself, are protected from being erased if WP is high.

FUNCTIONAL DIAGRAM



Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-up resistor selection graph at the end of this data sheet.

Device Select (S_0, S_1, S_2)

The device select inputs (S_0, S_1, S_2) are used to set bits in the slave address. This allows up to eight devices to share a common bus. These inputs can be static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If actively driven, they must be driven with CMOS levels (driven to V_{CC} or V_{SS}) and they must be constant between each start and stop issued on the SDA bus. These pins have an active pull down internally and will be sensed as low if the pin is left unconnected.

Write Protect (WP)

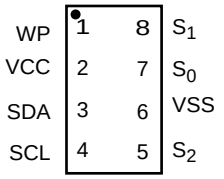
WP must be constant between each start and stop issued on the SDA bus and is always active (not gated). The WP pin has an active pull down to disable the write protection when the input is left floating. The Write Protect input controls the Hardware Write Protect feature. When held LOW, Hardware Write Protection is disabled. When this input is held HIGH, and the WPEN bit in the Write Protect Register is set HIGH, the Write Protect Register is protected, preventing changes to the Block Lock Protection and WPEN bits.

PIN NAMES

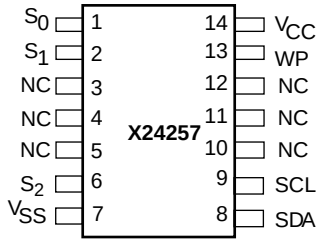
Symbol	Description
S_0, S_1, S_2	Device Select Inputs
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

PIN CONFIGURATION

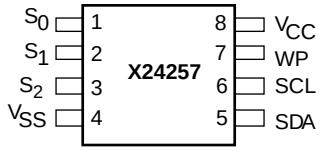
8-Lead XBGA: Top View



14 Lead TSSOP



8 Lead PDIP/SOIC



DEVICE OPERATION

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the device will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Figure 1. Data Validity

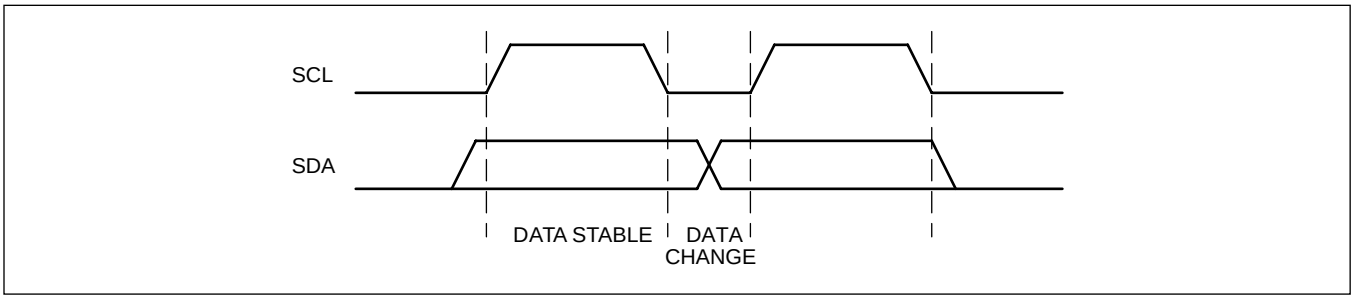
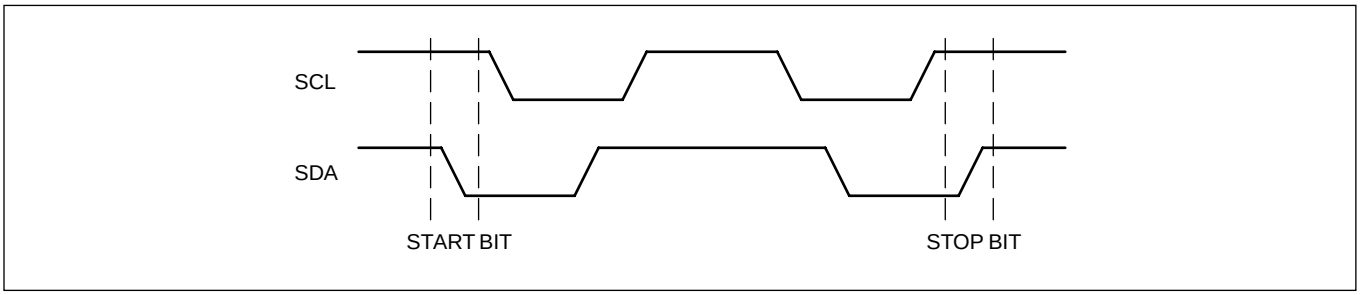


Figure 2. Definition of Start and Stop



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

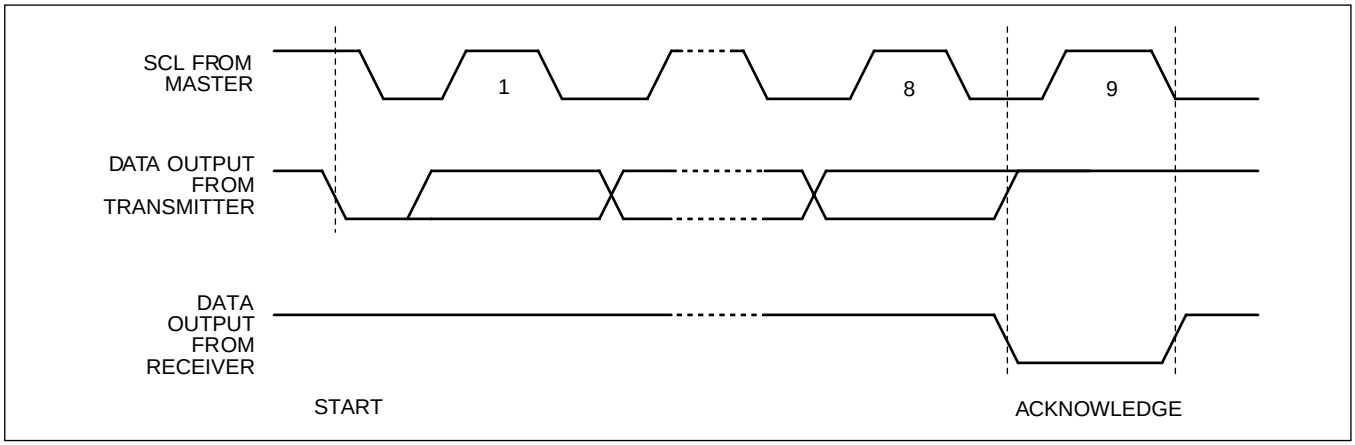
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The device will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the device will respond with an acknowledge after the receipt of each subsequent 8-bit word.

In the read mode the device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. If an acknowledge is not detected, the device will terminate further data transmissions. The master must then issue a stop condition to return the device to the standby power mode and place the device into a known state.

Figure 3. Acknowledge Response From Receiver



DEVICE ADDRESSING

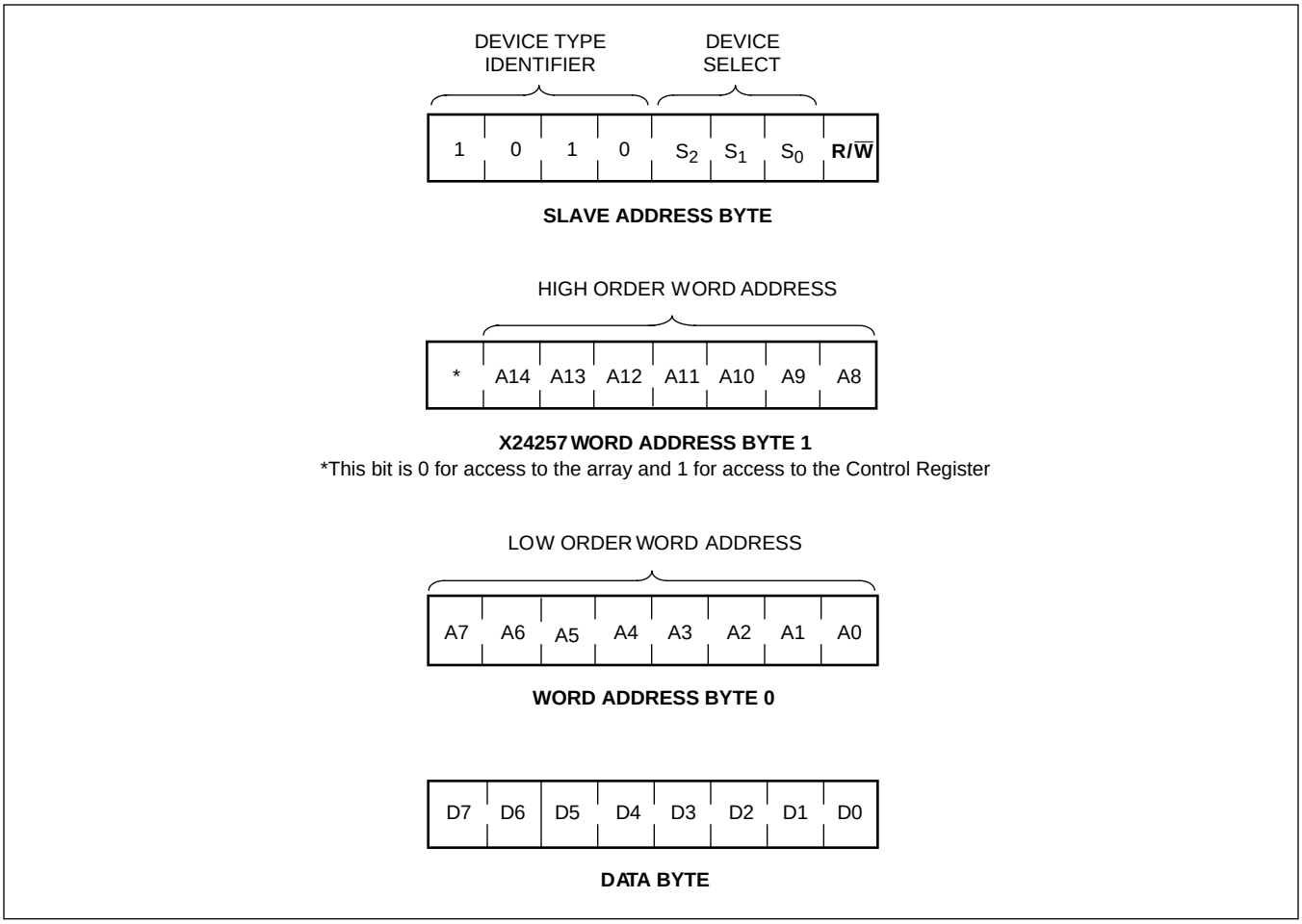
Following a start condition, the master must output the address of the slave it is accessing. The first four bits of the Slave Address Byte are the device type identifier bits. These must equal “1010”. The next 3 bits are the device select bits S_0, S_1, and S_2. This allows up to 8 devices to share a single bus. These bits are compared to the S_0, S_1, and S_2 device select input pins. The last bit of the Slave Address Byte defines the operation to be performed. When the R/$\overline{W}$ bit is a one, then a read operation is selected. When it is zero then a write operation is selected. Refer to Figure 4. After loading the Slave Address Byte from the SDA bus, the device compares the device type bits with the value “1010” and the device select bits with the status of the device select input pins. If the compare is not successful, no acknowledge is output during the ninth clock cycle and the device returns to the standby mode.

On power up the internal address is undefined, so the first read or write operation must supply an address.

The word address is either supplied by the master or obtained from an internal counter, depending on the operation. The master must supply the two Word Address Bytes as shown in Figure 4.

The internal organization of the E^2 array is 512 pages by 64 bytes per page. The page address is partially contained in the Word Address Byte 1 and partially in bits 7 through 6 of the Word Address Byte 0. The byte address is contained in bits 5 through 0 of the Word Address Byte 0. See Figure 4.

Figure 4. Device Addressing



WRITE OPERATIONS

Byte Write

For a write operation, the device follows “3 byte” protocol, consisting of one Slave Address Byte, one Word Address Byte 1, and the Word Address Byte 0, which gives the master access to any one of the words in the array. Upon receipt of the Word Address Byte 0, the device responds with an acknowledge, and waits for the first eight bits of data. After receiving the 8 bits of the data byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the device inputs are disabled and the device will not respond to any requests from the master. The SDA pin is at high impedance. See Figure 5.

Page Write

The device is capable of a 64 byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write operation after the first data word is transferred, the master can transmit up to sixty-three more words. The device will respond with an acknowledge after the receipt of each word, and then the byte address is internally incremented by one. The page address remains constant. When the counter reaches the end of the page, it “rolls over” and goes back to the first byte of the current page. This means that the master can write 64 bytes to the page beginning at any byte. If the master begins writing at byte 32, and loads 64 bytes, then the first 32 bytes are written to bytes 32 through 63, and the last 16 words are written to bytes 0 through 31. Afterwards, the address counter would point to byte 32.

If the master writes more than 64 bytes, then the previously loaded data is overwritten by the new data, one byte at a time.

The master terminates the data byte loading by issuing a stop condition, which causes the device to begin the nonvolatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge, and data transfer sequence.

Figure 5. Byte Write Sequence

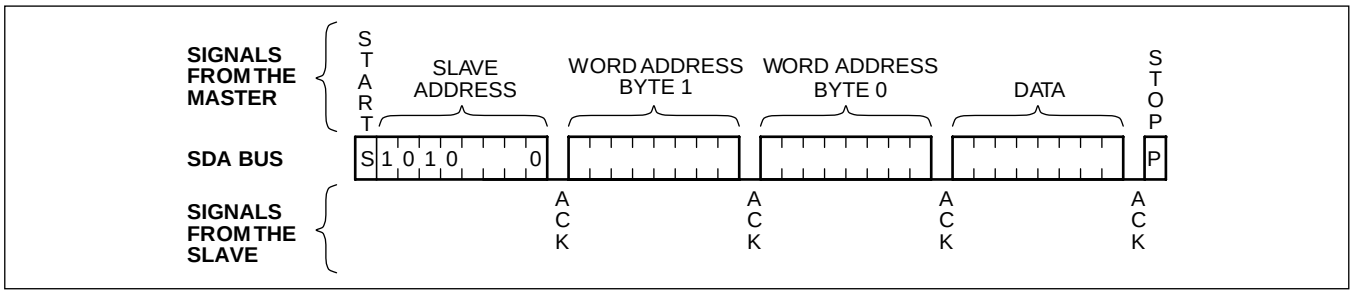
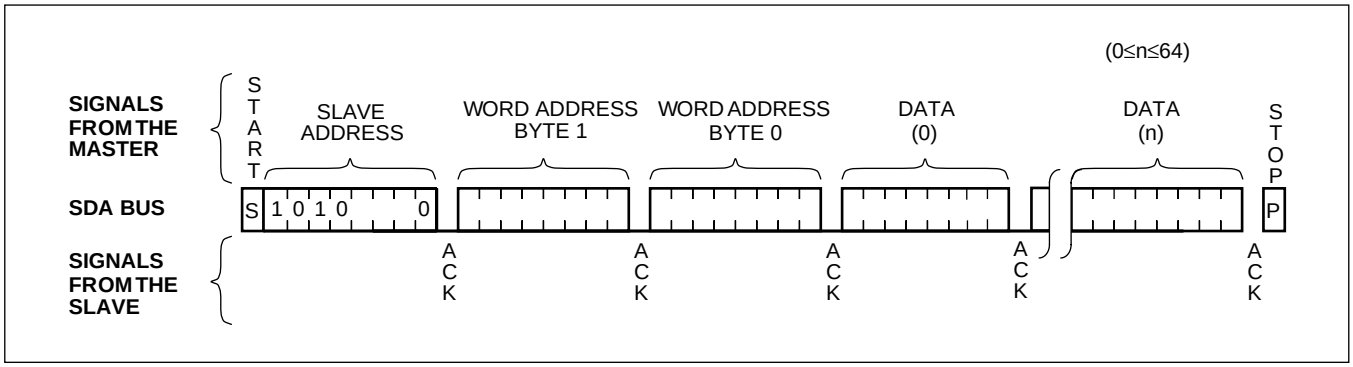


Figure 6. Page Write Sequence



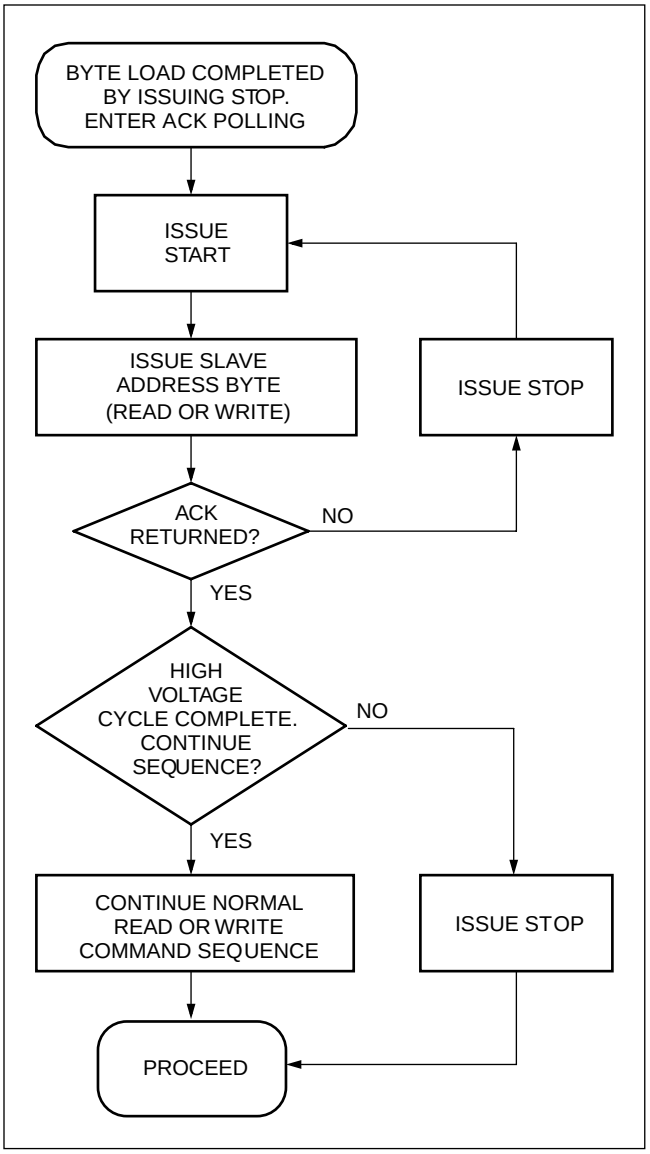
Stop and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and it's associated ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte + ACK is sent, then the device will reset itself without performing the write. The contents of the array will not be affected.

Acknowledge Polling

The maximum write cycle time can be significantly reduced using Acknowledge Polling. To initiate Acknowledge Polling, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the internal write cycle, then no ACK will be returned. If the device has completed the internal write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to Figure 7.

Figure 7. Acknowledge Polling Sequence



READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the Slave Address Byte is set to one. There are three basic read operations: Current Address Reads, Random Reads, and Sequential Reads.

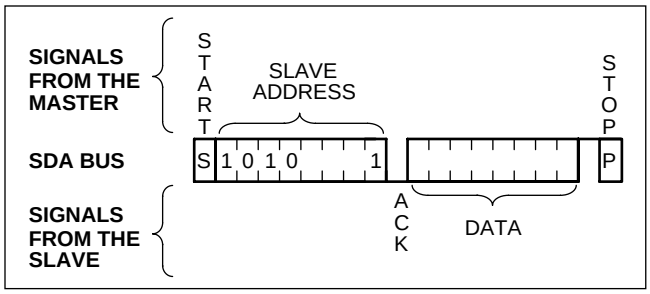
Current Address Read

Internally, the device contains an address counter that maintains the address of the last word read or written incremented by one. After a read operation from the last address in the array, the counter will “roll over” to the first address in the array. After a write operation to the last address in a given page, the counter will “roll over” to the first address on the same page.

Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the eight bits of the Data Byte. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. Refer to Figure 8 for the address, acknowledge, and data transfer sequence.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Figure 8. Current Address Read Sequence



Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to one, the master must first perform a “Dummy” write operation. The master issues the start condition and the Slave Address Byte with the R/$\overline{W}$ bit low, receives an acknowledge, then issues the Word Address Byte 1, receives another acknowledge, then issues the Word Address Byte 0. After the device acknowledges receipt of the Word Address Byte 0, the master issues another start condition and the Slave Address Byte with the R/W bit set to one. This is followed by an acknowledge and then eight bits of data from the device. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 9 for the address, acknowledge, and data transfer sequence.

The device will perform a similar operation called “Set Current Address” if a stop is issued instead of the second start shown in Figure 9. The device will go into standby mode after the stop and all bus activity will be ignored until a start is detected. The effect of this operation is that the new address is loaded into the address counter, but no data is output by the device.

The next Current Address Read operation will read from the newly loaded address.

Sequential Read

Sequential reads can be initiated as either a current address read or random read. The first Data Byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all byte addresses, allowing the entire memory contents to be read during one operation. At the end of the address space the counter “rolls over” to address 0000h and the device continues to output data for each acknowledge received. Refer to Figure 10 for the acknowledge and data transfer sequence.

Figure 9. Random Read Sequence

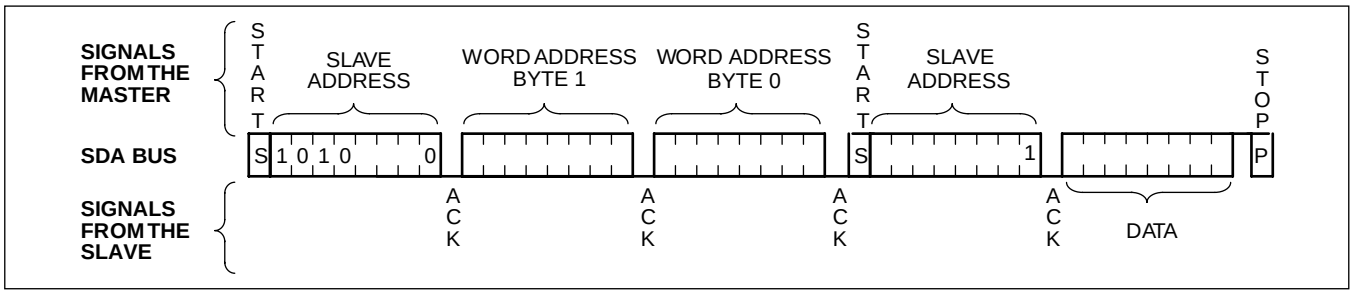
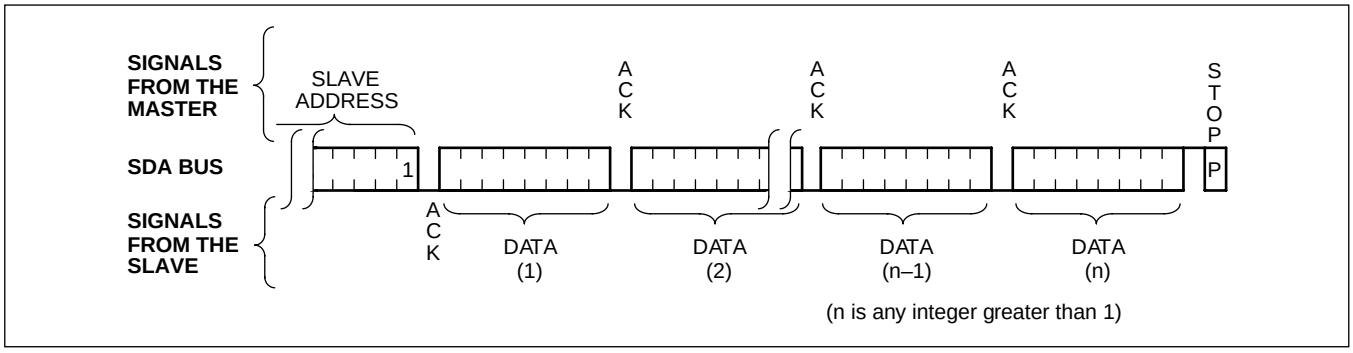


Figure 10. Sequential Read Sequence



CONTROL REGISTER (CR)

The Control Register is located in an area logically separated from the array and is only accessible via a byte write to the register address of FFFFH. The Control Register is physically part of the array.

The Control Register can only be modified by performing a byte write operation directly to the address of the register and only one data byte is allowed for each register write operation. Prior to initiating a nonvolatile write to the Control Register, the WEL and RWEL bits must be set using a two step process, with the whole sequence requiring 3 steps.

The user must issue a stop, after sending this byte to the register, to initiate the high voltage cycle that writes BP2, BP1, BP0 and WPEN to the nonvolatile bits. The part will not acknowledge any data bytes written after the first byte is entered. A stop must also be issued after a volatile register write operation to put the device into Standby. After a write to the CR, the address counter contents are undefined.

The state of the Control Register can be read by performing a random read at the address of the register at any time. Only one byte is read by the register read operation. The part will reset itself after the first byte is read. The master should supply a stop condition to be consistent with the bus protocol, but a stop is not required to end this operation. After the read of the CR, the address counter contents are reset to zero, but the user will be told these bits are undefined and instructed to do a random read.

Table 1. Control Register

7	6	5	4	3	2	1	0
WPEN	X	X	BP1	BP0	RWEL	WEL	BP2

RWEL: Register Write Enable Latch

The RWEL bit must be set to “1” prior to a write to Control Register.

WEL: Write Enable Latch (Volatile)

The WEL bit controls the access to the memory and to the Register during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes to any address, including any control registers will be ignored (no acknowledge will be issued after the Data Byte). The WEL bit is set by writing a “1” to the WEL bit and zeros to the other bits of the control register. Once set, WEL remains set until either it is reset to 0 (by writing a “0” to the WEL bit and zeros to the other bits of the control register) or until the part powers up again. Writes to WEL bit do not cause a high voltage write cycle, so the device is ready for the next operation immediately after the stop condition.

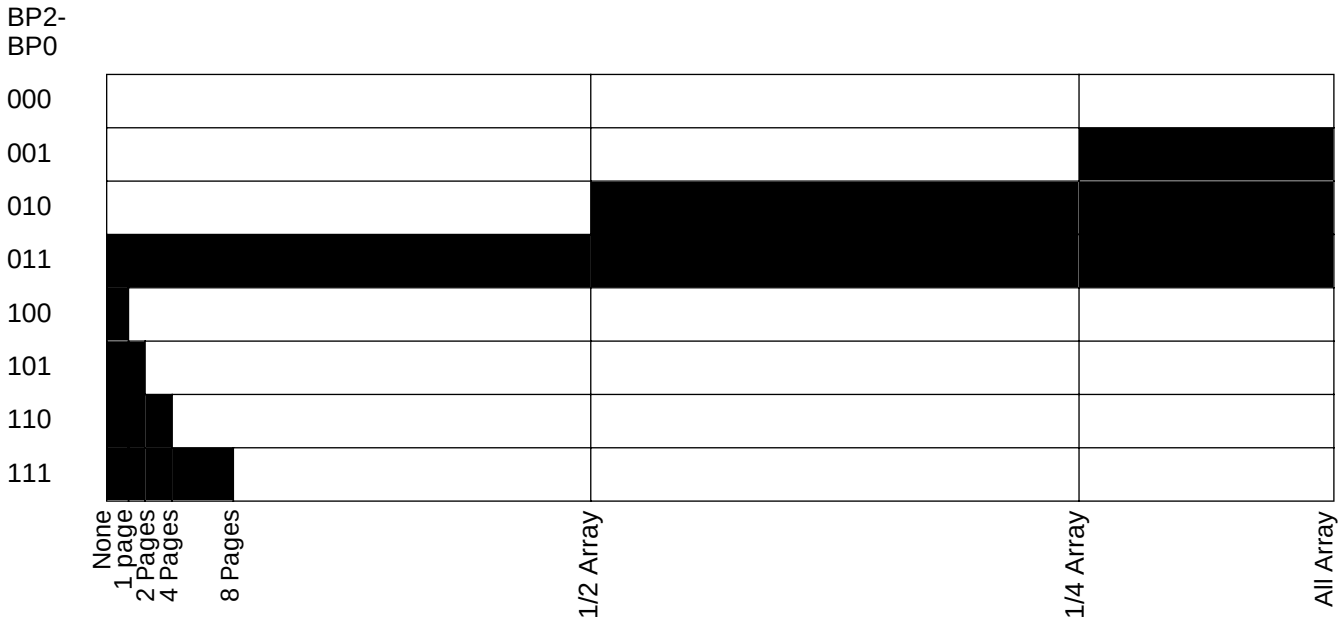
BP2, BP1, BP0: Block Protect Bits (Nonvolatile)

The Block Protect Bits, BP2, BP1 and BP0, determine which blocks of the array are write protected. A write to a protected block of memory is ignored. The block protect bits will prevent write operations to one of eight segments of the array. The partitions are described in Table 2.

Table 2. Block Protect Bits

BP2	BP1	BP0	Protected Addresses	Array Lock
0	0	0	None	None
0	0	1	6000h - 7FFFh (8K bytes)	Upper 1/4 (Q4)
0	1	0	4000h - 7FFFh (16K bytes)	Upper 1/2 (Q3, Q4)
0	1	1	0000h - 7FFFh (32K bytes)	Full Array (All)
1	0	0	0000h - 003Fh (64 bytes)	First Page (P1)
1	0	1	0000h - 007Fh (128 bytes)	First 2 pgs (P2)
1	1	0	0000h - 00FFh (256 bytes)	First 4 pgs (P4)
1	1	1	0000h - 01FFh (512 bytes)	First 8 pgs (P8)

Figure 11. Block Protection Configuration



Write Protect Enable Bit - WPEN - (Nonvolatile)

The Write Protect ($\overline{WP}$) pin and the Write Protect Enable (WPEN) bit in the Control Register control the Programmable Hardware Write Protect feature. Hardware Write Protection is enabled when the $\overline{WP}$ pin is HIGH and the WPEN bit is HIGH, and disabled when either the $\overline{WP}$ pin is LOW. When the chip is Hardware Write Protected, nonvolatile writes are disabled to the Control Register, including the Block Protect bits and the WPEN bit itself, as well as to the block sections in the memory array. Only the sections of the memory array that are not block protected can be written. Note that since the WPEN bit is write protected, it cannot be changed back to a LOW state; so write protection is enabled as long as the WP pin is held HIGH.

Table 3. Write Protect Enable Bit and WP Pin Function

WP	WPEN	Memory Array Not Block Protected	Memory Array Block Protected	Block Lock Bits	WPEN Bit	Protection
LOW	X	Writes OK	Writes Blocked	Writes OK	Writes OK	Software
HIGH	0	Writes OK	Writes Blocked	Writes OK	Writes OK	Software
HIGH	1	Writes OK	Writes Blocked	Writes Blocked	Writes Blocked	Hardware

Unused Bits:

Bits 5 & 6 are unused. All writes to the Control Register must have a zero in these bit positions. The Data Byte output during a Control Register read will contain zeros in these bit locations.

Writing to the Control Register

Changing any of the nonvolatile bits of the control register requires the following steps:

- Write a 02H to the Control Register to set the Write Enable Latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceeded by a start and ended with a stop).
- Write a 06H to the Control Register to set both the Register Write Enable Latch (RWEL) and the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation preceeded by a start and ended with a stop).
- Write a value to the Control Register that has all the control bits set to the desired state, with the WEL bit set to '1' and the RWEL bit set to '0'. This can be represented as *n*00*s t*01*r* in binary, where *n* is the WPEN bit and *rst* are the BP2-BP0 bits. (Operation preceeded by a start and ended with a stop). Since this is nonvolatile write cycle it will take up to 10ms to complete. The RWEL bit is reset by this cycle and the sequence must be repeated to change the nonvolatile bits again. If bit 2 is set to '1' in this third step (*n*00*s t*11*r*) then the RWEL bit remains set and the WPEN, BP2, BP1 and BP0 bits remain unchanged.
- A read operation occurring between any of the previous operations will not interrupt the register write operation.
- The RWEL bit cannot be reset without writing to the nonvolatile control bits in the control register, power cycling the device or attempting a write to a write protected block.

To illustate, a sequence of writes to the device consisting of [02H, 06H, 02H] will reset all of the nonvolatile bits to 0 and clear the RWEL bit. A sequence of [02H, 06H, 06H] will leave the nonvolatile bits unchanged and the RWEL bit remains set.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
24257.....–65°C to +135°C
Storage Temperature.....–65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} .....–1V to +7V
D.C. Output Current..... 5mA
Lead Temperature
(Soldering, 10 seconds).....300°C

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage	Limits
X24257	4.5V to 5.5V
X24257–2.5	2.5V to 5.5V
X24257–1.8	1.8V to 3.6V

D.C. OPERATING CHARACTERISTICS

V_{CC} equals the range indicated for each device type, unless otherwise stated.

Symbol	Parameter	V_{CC} = 1.8 to 3.6V		V_{CC} = 2.5 to 5.5V		V_{CC} = 4.5 to 5.5V		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{CC1}	Active Supply Current (Read)		0.5		1		1	mA	$V_{IL} = V_{CC}$ X 0.1 $V_{IH} = V_{CC}$ X 0.9 f_{SCL} = 400KHz SDA = Open
I_{CC2}	Active Supply Current (Write)		1.5		3		3	mA	
I_{SB1}(2)	Standby Current AC		1		1		1	mA	$V_{IL} = V_{CC}$ X 0.1 $V_{IH} = V_{CC}$ X 0.9 f_{SCL} = 400KHz SDA = Open
V_{SB}	Standby Voltage (Test)	V_{CC}– 0.1		V_{CC}– 0.2		V_{CC}– 0.3		V	
I_{SB2}(2)	Standby Current DC		1		1		10	mA	$V_{SDA} = V_{SCL} = V_{SB}$, Others = GND or V_{SB}
I_{LI}	Input Leakage Current		10		10		10	mA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10		10		10	mA	V_{SDA} = GND to V_{CC} Device is in Standby(2)
V_{IL}(3)	Input LOW Voltage	–0.5	V_{CC} x 0.3	–0.5	V_{CC} x 0.3	–0.5	V_{CC} x 0.3	V	
V_{IH}(3)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V_{CC} x 0.7	V_{CC} + 0.5	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{HYS}	Schmitt Trigger Input Hysteresis Fixed input level	0.2		0.2		0.2		V	
	V_{CC} related level	V_{CC} x 0.05		V_{CC} x 0.05		V_{CC} x 0.05		V	
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	I_{OL} = 3mA

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (S_0, S_1, S_2, SCL, WP)	6	pF	V_{IN} = 0V

Notes:

(1) The device enters the Active state after any start, and remains active until: 9 clock cycles later if the Device Select Bits in the Slave Address Byte are incorrect; 200ns after a stop ending a read operation; or t_{WC} after a stop ending a write operation.

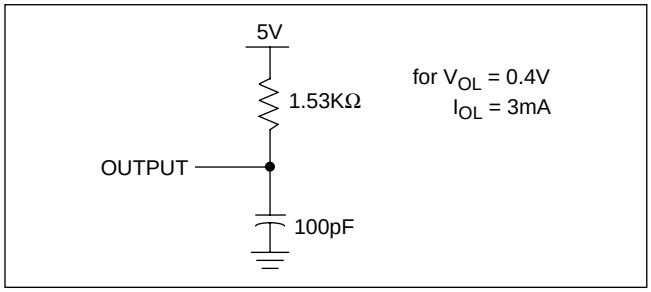
(2) The device goes into Standby: 200ns after any stop, except those that initiate a high voltage write cycle; t_{WC} after a stop that initiates a high voltage cycle; or 9 clock cycles after any start that is not followed by the correct Device Select Bits in the Slave Address Byte.

(3) VIL Min. and VIH Max. are for reference only and are not tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} X 0.5
Output Load	Standard Output Load

EQUIVALENT A.C. LOAD CIRCUIT



A.C. OPERATING CHARACTERISTICS

(Over the recommended operating conditions, unless otherwise specified.)

Read & Write Cycle Limits

Symbol	Parameter	V_{CC} 1.8V		V_{CC} 2.5V		Units
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	0	100	0	400	KHz
t_{IN}	Pulse width Suppression Time at Inputs	n/a	n/a	50		ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		1.3		µs
t_{LOW}	Clock LOW Period	4.7		1.3		µs
t_{HIGH}	Clock HIGH Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time	4.7		0.6		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
$t_{HD:DAT}$	Data In Hold Time	0		0		µs
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Output Hold Time	300		50		ns

A.C. OPERATING CHARACTERISTICS (CONTINUED)

(Over the recommended operating conditions, unless otherwise specified.)

Read & Write Cycle Limits

Symbol	Parameter	V_{CC} 1.8V		V_{CC} 2.5V		Units
		Min.	Max.	Min.	Max.	
t_R	SDA and SCL Rise Time		1000	20+ .1Cb(3)	300	ns
t_F	SDA and SCL Fall Time		300	20+ .1Cb(3)	300	ns
$t_{SU:S0, S1, S2, WP}$	S0, S1, S2, and WP Setup Time	0.4		0.6		ns
$t_{HD:S0, S1, S2, WP}$	S0, S1, S2, and WP Hold Time	0		0		ns
Cb	Capacitive load for each bus line		400		400	pF

POWER-UP TIMING(4)

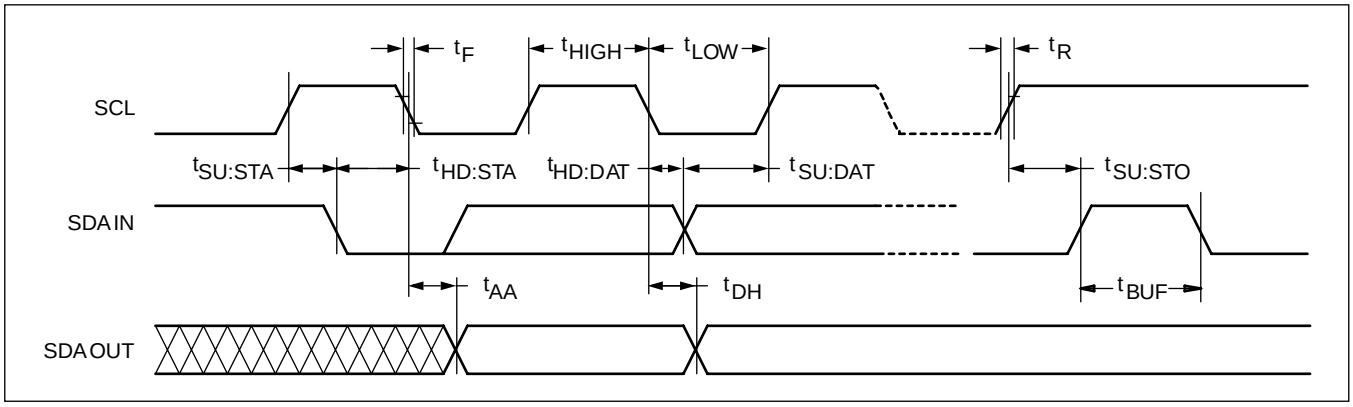
Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	5	ms

Notes:

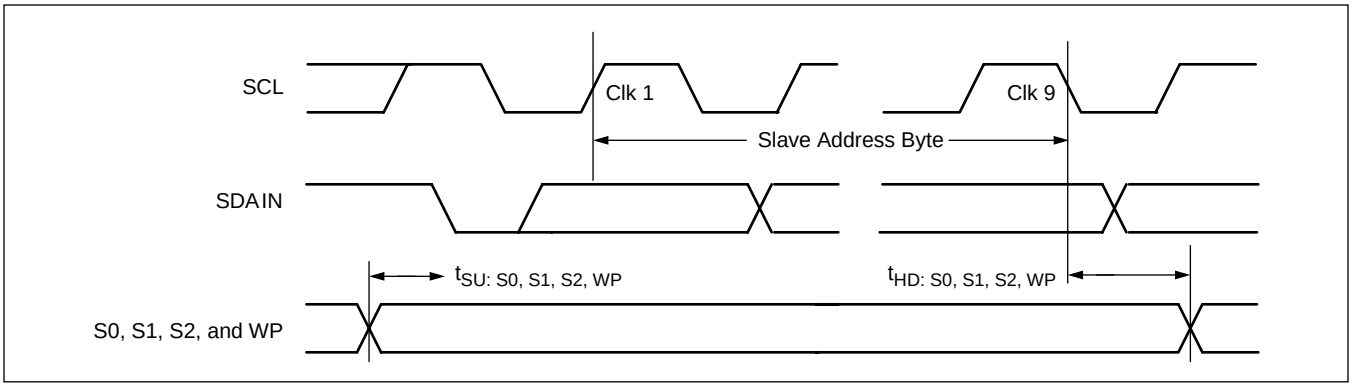
(4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

(5) Typical values are for T_A = 25°C and nominal supply voltage (5V), Cb = total capacitance of one bus line in pF.

Bus Timing



S0, S1, S2, and WP Pin Timing



Write Cycle Limits

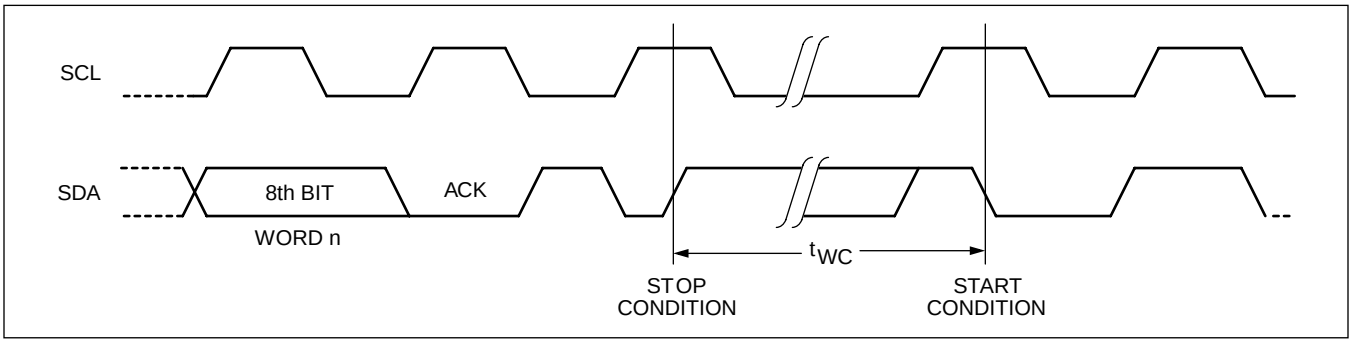
Symbol	Parameter	Min.	Typ.	Max.	Units
T_{WC}(6)	Write Cycle Time	—	5	10	ms

Notes:

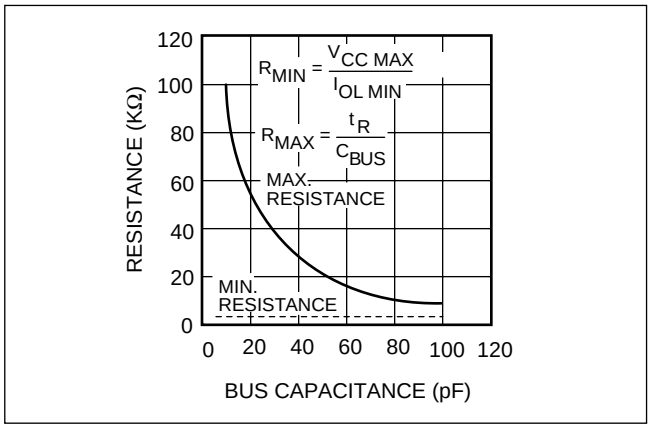
(6) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/write cycle. During the write cycle, the X24257 bus interface circuits are disabled, SDA is allowed to remain HIGH, and the device does not respond to its slave address.

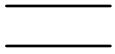
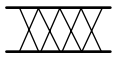
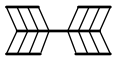
Write CycleTiming



Guidelines for Calculating Typical Values of Bus Pull-Up Resistors

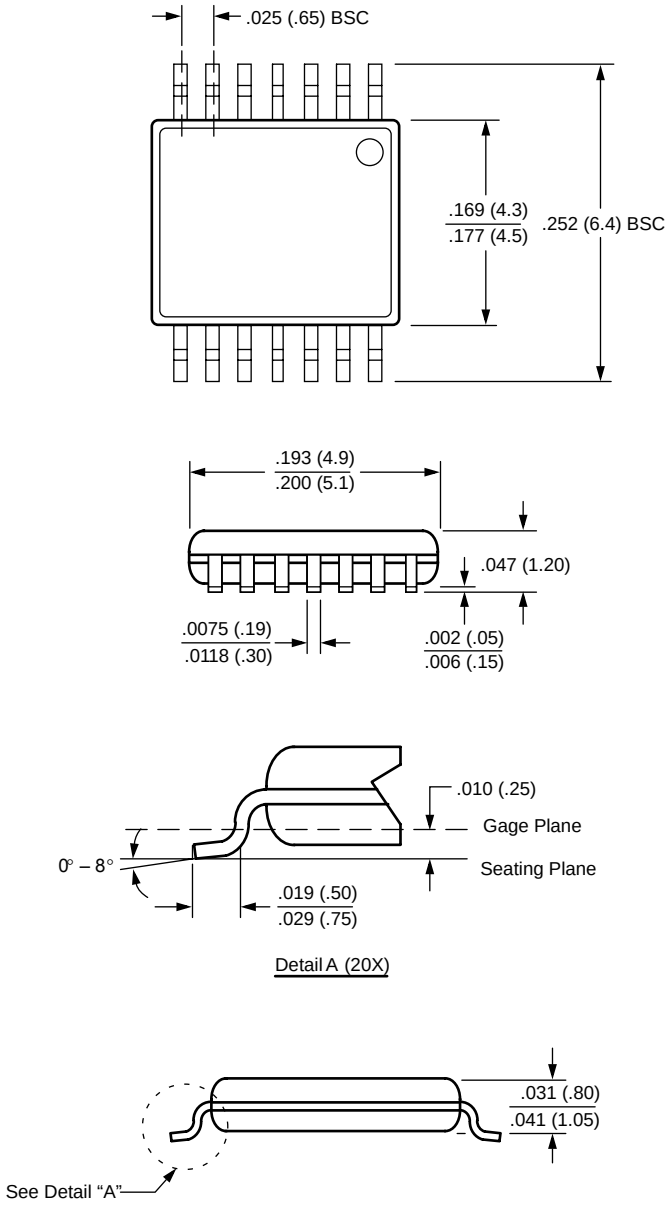


SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

PACKAGING INFORMATION

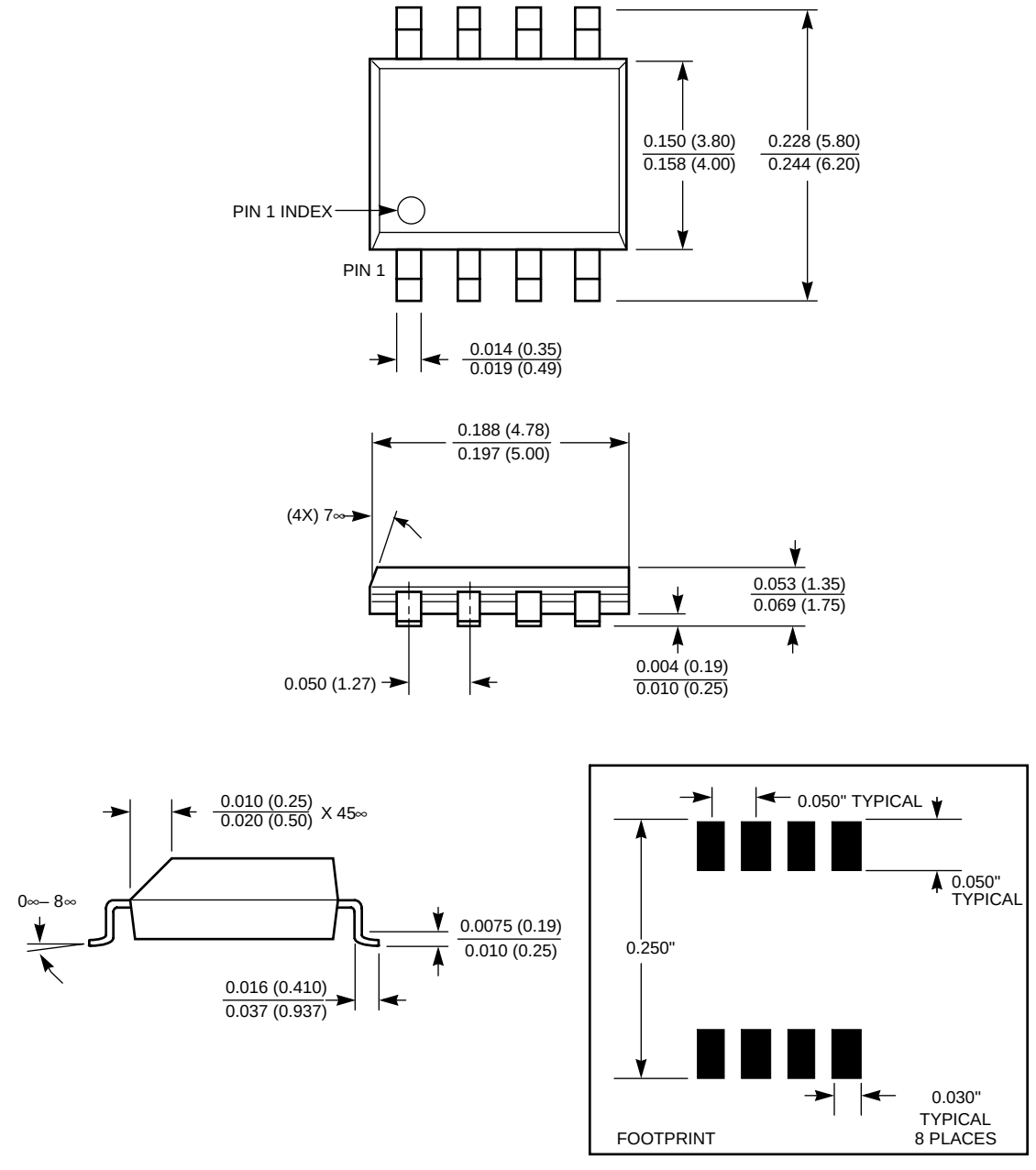
14-LEAD PLASTIC, TSSOP, PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

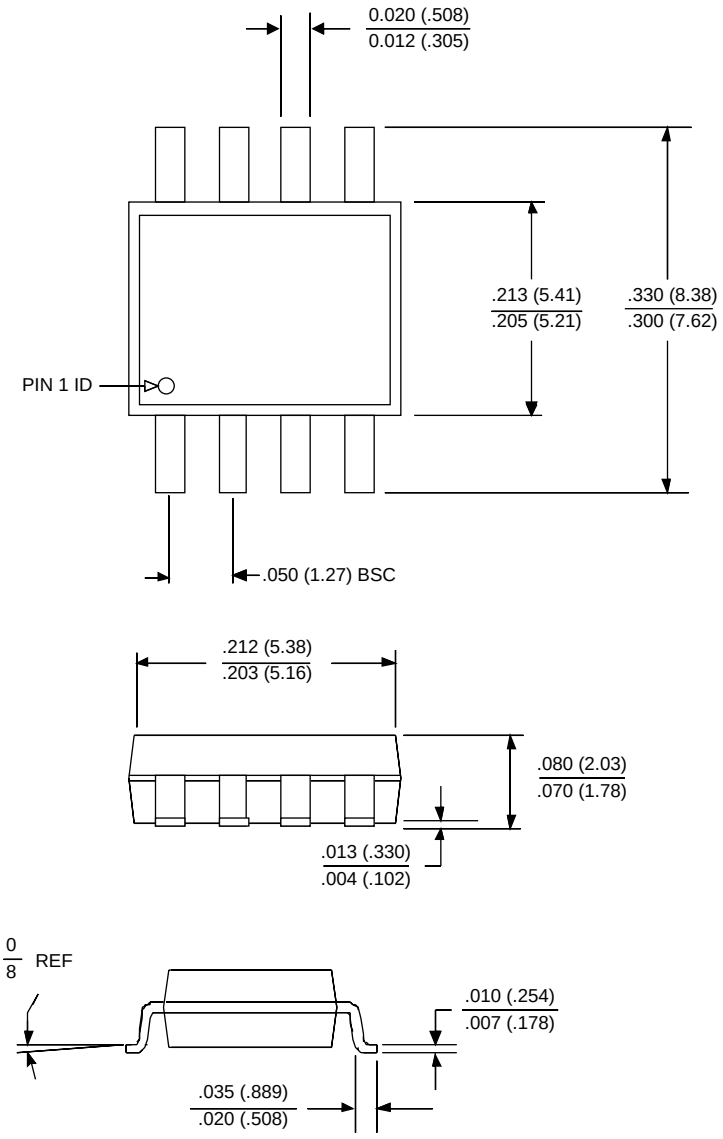
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-LEAD PLASTIC, 0.200" WIDE SMALL OUTLINE GULLWING PACKAGE TYP "A" (EIAJ SOIC)



NOTE:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

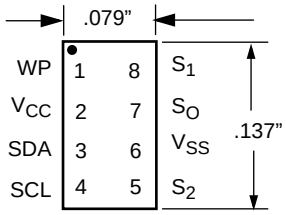
PACKAGING INFORMATION

8-Lead XBGA

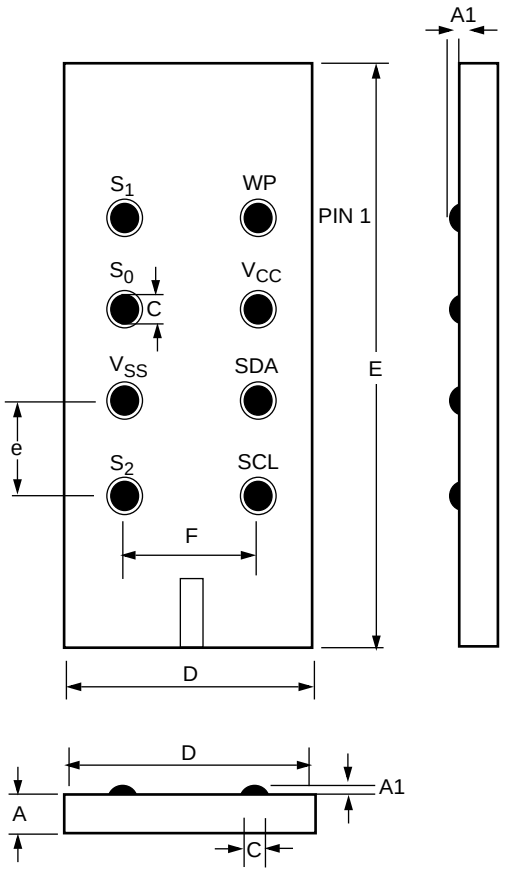
8-Lead XBGA

Complete Part Number	Top Mark
X24257Z-2.5	XACG
X24257ZI-2.5	XACH
X24257B-2.5	XACG
X24257BI-2.5	XACH

8-Lead XBGA: Top View



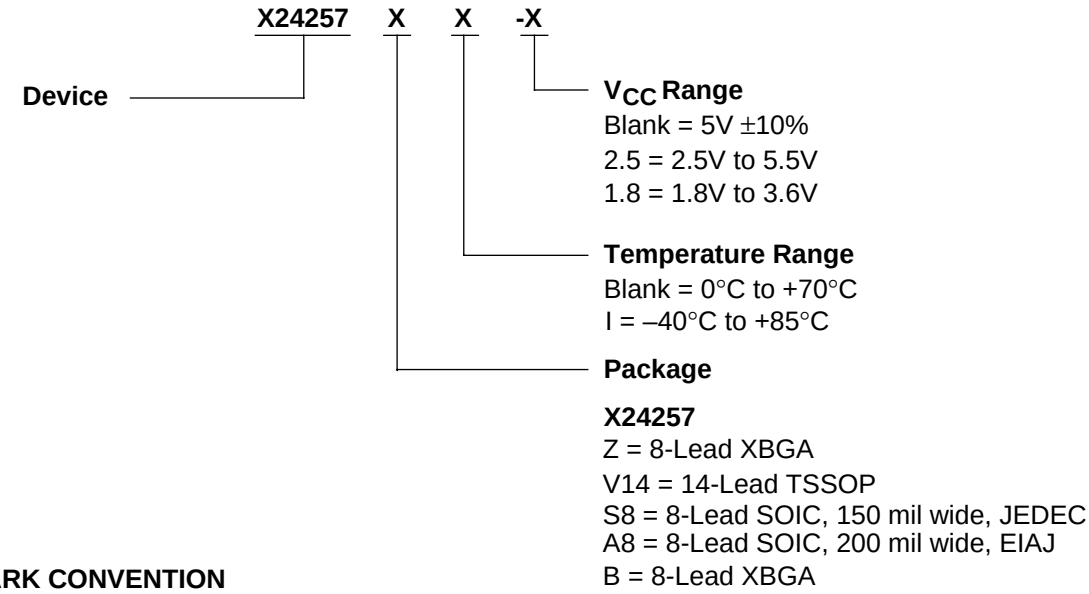
X24257: Bottom View



Dwg Symbol	8L XBGA
A	Contact Factory
A1	Contact Factory
C	Contact Factory
D	Contact Factory
E	Contact Factory
e	Contact Factory
F	Contact Factory

ALL DIMENSIONS IN μM (to convert to inches, 1μm = 3.94 x 10^{-5} inch)
ALL DIMENSIONS ARE TYPICAL VALUES

ORDERING INFORMATION



PART MARK CONVENTION

XBGA PACKAGE

Complete Part Number	Top Mark
X24257Z - 2.5	XACG
X24257ZI - 2.5	XACH
X24257B - 2.5	XACG
X24257BI - 2.5	XACH

Lead TSSOP/SOIC