

Advance Information

Switching Power Supply with Linear Regulators

The 33997 is a medium-power, multi-output power supply integrated circuit that is capable of operating over a wide input voltage range, from 6.0 V up to 26.5 V with 40 V transient capability. It incorporates a sensorless current mode control step-down switching controller regulating directly to 5.0 V. The 3.3 V linear regulator uses an external pass transistor to reduce the 33997 power dissipation. The 33997 also provides a 3.3 V linear standby regulator and two 5.0 V sensor supply outputs protected by internal low-resistance LDMOS transistors.

There are two separate enable pins for the main and sensor supply outputs and standard supervisory functions such as resets with power-up reset delay.

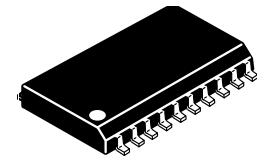
The 33997 provides proper power supply sequencing for advanced microprocessor architectures such as the Motorola MPC5xx and 683xx microprocessor families.

Features

- Operating Voltage Range 6.0 V up to 26.5 V (40 V transient)
- Step-Down Switching Regulator Output $V_{DDH} = 5.0 \text{ V} @ 1400 \text{ mA}$ (total)
- Linear Regulator with External Pass Transistor $V_{DDL} = 3.3 \text{ V} @ 400 \text{ mA}$
- Low-Power Standby Linear Regulator $V_{KAM} = 3.3 \text{ V} @ 10 \text{ mA}$
- Two 5.0 V @ 200 mA (typical) Sensor Supplies V_{REF} Protected Against Short-to-Battery and Short-to-Ground with Retry Capability
- Undervoltage Shutdown on the V_{DDL} , V_{DDH} Outputs with Retry Capability
- Reset Signals
- Power-Up Delay
- Enable Pins for Main Supplies (EN) and Sensor Supplies (SNSEN)
- Power Sequencing for Advanced Microprocessor Architectures
- SOIC-24WB Package

33997

**POWER SUPPLY
INTEGRATED CIRCUIT**

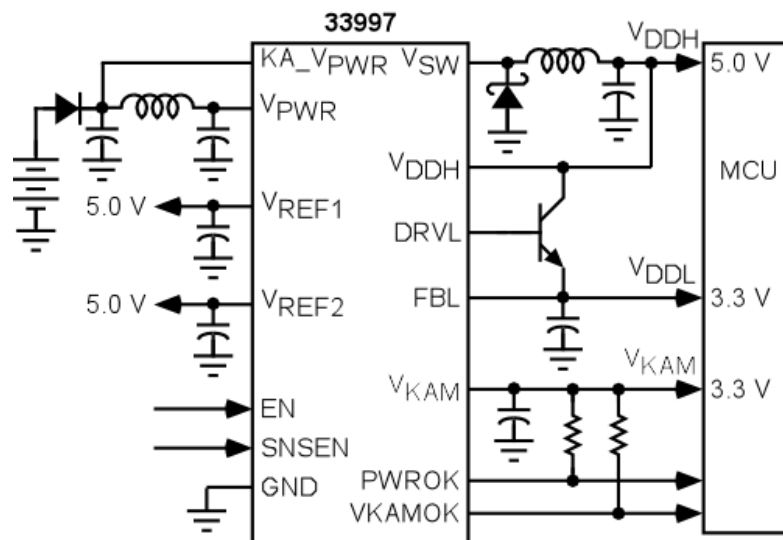


**DW SUFFIX
PLASTIC PACKAGE
24-LEAD SOICW
CASE 751E**

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33997DW/R2	-40°C to 125°C	24 SOICW

33997 Simplified Application Diagram



This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

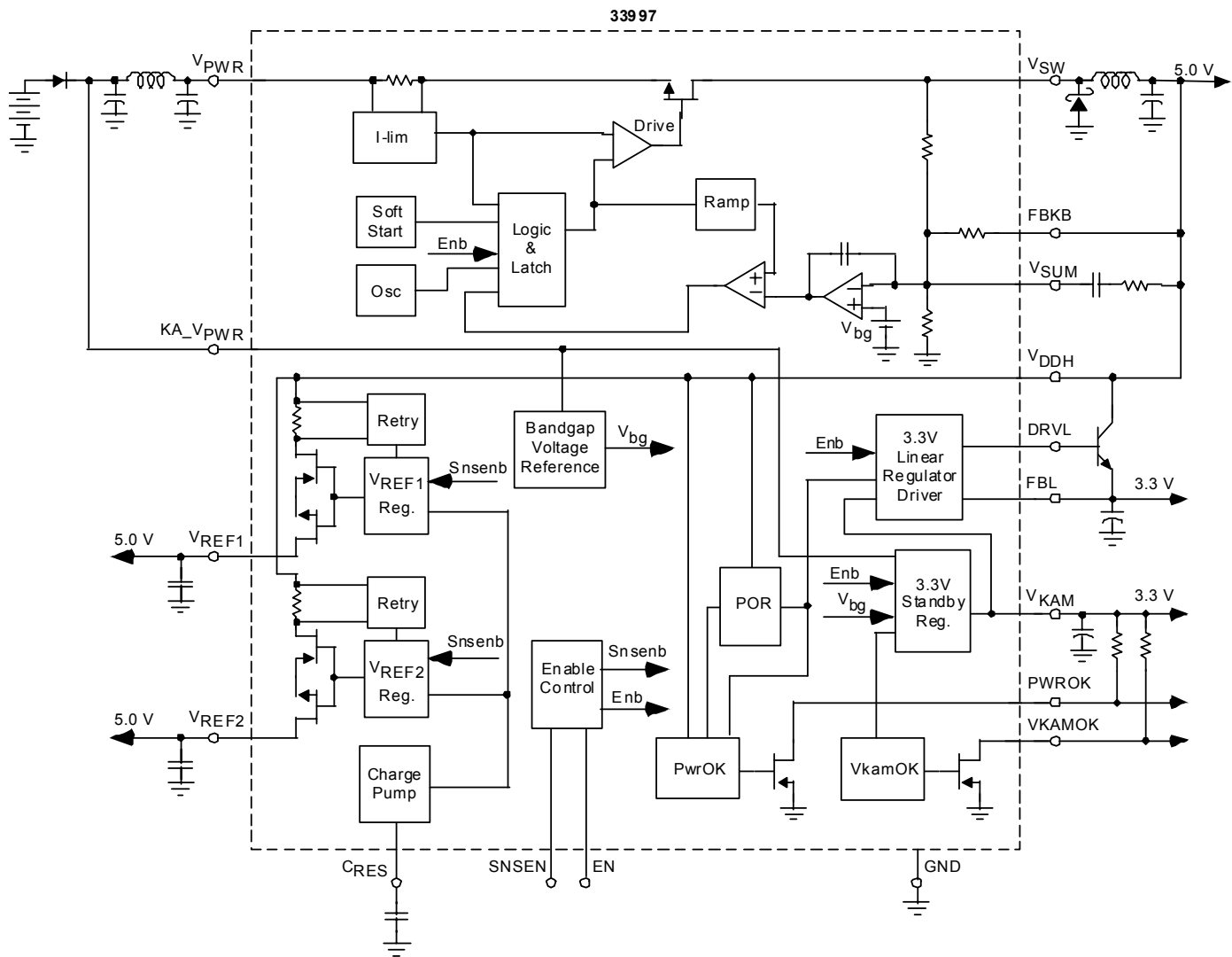
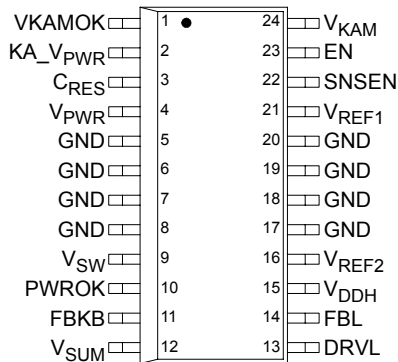


Figure 1. 33997 Simplified Block Diagram



PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1	VKAMOK	Keep-Alive Output Monitoring. This pin is an "open-drain" output that will be used with a discrete pull-up resistor to V_{KAM} . When the supply voltage to the 33997 is disconnected or lost, the VKAMOK signal goes low.
2	KA_VPWR	Keep Alive Power Supply Pin. This supply pin is used in modules that have both direct battery connections and ignition switch activated connections.
3	CRES	Reservoir Capacitor. This pin is tied to an external "reservoir capacitor" for the internal charge pump.
4	V _{PWR}	Power Supply Pin. Main power input to the IC. This pin is directly connected to the switching regulator power MOSFET. In automotive applications this pin must be protected against reverse battery conditions by an external diode.
5–8	GND	Ground of the integrated circuit.
9	V _{SW}	Internal P-Channel Power MOSFET Drain. V_{SW} is the "switching node" of the voltage buck converter. This pin is connected to the V_{PWR} pin by an integrated p-channel MOSFET.
10	PWROK	Power OK Reset Pin. This pin is an "open-drain" output that will be used with a discrete pull-up resistor to V_{KAM} , V_{DDH} , or V_{DDL} . When either V_{DDH} or V_{DDL} output voltage goes out of the regulation limits this pin is pulled down.
11	FBKB	Step-Down Switching Regulator Feedback Pin. The FBKB pin is the V_{DDH} feedback signal for the switching regulator.
12	V _{SUM}	Error Amplifier "Summing Node". The V_{SUM} pin is connected to the inverting input of the error amplifier. This node is also the "common" point of the integrated feedback resistor divider.
13	DRV L	Drive for V_{DDL} (3.3 V) Regulator. The DRV L pin drives the base of an external NPN pass transistor for the V_{DDL} linear post regulator. The collector of the VDDL pass transistor is connected to V_{DDH} . An example of a suitable pass transistor is BCP68.
14	FBL	Feedback for V_{DDL} (3.3 V) Regulator. The FBL pin is the voltage feedback sense signal from the V_{DDL} (3.3 V) linear post regulator.
15	V _{DDH}	V_{DDH} is an input supply pin providing power for the buffered sensor supplies and the drive circuitry for the 3.3 V linear power regulator. The V_{DDH} pin is supplied from the switching regulator output, capable of providing 5.0 V @ 1400 mA total output current.
16	V _{REF2}	Sensor Supply #2 Output. The V_{REF2} pin is sensor supply output #2.
17–20	GND	Ground of the integrated circuit.
21	V _{REF1}	Sensor Supply #1 Output. The V_{REF1} pin is sensor supply output #1.

PIN FUNCTION DESCRIPTION (continued)

Pin	Pin Name	Description
22	SNSEN	Sensor Supply Enable Input. The SNSEN pin is an input, which enables the V_{REF1} and V_{REF2} supplies. It allows the control module hardware/software to shut down the sensor supplies.
23	EN	Enable Input. The EN pin is an input, which enables the main switching regulator and all other functions. When this pin is low, the power supply is in a low quiescent state.
24	V_{KAM}	Keep-Alive (standby) 3.3 V Regulator Output. This is a 3.3 V low quiescent, low dropout regulator for Keep Alive memory.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Main Supply Voltage	V_{PWR}	-0.3 to 45	V
Keep-Alive Supply Voltage	KA_V_{PWR}	-0.3 to 45	V
Switching Node	V_{SW}	-0.5 to 45	V
5.0 V Input Power	V_{DDH}	-0.3 to 6.0	V
Sensor Supply	V_{REF1} V_{REF2}	-0.3 to 18 -0.3 to 18	V
Keep-Alive Supply Voltage	V_{KAM}	-0.3 to 6.0	V
Maximum Voltage at Logic I/O Pins	EN SSEN PWROK VKAMOK	-0.3 to 6.0 -0.3 to 6.0 -0.3 to 6.0 -0.3 to 6.0	V
Charge Pump Reservoir Capacitor Voltage	C_{RES}	-0.3 to 18	V
Error Amplifier Summing Node	V_{SUM}	-0.3 to 6.0	V
Switching Regulator Output Feedback	FBKB	-0.3 to 6.0	V
V_{DDL} Base Drive	DRV_L	-0.3 to 6.0	V
V_{DDL} Feedback	FBL	-0.3 to 6.0	V
ESD Voltage			V
Human Body Model (all pins) (Note 1)	V_{ESD1}	±500	
Machine Model (all pins) (Note 2)	V_{ESD2}	±100	
Power Dissipation ($T_A = 25^\circ\text{C}$) (Note 3)	P_D	800	mW
Thermal Resistance, Junction to Ambient (Note 4), (Note 5)	$R_{\theta J-A}$	60	$^\circ\text{C/W}$
Thermal Resistance, Junction to Board (Note 6)	$R_{\theta J-B}$	20	$^\circ\text{C/W}$
Operational Package Temperature [Ambient Temperature] (Note 7)	T_A	-40 to 125	$^\circ\text{C}$
Operational Junction Temperature	T_J	-40 to 150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 to 150	$^\circ\text{C}$
Lead Soldering Temperature (Note 8)	T_S	260	$^\circ\text{C}$

Notes

- ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP}=100\text{ pF}$, $R_{ZAP}=1500\ \Omega$).
- ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP}=200\text{ pF}$, $R_{ZAP}=0\ \Omega$)
- Maximum power dissipation at indicated junction temperature.
- Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.
- Lead soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions $9.0\text{ V} \leq V_{PWR} \leq 16\text{ V}$, $-40^\circ\text{C} \leq T_J = T_A \leq 125^\circ\text{C}$, using the typical application circuit (see Figure 8) unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL					
Supply Voltage Range					V
Normal Operating Voltage Range (Note 9)	$V_{PWR(N)}$	6.0	–	18	
Extended Operating Voltage Range (Note 9)	$V_{PWR(E)}$	18	–	26.5	
Maximum Transient Voltage - Load Dump (Note 10)	$V_{PWR(LD)}$	–	–	40	V
V_{PWR} Supply Current	I_{VPWR}				mA
EN = 5.0 V, $V_{PWR} = 14\text{ V}$, No Loads		25	–	150	
V_{PWR} Quiescent Supply Current	I_{Q_VPWR}				μA
EN = 0 V, $V_{PWR} = 12\text{ V}$		5.0	–	15	
KA_V_{PWR} Supply Current,	I_{KAVPWR}				mA
EN = 5.0 V, $KA_V_{PWR} = 14\text{ V}$, No Load on V_{KAM}		0.5	–	3.0	
KA_V_{PWR} Quiescent Supply Current	I_{Q_KAVPWR}				μA
EN = 0 V, $KA_V_{PWR} = 12\text{ V}$		50	–	350	

BUCK REGULATOR V_{DDH}

Buck Converter Output Voltage	V_{DDH}				V
$I_{VDDH} = 200\text{ mA}$ to 1.4 A, $V_{PWR} = KA_V_{PWR} = 14\text{ V}$		4.9	–	5.1	
Buck Converter Output Voltage	V_{DDH}				V
$I_{VDDH} = 1.4\text{ A}$, $V_{PWR} = KA_V_{PWR} = 6.0\text{ V}$		4.9	–	5.1	
V_{DDH} Line Regulation	$RegL_{VDDH}$				mV
$V_{PWR} = KA_V_{PWR} = 10\text{ V}$ to 14 V, $I_{VDDH} = 200\text{ mA}$		-20	–	30	
V_{DDH} Load Regulation	$RegLd_{VDDH}$				mV
$V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $I_{VDDH} = 200\text{ mA}$ to 1.4 A		-20	–	20	
$V_{PWR} = KA_V_{PWR} = 6.0\text{ V}$, $I_{VDDH} = 200\text{ mA}$ to 1.4 A		-20	–	20	
V_{DDH} Active Discharge Resistance	R_{HDisch}				Ω
$V_{PWR} = KA_V_{PWR} = 14\text{ V}$, EN = 0 V, $I_{VDDH} = 10\text{ mA}$		1.0	–	15	

P-CHANNEL MOSFET

Drain-Source Breakdown Voltage—Not Tested (Note 11)	BV_{DSS}	45	–	–	V
Drain-Source Current Limit—Not Tested (Note 11)	I_{scSW1}	–	-7.0	–	A

Notes

9. V_{DDH} is fully functional when the 33997 is operating at higher battery voltages, but these parameters are not tested. The test condition as are:
 - a) V_{DDH} must be between 4.9 V and 5.1 V (200 mA to 1.4 A) for $V_{PWR} = 14\text{ V}$ to 18 V.
 - b) V_{DDH} must be between 4.8 V and 5.5 V (200 mA to 1.4 A) for $V_{PWR} = 18\text{ V}$ to 26.5 V.
10. Part can survive, but no parameters are guaranteed.
11. Guaranteed by design but not production tested.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions $9.0\text{ V} \leq V_{PWR} \leq 16\text{ V}$, $-40^\circ\text{C} \leq T_J = T_A \leq 125^\circ\text{C}$, using the typical application circuit (see Figure 8) unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LINEAR REGULATOR V_{DDL}					
V_{DDL} Output Voltage $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $I_{VDDL} = 200\text{ mA}$	V_{DDL}	3.15	–	3.45	V
V_{DDL} Line Regulation $V_{DDH} = 4.8\text{ V}$ to 5.2 V , $I_{VDDL} = 400\text{ mA}$	$RegLn_{VDDL}$	-70	–	70	mV
V_{DDL} Load Regulation $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $I_{VDDL} = 10\text{ mA}$ to 400 mA	$RegLd_{VDDL}$	-70	–	70	mV
DRV1 Output Current $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $V_{DRV1} = 1.0\text{V}$	I_{DRV1}	5.0	11	25	mA
V_{DDL} Active Discharge Resistance $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $EN = 0\text{ V}$, $I_{FBL} = 10\text{ mA}$	R_{LDisch}	1.0	–	10	Ω
V_{DDH} to V_{DDL} Active Clamp Resistance $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $EN = 0\text{ V}$, $I_{VDDH} = 50\text{ mA}$, $V_{FBKB} = 0\text{ V}$	R_{CLAMP}	0.6	–	10	Ω
V_{DDL} Output Capacitor Capacitance (Note 12)	C_{VDDL}	–	68	–	μF
V_{DDL} Output Capacitor ESR (Note 12)	ESR_{VDDL}	–	0.125	–	Ω

KEEP-ALIVE (STANDBY) REGULATOR V_{KAM}

V_{KAM} Output Voltage $I_{VKAM} = 5.0\text{ mA}$, $V_{PWR} = KA_V_{PWR} = 18\text{ V}$, $EN = 5.0\text{ V}$	V_{KAM}	3.0	–	3.6	V
V_{KAM} Output Voltage, $EN = 0\text{ V}$ (Standby Mode) $V_{PWR} = KA_V_{PWR} = 26\text{ V}$, $I_{VKAM} = 0.5\text{ mA}$ $V_{PWR} = KA_V_{PWR} = 18\text{ V}$, $I_{VKAM} = 5.0\text{ mA}$ $V_{PWR} = KA_V_{PWR} = 5.0\text{ V}$, $I_{VKAM} = 10.0\text{ mA}$ $V_{PWR} = 0\text{ V}$, $KA_V_{PWR} = 3.5\text{ V}$, $I_{VKAM} = 5.0\text{ mA}$	V_{KAM}	3.0 3.0 3.0 2.0	– – – –	3.6 3.6 3.6 3.5	V
V_{KAM} Line Regulation, $EN = 0\text{ V}$ (Standby Mode) $V_{PWR} = KA_V_{PWR} = 5.0\text{ V}$ to 18 V , $I_{VKAM} = 2.0\text{ mA}$	$RegLn_{VKAM}$	-20	–	20	mV
V_{KAM} Load Regulation, $EN = 0\text{ V}$ (Standby Mode) $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $I_{VKAM} = 1.0\text{ mA}$ to 10 mA	$RegLd_{VKAM}$	0	–	100	mV
Differential Voltage $V_{KAM} - V_{DDL}$ $EN = 5.0\text{ V}$, $I_{VKAM} = 5.0\text{ mA}$, $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $I_{VDDL} = 200\text{ mA}$	Reg_{VKAM}	-20	–	20	mV
V_{KAM} Output Capacitor Capacitance (Note 12)	C_{VKAM}	–	4.7	–	μF
V_{KAM} Output Capacitor ESR (Note 12)	ESR_{VKAM}	–	1.4	–	Ω

Notes

12. Recommended value.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions $9.0\text{ V} \leq V_{PWR} \leq 16\text{ V}$, $-40^\circ\text{C} \leq T_J = T_A \leq 125^\circ\text{C}$, using the typical application circuit (see Figure 8) unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SENSOR SUPPLIES V_{REF1}, V_{REF2}					
V_{REF} On-Resistance, $T_A = -40^\circ\text{C}$ $I_{VREF} = 200\text{ mA}$, $I_{VDDH} = 200\text{ mA}$, $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $EN = 5.0\text{ V}$	$R_{DS(on)}$	–	–	280	$\text{m}\Omega$
V_{REF} On-Resistance, $T_A = +25^\circ\text{C}$ $I_{VREF} = 200\text{ mA}$, $I_{VDDH} = 200\text{ mA}$, $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $EN = 5.0\text{ V}$	$R_{DS(on)}$	–	–	350	$\text{m}\Omega$
V_{REF} On-Resistance, $T_A = +125^\circ\text{C}$ $I_{VREF} = 200\text{ mA}$, $I_{VDDH} = 200\text{ mA}$, $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $EN = 5.0\text{ V}$	$R_{DS(on)}$	–	–	455	$\text{m}\Omega$
V_{REF} Short-to-Battery Detect Current $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $EN = 5.0\text{ V}$, $SNSEN = 5.0\text{ V}$	I_{SC_Bat}	500	–	900	mA
V_{REF} Short-to-Ground Detect Current $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $EN = 5.0\text{ V}$, $SNSEN = 5.0\text{ V}$	I_{SC_Gnd}	500	–	900	mA
Maximum Output Capacitance (Total) (Note 13)	C_{VREF}	33	–	39	nF

SUPERVISORY CIRCUITS

PWROK Undervoltage Threshold on V_{DDL} , FBL Ramps Down $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $I_{VDDH} = 200\text{ mA}$	$V_{FBL(thL)}$	2.6	–	3.1	V
PWROK Undervoltage Threshold on V_{DDH} $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $I_{VDDH} = 200\text{ mA}$	$V_{DDH(thL)}$	4.5	–	4.8	V
V_{DDH} Overvoltage Threshold $V_{PWR} = KA_V_{PWR} = 10\text{ V}$, $I_{VDDH} = 200\text{ mA}$	$V_{DDH(thH)}$	5.12	–	5.7	V
PWROK Open Drain On-Resistance $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $EN = 5\text{ V}$, $I_{PwrOK} = 5.0\text{ mA}$	$R_{DS(on)}$	–	–	200	Ω
VKAMOK Threshold, $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $I_{VDDH} = 200\text{ mA}$	$V_{KAM(thL)}$	0.9	–	1.9	V
VKAMOK Threshold on V_{PWR} , V_{PWR} Ramps Up $KA_V_{PWR} = 14\text{ V}$, $I_{VDDH} = 200\text{ mA}$	$V_{PWRok(th)}$	4.0	–	5.0	V
VKAMOK Open Drain On-Resistance $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $EN = 0\text{ V}$, $I_{VKAMOK} = 10\text{ mA}$	$R_{DS(on)}$	50	–	200	Ω
Enable Input Voltage Threshold (Pin EN)	V_{IH}	1.0	–	2.0	V
Enable Pull-Down Current (Pin EN), $EN = 1.0\text{ V}$ V_{DDH} to $V_{IL(min)}$	I_{PD}	500	–	1200	nA
Sensor Enable Input Voltage Threshold (Pin SNSEN)	V_{IH}	1.0	–	2.0	V
Sensor Enable Pull-Down Current (Pin SNSEN) $SNSEN = 1.0\text{ V}$ V_{DDH} to $V_{IL(min)}$	I_{PD}	500	–	1200	nA

Notes

13. Recommended value.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions $9.0\text{ V} \leq V_{PWR} \leq 16\text{ V}$, $-40^\circ\text{C} \leq T_J = T_A \leq 125^\circ\text{C}$, using the typical application circuit (see Figure 8) unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CHARGE PUMP C_{RES}					
Charge Pump Voltage	V_{CRES}				V
$V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $I_{VDDH} = 200\text{ mA}$, $I_{CP} = 0\text{ }\mu\text{A}$		12	–	15	
$V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $I_{VDDH} = 200\text{ mA}$, $I_{CP} = 10\text{ }\mu\text{A}$		12	–	15	

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions $9.0\text{ V} \leq V_{PWR} \leq 16\text{ V}$, $-40^\circ\text{C} \leq T_J = T_A \leq 125^\circ\text{C}$ using the typical application circuit (see Figure 8) unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
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BUCK REGULATOR V_{DDH}

Switching Frequency (Note 14)	f_{SW}	–	750	–	kHz
Soft Start Duration (see Figure 2) $V_{PWR} = KA_V_{PWR} = 6.0\text{ V}$	t_{SS}	5.0	–	15	ms

CHARGE PUMP C_{RES}

Charge Pump Current Ramp-Up Time $V_{PWR} = KA_V_{PWR} = 14\text{ V}$, $C_{RES} = 22\text{ nF}$, $V_{CP} = 1.0\text{ V to }11\text{ V}$	t_{CRES}	1.0	–	20	ms
Charge Pump Ramp-Up Time $V_{PWR} = KA_V_{PWR} = 7.0\text{ V}$, $C_{RES} = 22\text{ nF}$, $V_{CP} = 7.0\text{ V to }10\text{ V}$	t_{CRES}	1.0	–	10	ms

SENSOR SUPPLIES V_{REF1} , V_{REF2}

V_{REF} Overcurrent Detection Time (see Figure 3) V_{REF} Load $R_L = 5.0\ \Omega$ to GND, $V_{DDH} = 5.1\text{ V}$, $V_{PWR} = KA_V_{PWR} = 10\text{ V}$, $EN = 5.0\text{ V}$, $SNSEN = 5.0\text{ V}$	t_{Det}	0.5	–	2.0	μs
V_{REF} Retry Timer Delay (see Figure 3) V_{REF} Load $R_L = 5.0\ \Omega$ to GND, $V_{DDH} = 5.1\text{ V}$, $V_{PWR} = KA_V_{PWR} = 10\text{ V}$, $EN = 5.0\text{ V}$, $SNSEN = 5.0\text{ V}$	t_{Ret}	5.0	–	20	ms

SUPERVISORY CIRCUITS

PWROK Delay Time (Power-On Reset) (see Figure 4)	$t_{D(PWROK)}$	5.0	–	15	ms
VKAMOK Delay Time (see Figure 5)	$t_{D(VKAMOK)}$	10	–	30	ms
V_{DDH} Power-Up Delay Time (see Figure 6)	$t_{D(VPWR)}$	1.0	–	10	ms
Fault-Off Timer Delay Time (see Figure 7)	t_{Fault}	1.0	–	10	ms

Notes

- Guaranteed by design but not production tested.

Timing Diagrams

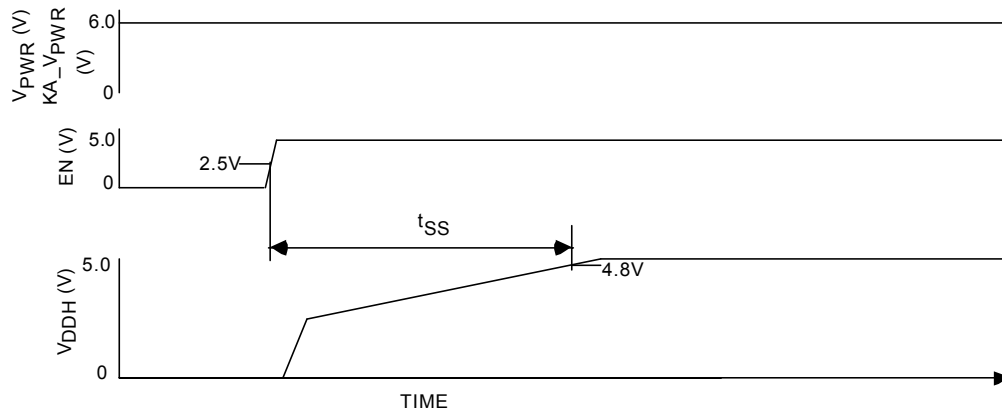


Figure 2. Soft-Start Time

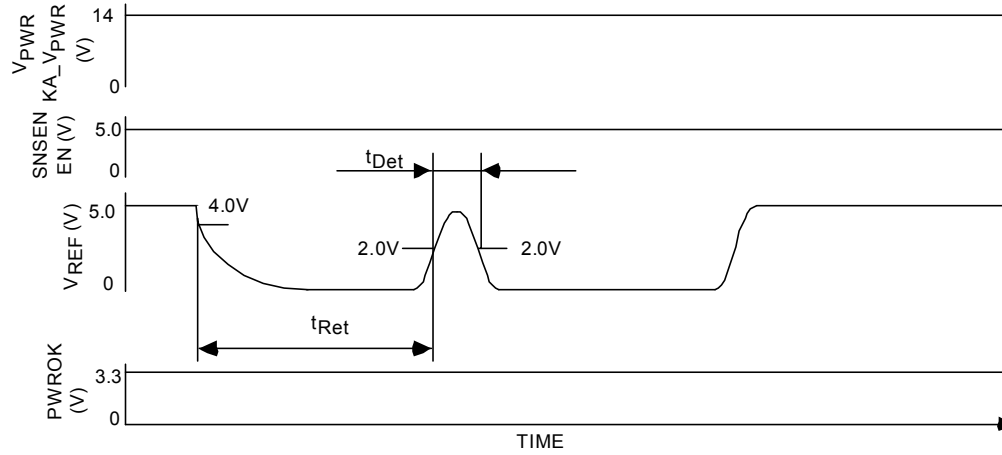


Figure 3. V_{REF} Retry Timer

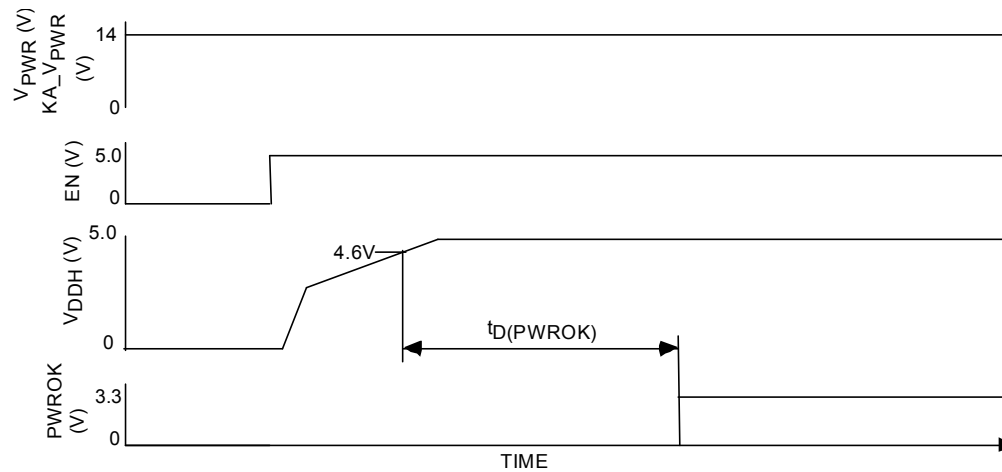


Figure 4. PWROK Delay Timer (Power-On Reset)

Timing Diagrams (continued)

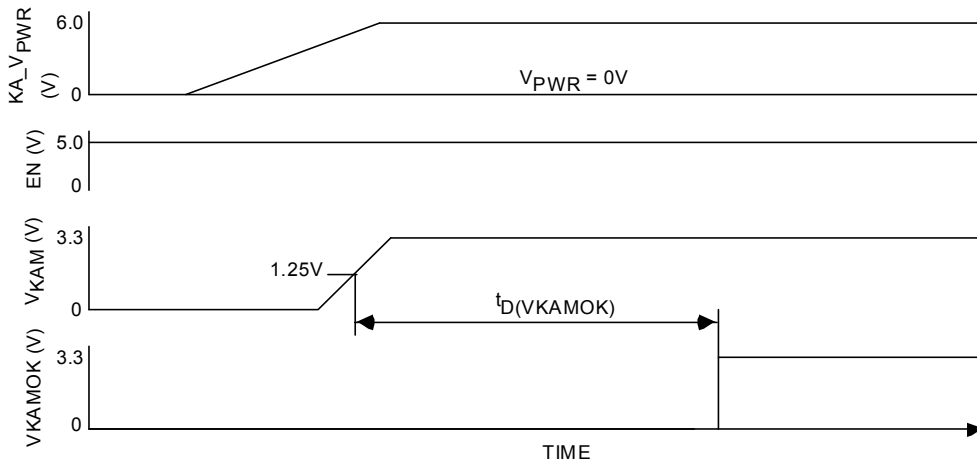


Figure 5. VKAMOK Delay Time

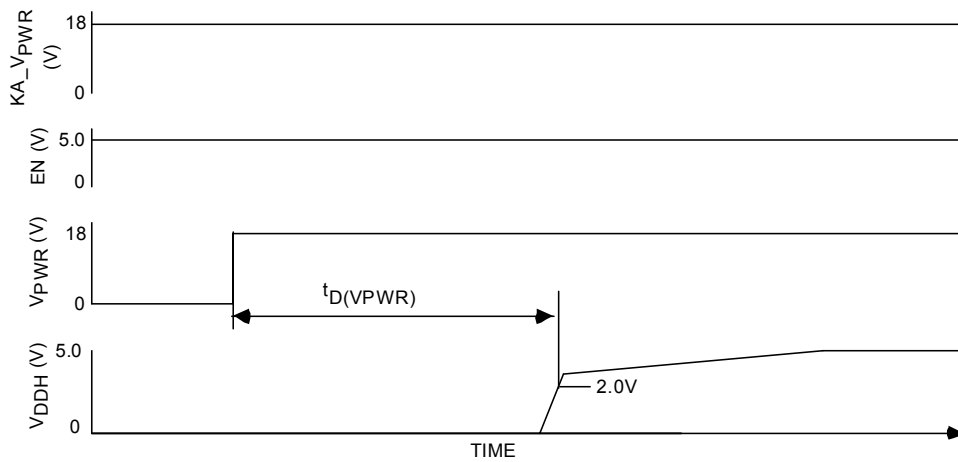


Figure 6. V_{DDH} Power-Up Delay Time

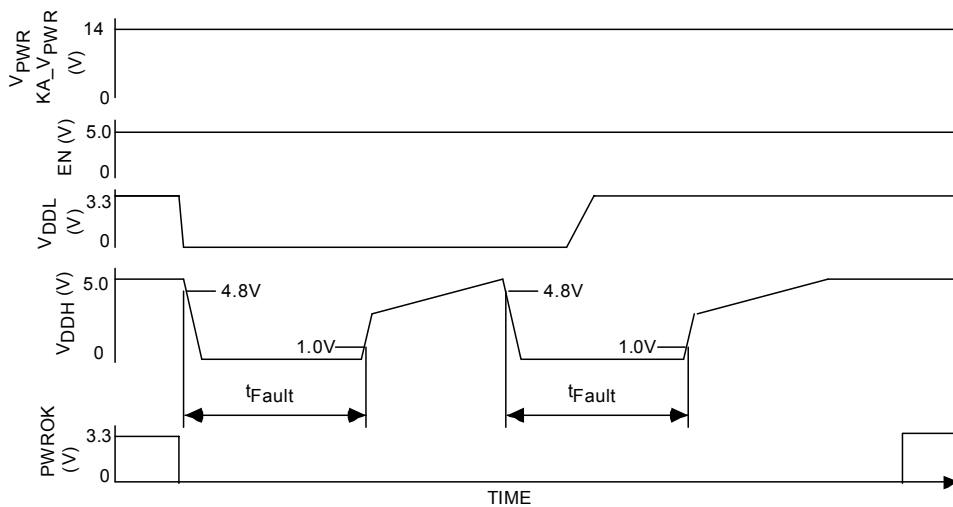


Figure 7. Fault-Off Timer Delay Time

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 33997 multi-output power supply integrated circuit is capable of operating from 6.0 V up to 26.5 V with 40 V transient capability. It incorporates a step-down switching controller regulating directly to 5.0 V. The 3.3 V linear regulator uses an external pass transistor, thus reducing the power dissipation of

the integrated circuit. The 33997 also provides a 3.3 V linear standby regulator and two 5.0 V sensor supply outputs protected by internal low-resistance LDMOS transistors against short-to-battery and short-to-ground.

FUNCTIONAL PIN DESCRIPTION

Switching Regulator V_{DDH}

The switching regulator is a high-frequency (750 kHz), conventional buck converter with integrated high-side p-channel power MOSFET. Its output voltage is regulated to provide 5.0 V with $\pm 2\%$ accuracy and it is intended to directly power the digital and analog circuits of the Electronic Control Module (ECM). The switching regulator output is rated for 1400 mA total output current. This current can be used by the linear regulator V_{DDL} and sensor supplies V_{REF1} and V_{REF2} . The 33997 switching controller utilizes "Sensorless Current Mode Control" to achieve good line rejection and stabilize the feedback loop. A soft-start feature is incorporated into the 33997. When the device is enabled, the switching regulator output voltage V_{DDH} ramps up to about half of full scale and then takes 16 steps up to the nominal regulation voltage level (5.0 V nominal).

3.3 V Linear Regulator V_{DDL}

The 3.3 V linear post-regulator is powered from the 5.0 V switching regulator output (V_{DDH}). A discrete pass transistor is used to the power path for the V_{DDL} regulator. This arrangement minimizes the power dissipation off the controller IC. The FBL pin is the feedback input of the regulator control loop and the DRV1 pin the external NPN pass transistor base drive. Power up, power down, and fault management are coordinated with the 5.0 V switching regulator.

Sensor Supplies V_{REF1} and V_{REF2}

The sensor supplies are implemented using a protected switch to the main 5.0 V (switching regulator) output. The 33997 integrated circuit provides two low-resistance LDMOS power MOSFETs connected to the switching regulator output (V_{DDH}). These switches have short-to-battery and short-to-ground protection integrated into the IC. When a severe fault condition is detected, the affected sensor output is turned off and the sensor Retry Timer starts to time out. After the Retry Timer expires, the sensor supply tries to power up again. Sensor supplies V_{REF} can be disabled by pulling the Sensor Enable SENSE pin low (see Figure 7 for the V_{REF} Retry Timer operation).

Notes: Severe fault conditions on the V_{REF1} and V_{REF2} outputs, like hard shorts to either ground or battery, may disrupt the operation of the main regulator V_{DDH} . Shorts to battery

above 17 V are considered "double faults" and neither one of the V_{REF} outputs is protected against such conditions.

Depending on the V_{DDH} capacitor value and its ESR value, the severity of the short may disrupt the V_{DDH} operation.

Keep-Alive (Standby) Regulator V_{KAM}

The Keep-Alive Regulator V_{KAM} (keep-alive memory) is intended to provide power for "key off" functions such as nonvolatile SRAM, "KeyOff" timers and controls, KeySwitch monitor circuits, and perhaps a CAN/SCP monitor and wake-up function. It may also power other low-current circuits required during a "KeyOff" condition. The regulated voltage is nominally 3.3 V. A severe fault condition on the V_{KAM} output is signaled by pulling the VKAMOK signal low.

V_{KAM} Keep-Alive Operation (Standby, Power-Down Mode)

When the EN pin is pulled low, the power supply is forced into a low-current standby mode. In order to reduce current drawn by the V_{PWR} and KA_V_{PWR} pins, all power supply functions are disabled except for the V_{KAM} and Enable (EN) pins. The latter pin is monitored for the "wake-up" signal. The switching transistor gate is actively disabled and the V_{DDL} and V_{DDH} pins are actively pulled low.

Power-Up Delay Timers

Two Power-Up Delay timers are integrated into the control section of the integrated circuit. One timer monitors the input voltage at the V_{PWR} input pin (see Figure 3), and the other monitors the input voltage at the KA_V_{PWR} input pin. In both cases, sufficient supply voltage must be present long enough for the timers to "time out" before the switching regulator can be enabled.

Fault-Off Timer

If the V_{DDL} output voltage does not reach its valid range at the end of soft-start period, or if the V_{DDH} or V_{DDL} output voltage gets below its PWROK threshold level, the Fault-Off Timer shuts the switching regulator off until the timer "times out" and the switching regulator retries to power up again (see Figure 7 for Fault-Off Timer operation details).

Power-On Reset Timer

This timer starts to time out at the end of the soft-start period if the V_{DDH} and V_{DDL} outputs are in the valid regulation range. If the timer “times out”, then the open-drain PWROK signal is released, indicating that “power is ON”.

Supervisory Circuits PWROK and VKAMOK

The 33997 has two voltage monitoring open-drain outputs, the PWROK and the VKAMOK pins. PWROK is “active high”. This output is pulled low when either of the regulator outputs

(V_{DDH} or V_{DDL}) are below their regulation windows. If both regulator outputs are above their respective lower thresholds, and the Power-On Reset Timer has expired, the output driver is turned off and this pin is at high-impedance state (see Figure 6).

The VKAMOK signal indicates a severe fault condition on the keep-alive regulator output V_{KAM} . The V_{KAM} output voltage is compared to the internal bandgap reference voltage. When the V_{KAM} falls below the bandgap reference voltage level, the VKAMOK signal is pulled low.

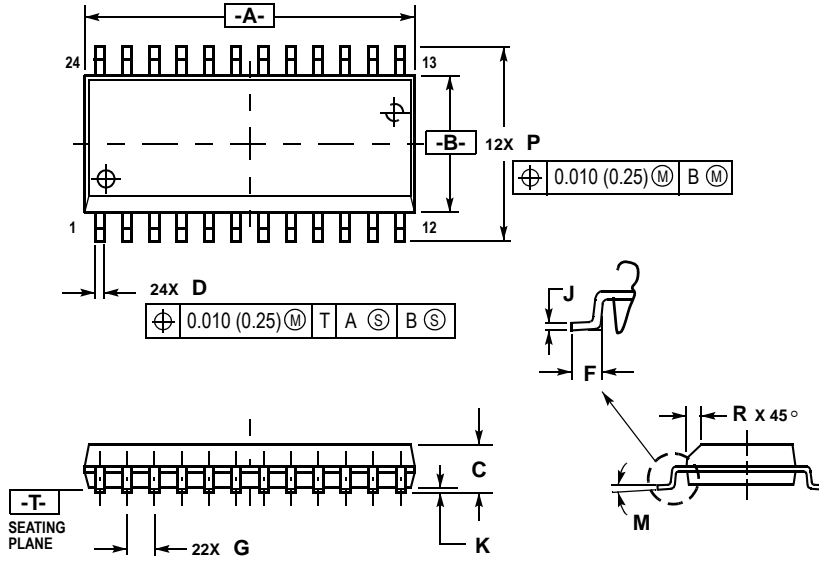
Designator	Value/Rating	Description/Part No.	Manufacturer (Note 17)
Cs1, Cs2	33 nF/25 V	Ceramic X7R	Any Manufacturer
Cc1	2.2 nF/16 V	Ceramic X7R	Any Manufacturer
R1, R2	10 k Ω	Resistor 0805, 5%	Any Manufacturer
R3 (Optional)	2.2 Ω	Resistor 0805, 5%	Any Manufacturer
Rc1	3.6 k Ω	Resistor 0805, 5%	Any Manufacturer
Lf1	10 μ H	CDRH127-100M or SLF10145-100M2R5	Sumida TDK
L1	15 μ H	CDRH127-150MC or SLF10145-150M2R2	Sumida TDK
Q1	1.0 A/20 V	Bipolar Transistor/BCP68T1	ON Semiconductor
D1	2.0 A/50 V	Schottky Diode/SS25	General Semiconductor
Dp1	3.0 A/200 V	Diode/MURS320	ON Semiconductor
Dp2	27 V	Transient Voltage Suppressor/SM5A27	General Semiconductor

Notes

17. Motorola does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Motorola offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

PACKAGE DIMENSIONS

DW SUFFIX
 (24-LEAD SOIC WIDE BODY)
 PLASTIC PACKAGE
 CASE 751E-04
 ISSUE E



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES

NOTES

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