YAMAHA

YAC526

EVR3

Electric Variable Resistance 3

■Outline

YAC526 (EVR3) is a 2ch high grade digital volume LSI for high-end audio systems.
Owing to its built-in high-quality sound operational amplifier, output with wide dynamic range and low distortion factor can be obtained.
YAC526 is able to control each channel through a serial data interface in 255 steps at 0.5dB per step, and daisy chain connection can constitute a multichannel system.
Owing to its zero-cross detection function, the device is able to suppress audible noise that may occur at a quick volume change.

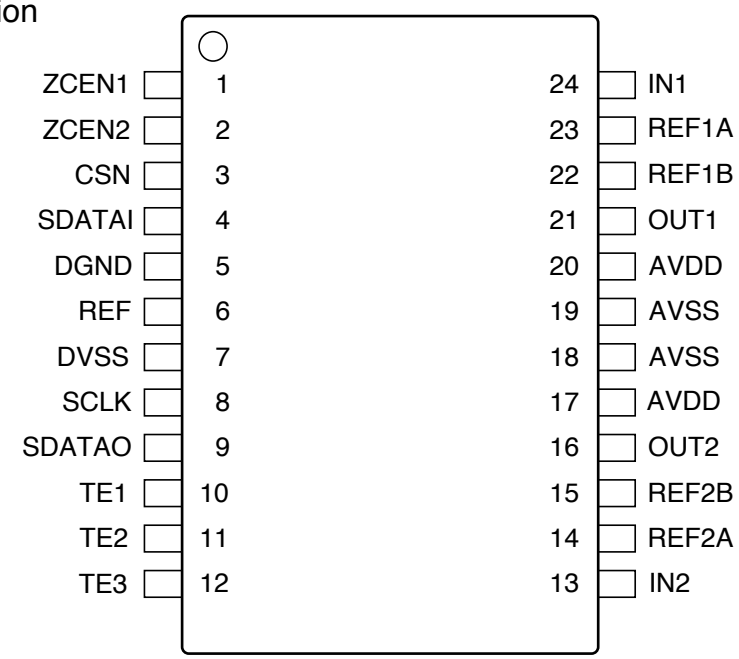
■Features

- Built-in 2channel high sound quality operational amplifier.
- Wide volume range.
  ＋31.5dB～－95.0dB, MUTE (0.5dB/step, 255 steps)
- Maximum input signal amplitude
  4.2Vrms (±6V power supply)
- Low distortion (THD)
  0.0002% typ. (Input=1Vrms@1kHz, Gain=0dB)
- Low residual noise
  1.2μVrms typ. (Gain=MUTE, IHF-A)
- Power supply voltage
  ±4.75V～±6.6V
- Silicon gate CMOS process.
- 24-pin plastic SSOP. The plating of pins is lead-free.(YAC526-EZ)

YAMAHA CORPORATION

YAC526 CATALOG
CATALOG No.:LSI-4AC526A2
2003.10

■Terminal configration



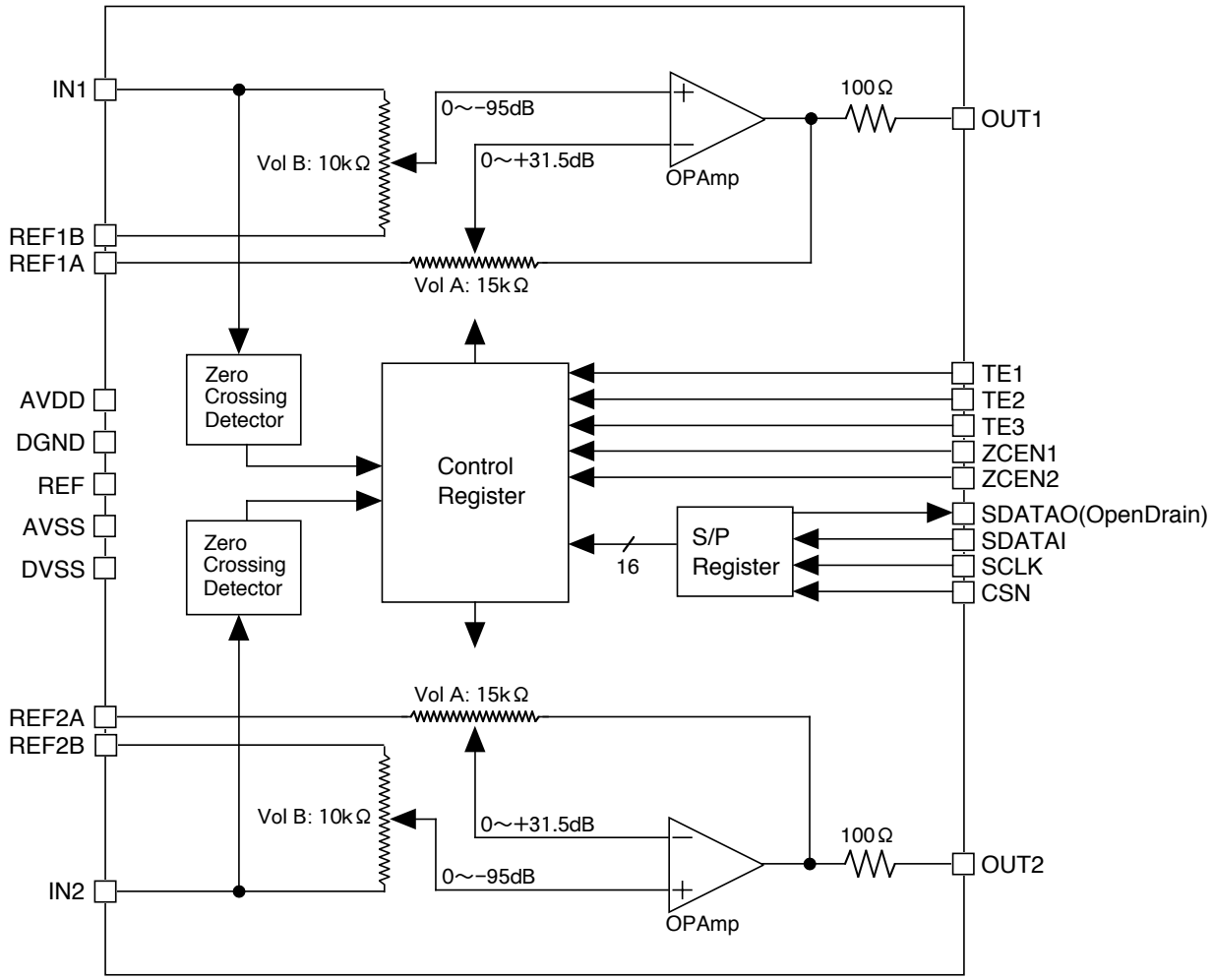
＜24 pin SSOP Top View＞

■Terminal function

No.	Name	I/O	Function
1	ZCEN1	I	Zero-cross control input 1. Select one from four types of zero-cross modes including non-zero-cross mode. When changing zero-cross modes during operation, set the system so that it changes at 1 second or more after the rise of CSN signal.
2	ZCEN2	I	Zero-cross control input 2. Select one from four types of zero-cross modes including non-zero-cross mode. When changing zero-cross modes during operation, set the system so that it changes at 1 second or more after the rise of CSN signal.
3	CSN	I	Chip select input
4	SDATAI	I	Serial data input
5	DGND	—	Digital ground
6	REF	O	Reference voltage output for digital For attaining stabilization, connect this terminal to DVSS terminal through a capacitance of 10μF or higher (C_{REF}). And please do not use this terminal output for the drive purpose of an external circuit.
7	DVSS	—	Minus power supply for digital (-6.0V Typ.)
8	SCLK	I	Serial clock input
9	SDATAO	OD	Serial data output Serial data are outputted from this terminal when CSN pin is "L" level. This terminal becomes high-impedance state when CSN pin is "H". Since it is an open drain output pin, pull it up through a resistor to the power supply voltage (to be AVDD or less) of a device to be connected. Do not allow output current of 1.5mA or over.
10	TE1	I	Test terminal (Pull-down) Non connection or connect to DGND terminal.
11	TE2	I	Test terminal (Pull-down) Non connection or connect to DGND terminal.
12	TE3	I	Test terminal (Pull-down) Non connection or connect to DGND terminal.
13	IN2	AI	ch2 analog input The output impedance of input signal source is used less than 10kΩ. When avoid the use of this terminal, connect to ground.
14	REF2A	AI	ch2 analog reference voltage input A Connect to ground directly.
15	REF2B	AI	ch2 analog reference voltage input B Connect to ground directly.
16	OUT2	AO	ch2 analog output
17	AVDD	—	Plus power supply for analog (+6.0V Typ.)
18	AVSS	—	Minus power supply for analog (-6.0V Typ.)
19	AVSS	—	Minus power supply for analog (-6.0V Typ.)
20	AVDD	—	Plus power supply for analog (+6.0V Typ.)
21	OUT1	AO	ch1 analog output
22	REF1B	AI	ch1 analog reference voltage input B Connect to ground directly.
23	REF1A	AI	ch1 analog reference voltage input A Connect to ground directly.
24	IN1	AI	ch1 analog input The output impedance of input signal source is used less than 10kΩ. When avoid the use of this terminal, connect to ground.

Note A: analog terminal, OD: Open drain output terminal, "L" level means V_{IL}, "H" level means V_{IH}.

■Block diagram



■Description of functions

●Analog functions

・Maximum input voltage

The maximum amplitude of the input signal that is inputted to the analog input pin of YAC526 is 4.2Vrms when power supply voltage is ±6V.
For a system to which a signal exceeding the power supply voltage (AVDD/AVSS) may be applied, use external diodes to suppress the signal to the maximum rating or less.

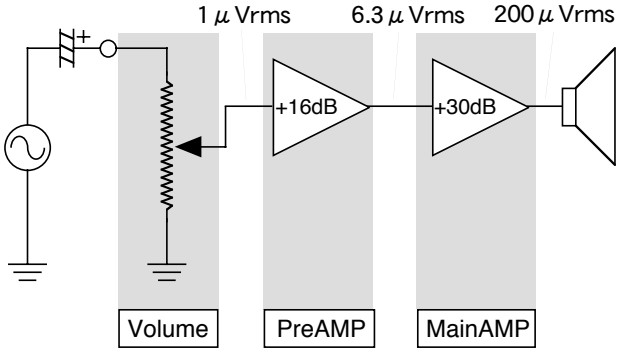
・Maximum output voltage

The maximum output voltage(THD<1%) of the signal that is outputted from the analog output pin of YAC526 is 4.2Vrms when power supply voltage is ±6V and no load is connected. The output impedance is 100Ω (typ.).

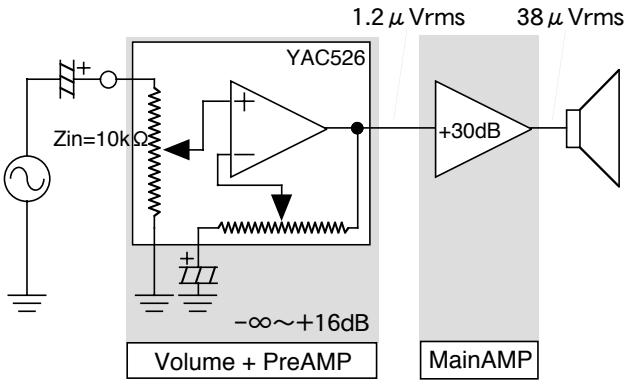
●Realization of low residual noise system

General audio amplifiers are designed to have input sensitivity of approximately 150mV, and have a gain of approximately 16dB at the preamplifier (PreAMP) section and approximately 30dB at the main amplifier section (MainAMP).
The residual noise of YAC526 (Gain=MUTE) is 1.2μVrms (typ.) which is very small, and the device has positive side gain (max: 31.5dB). Therefore, by using YAC526 also as ”PreAMP”, systems with a very small residual noise and amplification of volume control noise can be configured.
For conventional configurations that need a ”PreAMP”, even if the residual noise of the volume control itself is zero, the noise that is produced at the ”PreAMP” is amplified by the gain, the noise becomes very high when it is heard at the speakers.
When the input converted noise of ”PreAMP” is 1μV, the conventional configuration produces noise of approximately 200μV at the speakers. For the configuration that uses YAC526, the noise is 38μV which is very small.

Residual noise produced by conventional configuration



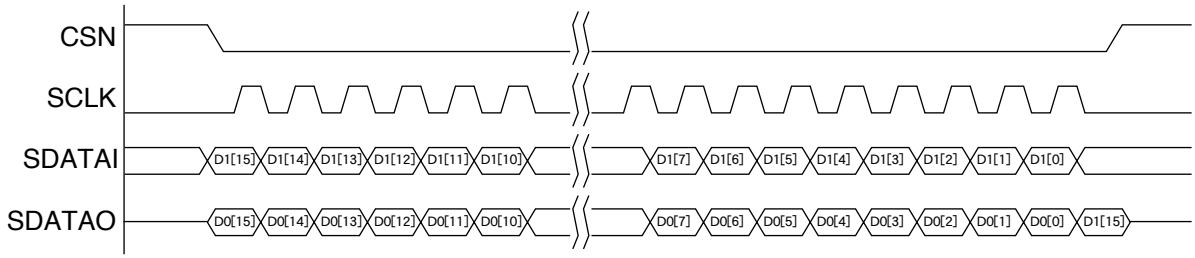
Residual noise produced by a configuration that adopts YAC526



●Digital functions

・Serial data interface

Writing of volume control data into YAC526 is performed through a serial interface. SDATAI is a serial data input pin, SCLK is a clock input pin, and CSN is a chip select pin for writing the value of volume. 16-bit serial data that is inputted from SDATAI (MSB first) is taken into YAC526 at the rising edge of SCLK when CSN terminal is at "L" level. The serial data is latched at the rising edge of CSN, and volume value of each channel is set into the register. The present volume value is outputted from SDATAO pin as serial data. With this data, the control by using daisy chain connection and verification of the present volume value can be performed easily.
Note that the register value after turning the power supply on is ALL"0" (muted state) and the interface is enabled after a predetermined period (t_{PUP}) has elapsed. (Serial access is prohibited in t_{PUP} period.)

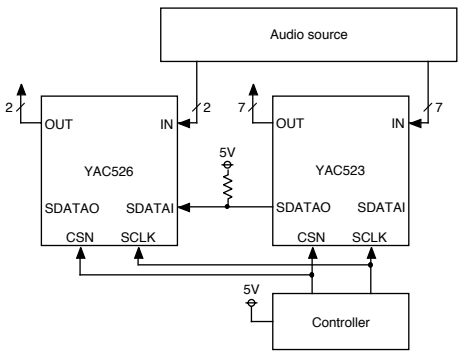


Assignment of volume control data

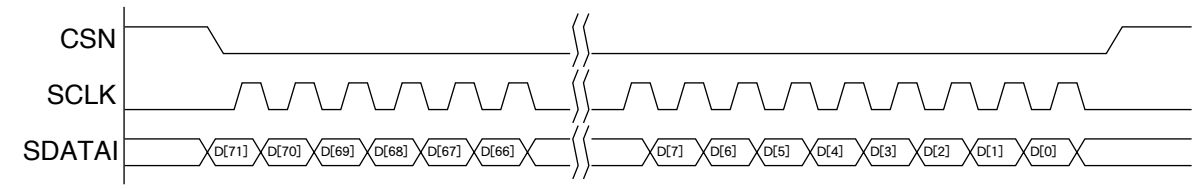
D[15: 8]	:	Channel1 Volume data	D1[15:0] is volume data value to change.
D[7: 0]	:	Channel2 Volume data	D0[15:0] is present volume data value.

・Daisy chain

YAC526 is extensible to a multichannel system with daisy chain connection.
For example, by connecting the device with YAC523 (7ch digital volume) through daisy chain, 8.1ch system can be attained. By connecting SDATAO pin of YAC526 (or YAC523) to SDATAI pin of YAC523 (or YAC526), YAC526 and YAC523 can be controlled simultaneously without need of a complex addressing.
(It is also possible to connect multiple YAC526.)
The volume data is taken into S/P (serial / parallel) registers of each LSI by setting CSN pin to "L" for 8 clock period on all channels that are connected with daisy chain. And, by setting CSN pin to "H" after the elapse of 8 clock period on all channels, the data is written from S/P registers of all YAC526 (or YAC523) that are connected with daisy chain into the control registers simultaneously to change the volume value.
Example: Assignment of volume control data when a combination of YAC526 and YAC523 as described below is used.



D[71:64]	:	[YAC526]	Channel1 Volume data
D[63:56]	:	[YAC526]	Channel2 Volume data
D[55:48]	:	[YAC523]	Channel1 Volume data
D[47:40]	:	[YAC523]	Channel2 Volume data
D[39:32]	:	[YAC523]	Channel3 Volume data
D[31:24]	:	[YAC523]	Channel4 Volume data
D[23:16]	:	[YAC523]	Channel5 Volume data
D[15: 8]	:	[YAC523]	Channel6 Volume data
D[7: 0]	:	[YAC523]	Channel7 Volume data



・Volume setting

The relationship between input code and volume value is as shown in the following table. (As for an input code, the left serves as MSB.)

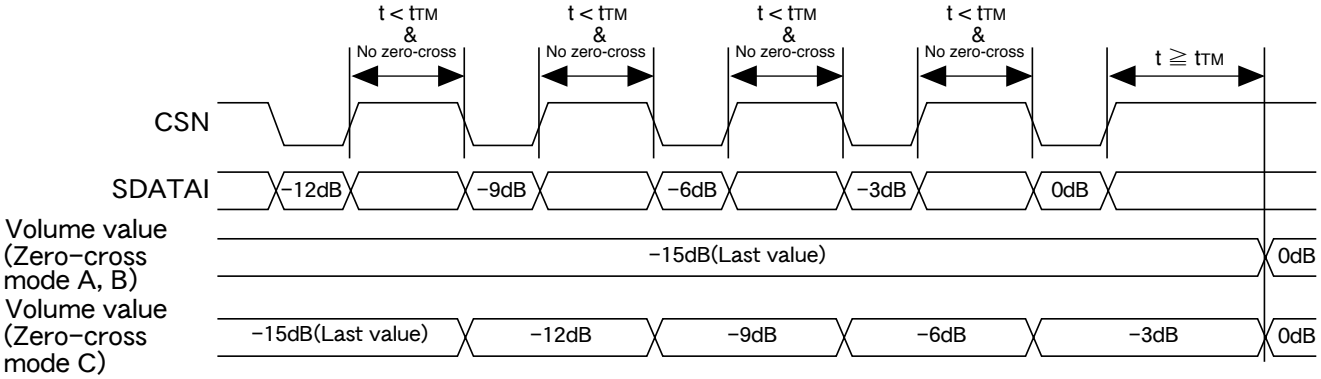
Input code	Gain or attenuate(dB)
11111111	MUTE
11111110	+31.5
・	・
・	・
11011111	+16.0
・	・
・	・
10111111	0
・	・
・	・
00000010	−94.5
00000001	−95.0
00000000	MUTE

The input codes ALL"0" and ALL"1" are set for mute.

・Zero-cross mode

YAC526 incorporates the zero-cross detection function to suppress audible noise when the volume is changed quickly. A mode is selected from the following four modes by setting ZCEN1 and 2 pins.

ZCEN[2:1]	Mode	Operation
00	Normal	Zero-cross is not detected, and the volume value is changed immediately after the rising of CSN.
01	Zero-cross mode A	Zero-cross is detected after the rising of CSN, or after t_{TM1} (20ms) passes, volume value is changed.
10	Zero-cross mode B	Zero-cross is detected after the rising of CSN, or after t_{TM2} (10ms) passes, volume value is changed.
11	Zero-cross mode C	When the next data is written within t_{TM1} (20ms) for zero-cross mode A, the changed is performed at the falling of CSN by using the volume value immediately before.



Operation in each zero-cross mode when zero-cross is not detected

※Be careful not to change the zero-cross mode during the operation of the device, or an erroneous operation may be caused. Perform change of zero-cross mode after the elapse of 1 second or more from the rising of CSN signal.

・Power on reset

YAC526 builds in the power on reset function that resets the volume value when the power is turned on. Since a system that perform the reset by detecting the power supply voltage level, when turning on the power supply again, do it after the power supply voltage AVDD and AVSS has reduced sufficiently (to +1.0V/ -1.0V or less). Moreover, although a volume register is reset at the time of a power supply injection, since shocking sound occurs in the case of power supply ON/OFF, please apply mute to the whole set.

■Electrical characteristics

1.Absolute maximum rating

Item	Symbol	Min.	Max.	Unit
Power supply voltage	AV_{DD}-AV_{SS}		14.0	V
Analog input terminal voltage	VIN_A	AV_{SS} -0.6	AV_{DD}+0.6 and V_{INA}-AV_{SS} < 14.0V	V
Digital input terminal voltage	VIN_D	AV_{SS} -0.3	AV_{DD}+0.3 and V_{IND}-AV_{SS} < 14.0V	V
Storage temperature	T_{STG}	-50	125	℃

Note : Please use AV_{SS} and DV_{SS} with the same potential.
DGND=0V

2. Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Analog power supply voltage(Positive)	AV_{DD}	4.75	6.00	6.60	V
Analog power supply voltage(Negative)	AV_{SS}	-6.60	-6.00	-4.75	V
(AV_{SS}=DV_{SS})	DV_{SS}	-6.60	-6.00	-4.75	V
Operating ambient temperature	Ta	-40		85	℃

Note : Please use AV_{SS} and DV_{SS} with the same potential.
DGND=0V

3. Analog characteristics (Ta=25℃, AV_{DD}=+6.0V, AV_{SS}=-6.0V, DV_{SS}=-6.0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Gain range	Gain	-95.0		+31.5	dB
Step size			0.5		dB
Gain matching between channel (0～-40dB, 1kHz)			±0.1		dB
Gain matching between channel (@-80dB, 1kHz)			±0.2		dB
Step error (≧-80dB)			±0.1		dB
Input resistance	R_I		10		kΩ
Output resistance	R_O		100		Ω
Load resistance	R_L	5			kΩ
Input capacitance	C_I			10	pF
Load capacitance	C_L			100	pF
Maximum input voltage (THD<1%, R_L=∞)	V_I			4.2	Vrms
Maximum output voltage (THD<1%, R_L=∞)	V_O			4.2	Vrms
Output noise voltage1 (In=GND, Vol=+16dB) *1	V_{n1}		10.0		μVrms
Output noise voltage2 (In=GND, Vol=0dB) *1	V_{n2}		2.5		μVrms
Output noise voltage3 (In=GND, Vol=Mute) *1	V_{n3}		1.2		μVrms
Total harmonic distortion (In=1Vrms, Vol=0dB, 1kHz) *2	THD1		0.0002		%
Total harmonic distortion (In=1Vrms, Vol=0dB, 20kHz) *3	THD2		0.0025		%
Inter channel isolation (Vol=0dB, 1kHz)	Cs		-130		dB

Note : *1 : Input of other channels are analog ground, Band Width=IHF-A
*2 : Input of other channels are analog ground, Band Width=400Hz～30kHz
*3 : Input of other channels are analog ground, Band Width=400Hz～

4. Power consumption

Item	Symbol	Min.	Typ.	Max.	Unit
Power consumption(AV_{DD}=+6V, AV_{SS}=-6V, CSN="H")	P_D		150		mW

5. DC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		2.2		AV_{DD}+0.3	V
Low level input voltage	V_{IL}		-0.3		0.8	V
Low level output voltage	V_{OL}	I_O= 1.5mA			0.4	V
Input leakage current	I_{LI}				10	μA

6. AC characteristics (C_L=20pF)

Item	Symbol	Min.	Typ.	Max.	Unit
Serial clock frequency	SCLK	0		1.0	MHz
Serial clock pulse width high	t_{PH}	500			ns
Serial clock pulse width Low	t_{PL}	500			ns
SDATAI set up time	t_{SDVS}	200			ns
SDATAI hold time	t_{SDH}	200			ns
CSN pulse width High	t_{CSPH}	1000			ns
CSN set up time	t_{CSVS}	500			ns
CSN hold time	t_{LTH}	200			ns
SDATAO data output set up time	t_{CSH}			300	ns
SDATAO output delay time	t_{SSD}			300	ns
SDATAO output data hold time (data output stop)	t_{CSDH}			200	ns
CSN, SCLK rise time	t_R			100	ns
CSN, SCLK fall time	t_F			100	ns
Zero-cross time out (Zero-cross MODE=A, C)	t_{TM1}		20		ms
Zero-cross time out (Zero-cross MODE=B)	t_{TM2}		10		ms
Regulation time until the data writing from a power supply injection (more than AVSS=90%) to LSI becomes effective. (C_{REF}=10 μF)	t_{PUP}		200	400	ms

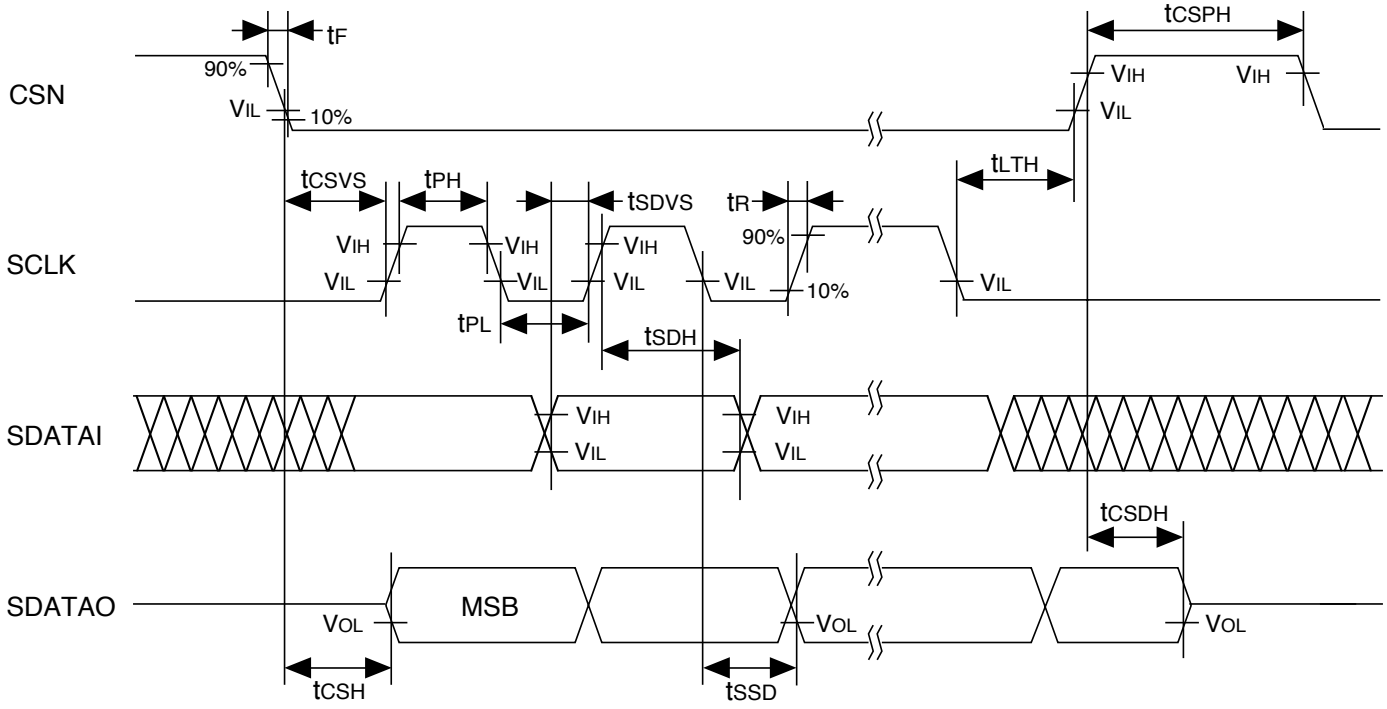
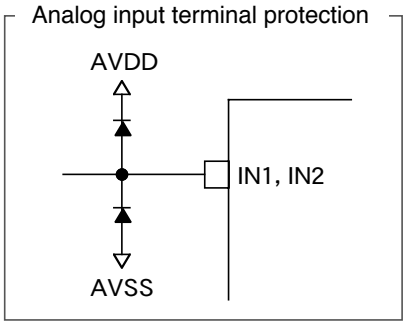
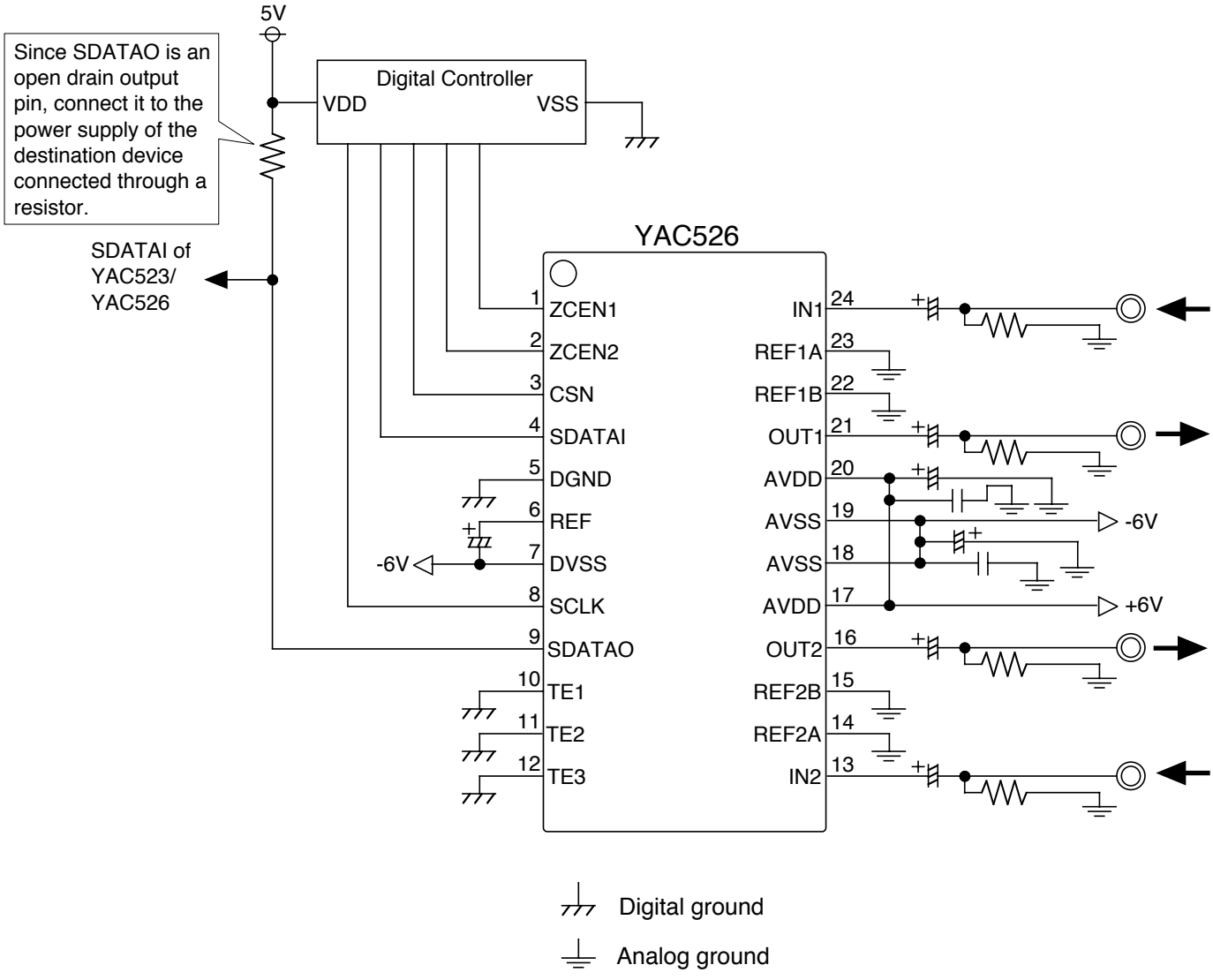


Fig 1 Serial port timing

■Example of system configuration

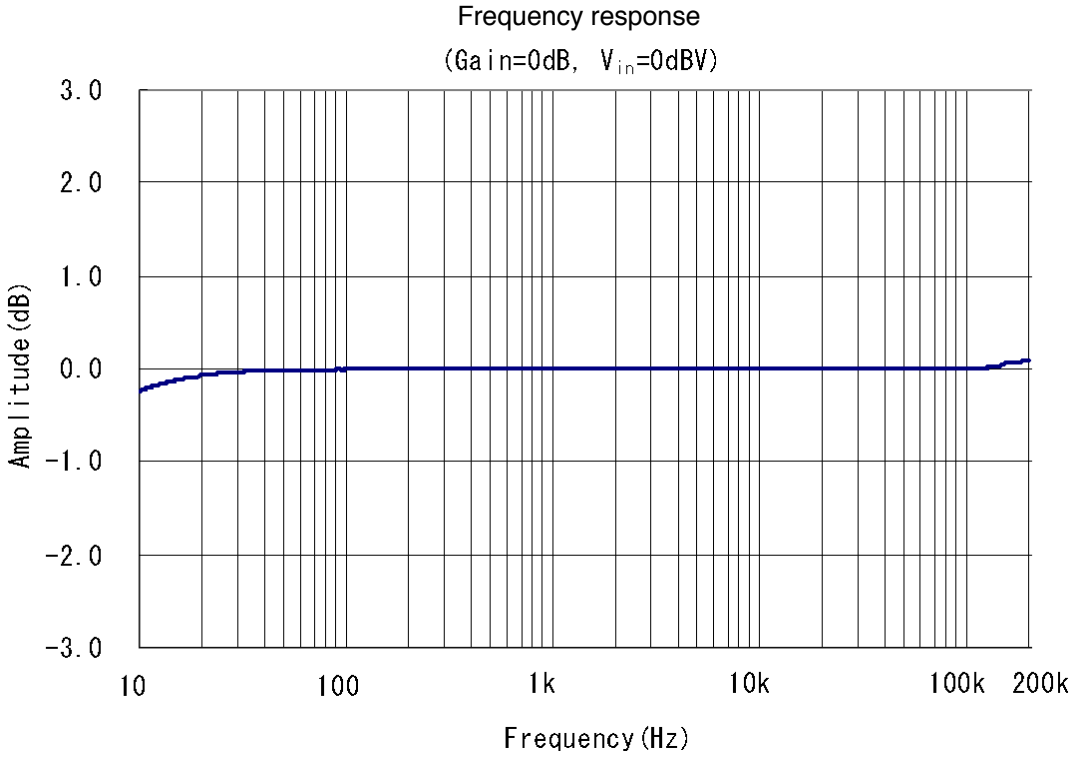
When there is a fear that voltage exceeding the maximum rating is applied to the analog input pins (IN1 and IN2) of YAC526, connect diodes between AVDD and AVSS as shown below to prevent application of voltage exceeding the maximum rating to the input pins.
Please make an analog domain and a digital domain into the ground side separated, respectively, and arrange YAC526 to an analog domain and the impedance to an AVSS pin should become small as much as possible.
And please secure an area large enough, and a radiation noise should fully be stopped and an analog ground and a digital ground also make it.
Control signals, such as serial interface, should wire a digital ground side collectively. In order to prevent interference with a control signal and an analog signal, be careful for an analog signal and a digital signal not to cross or not to adjoin.

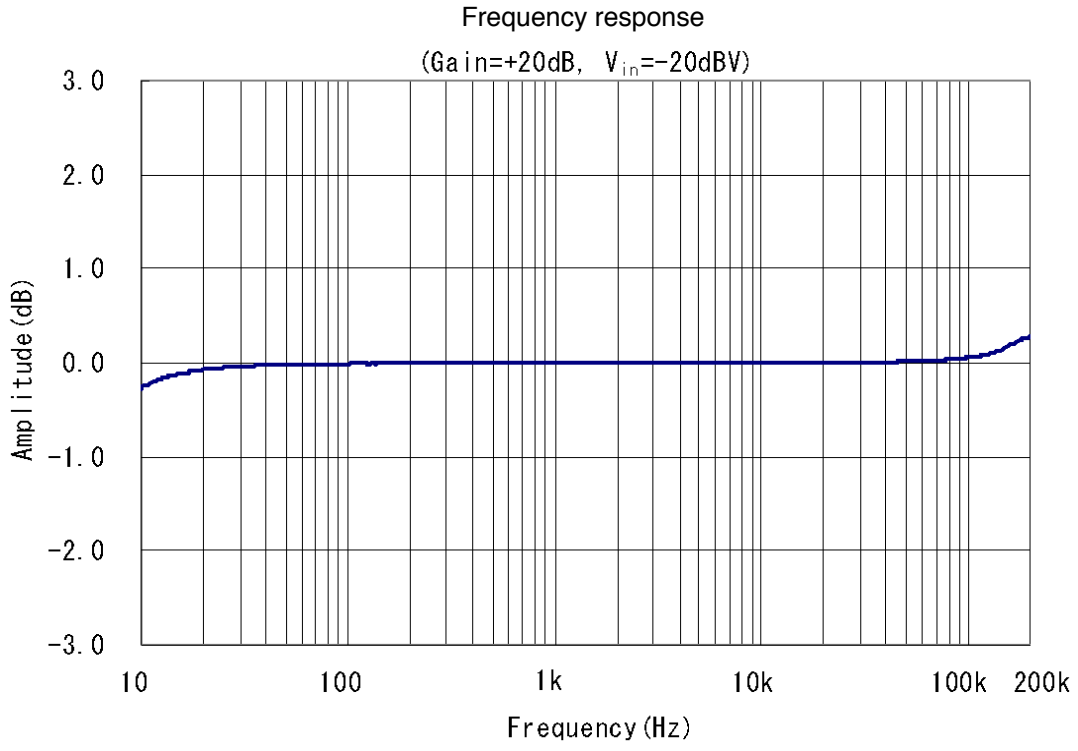




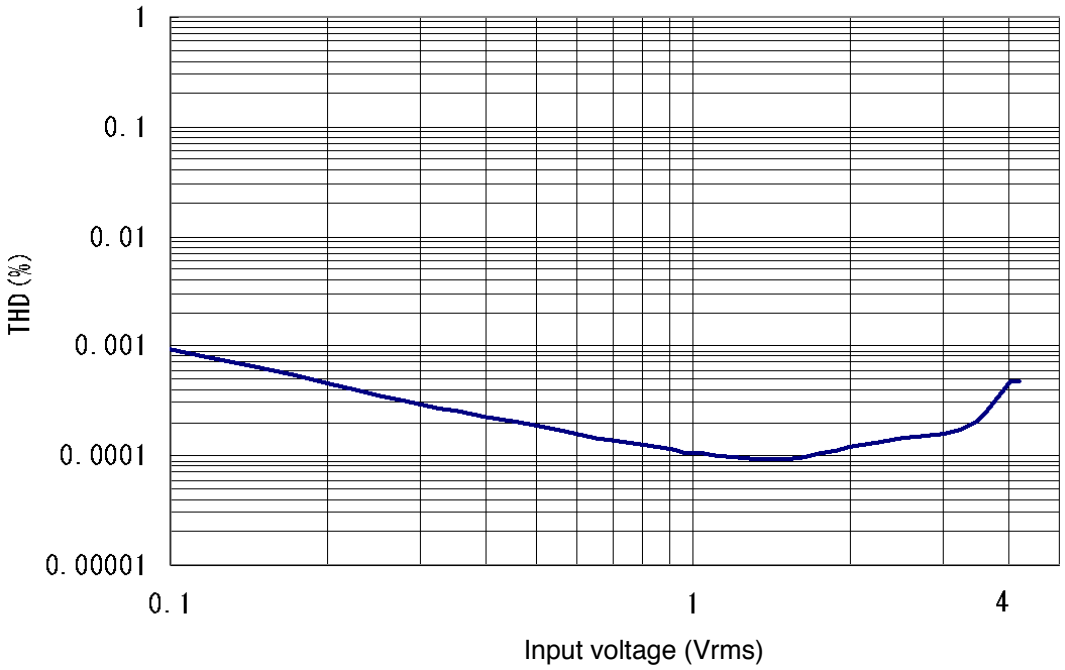
■Typical analog characteristic

As long as there is no description especially, it is Ta=+25°C, AVDD=+6V, AVSS=-6V, DVSS=-6V, RL=10kΩ, CL=100pF.

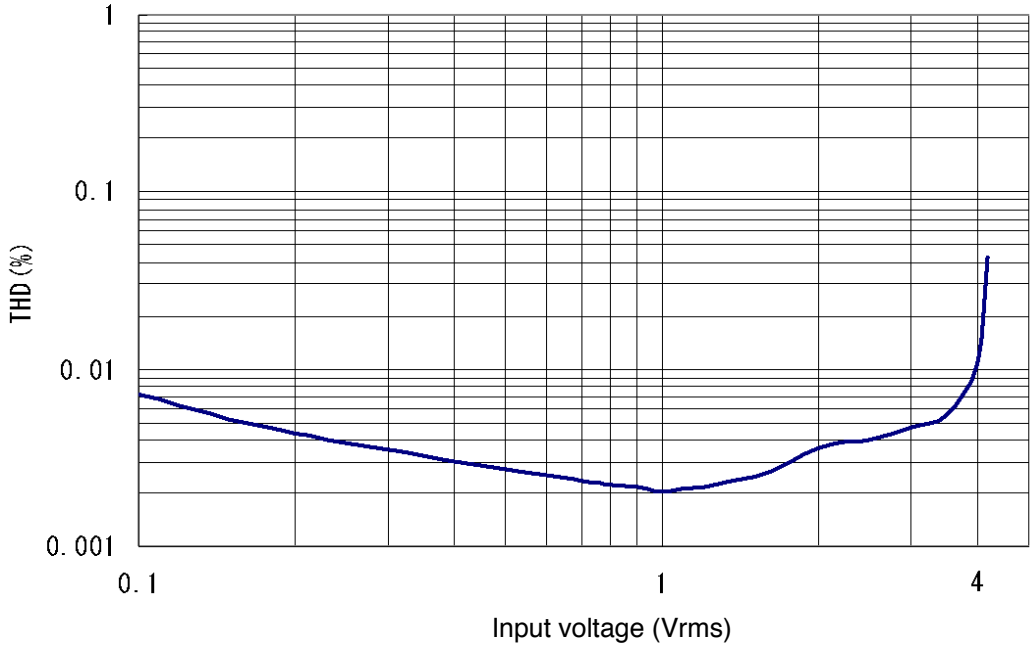




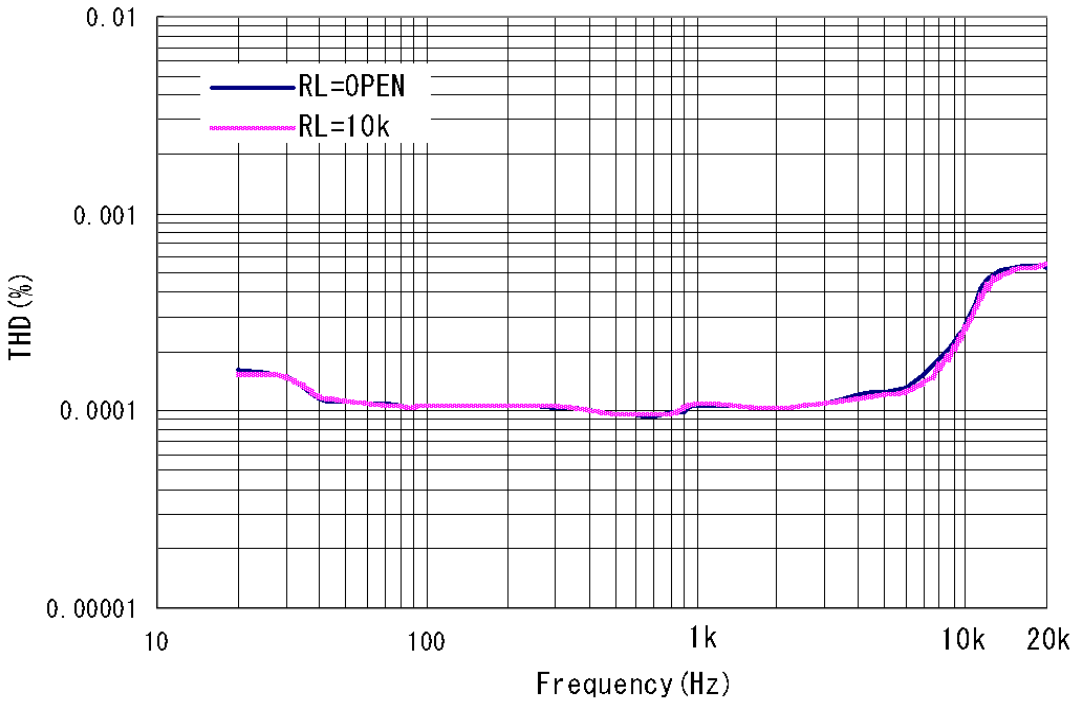
THD vs Input voltage 1kHz
(Gain=0dB, BW measure=400Hz～30kHz)



THD vs Input voltage 20kHz
(Gain=0dB, BW measure=400Hz～)

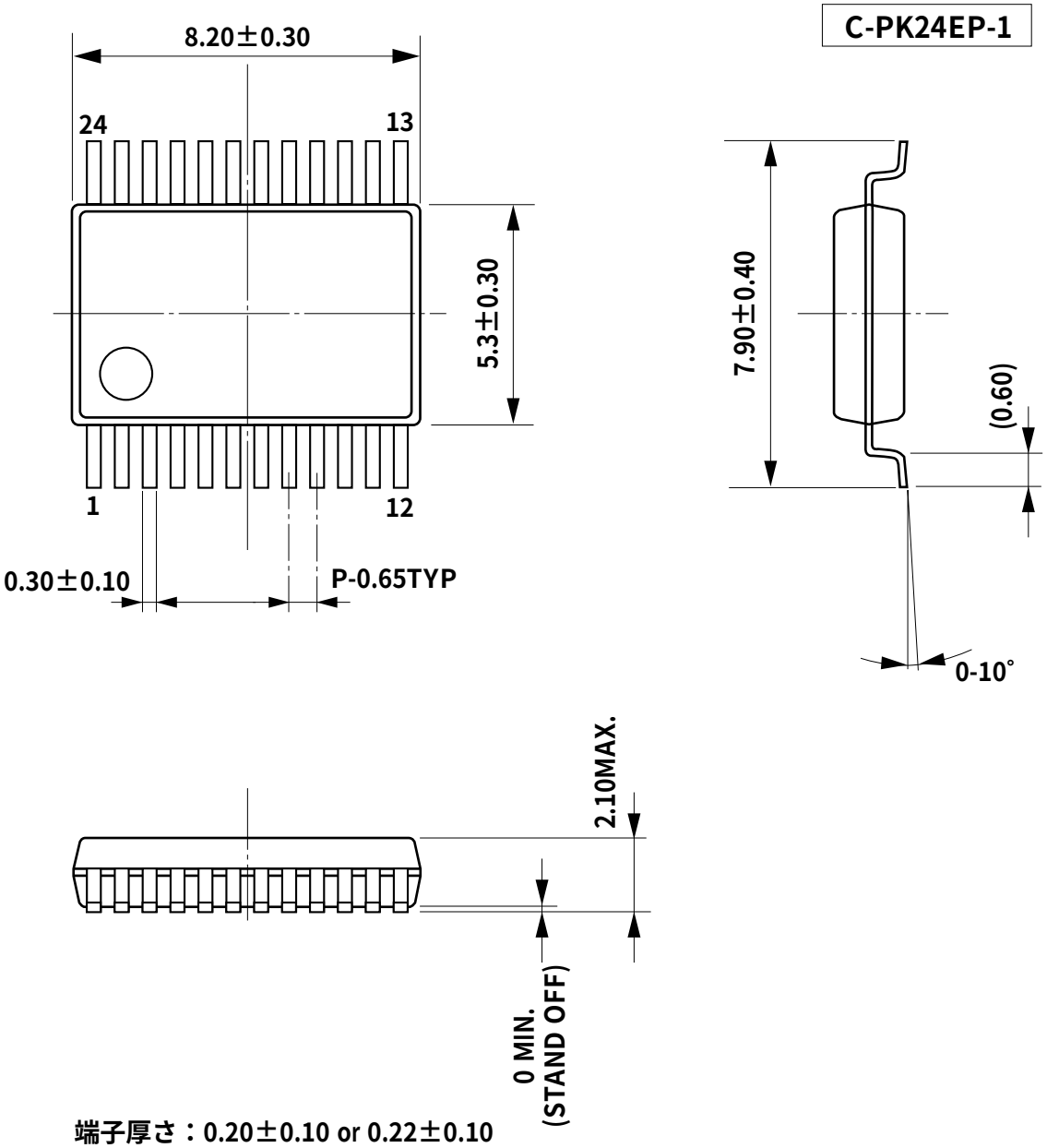


THD vs Frequency (RL=OPEN, 10kΩ)
(V_{IN}=0dBV, BW measure=～30kHz)



■ External dimensions of package

C-PK24EP-1



端子厚さ：0.20±0.10 or 0.22±0.10
(LEAD THICKNESS)

カッコ内の寸法値は参考値とする。
モールド外形寸法はバリを含まない。
単位(UNIT) : mm (millimeters)

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

注）表面実装 LSI は保管条件及び、半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせ下さい。

Note:The storage and soldering of LSIs for surface mounting need special consideration.
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