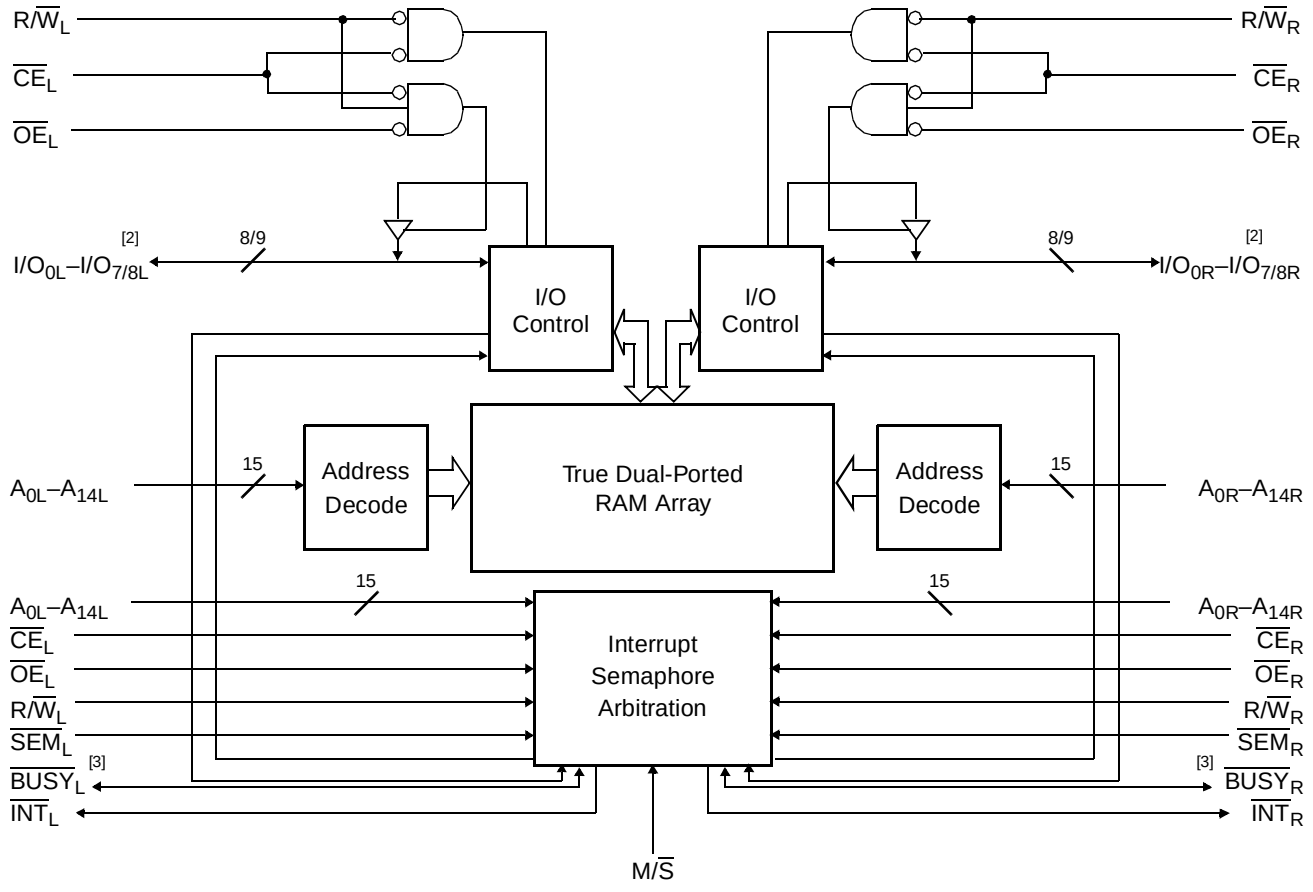
CY7C006A
CY7C007A
CY7C017A

32K/16K x 8, 32K x 9 Dual-Port Static RAM

Features

- True dual-ported memory cells which allow simultaneous access of the same memory location
- 16K x 8 organization (CY7C006A)
- 32K x 8 organization (CY7C007A)
- 32K x 9 organization (CY7C017A)
- 0.35-micron CMOS for optimum speed/power
- High-speed access: 12[1]/15/20 ns
- Low operating power
  - Active: I_{CC} = 180 mA (typical)
  - Standby: I_{SB3} = 0.05 mA (typical)
- Fully asynchronous operation
- Automatic power-down
- Expandable data bus to 16/18 bits or more using Master/Slave chip select when using more than one device
- On-chip arbitration logic
- Semaphores included to permit software handshaking between ports
- $\overline{INT}$ flags for port-to-port communication
- Pin select for Master or Slave
- Commercial temperature range
- Available in 68-pin PLCC (CY7C006A, CY7C007A and CY7C017A), 64-pin TQFP (CY7C006A), and in 80-pin TQFP (CY7C007A)
- Pin-compatible and functionally equivalent to IDT7006 and IDT7007

Logic Block Diagram



Notes:
1. See page 5 for Load Conditions.
2. I/O_0–I/O_7 for x8 devices; I/O_0–I/O_8 for x9 devices.
3. $\overline{BUSY}$ is an output in master mode and an input in slave mode.

Functional Description

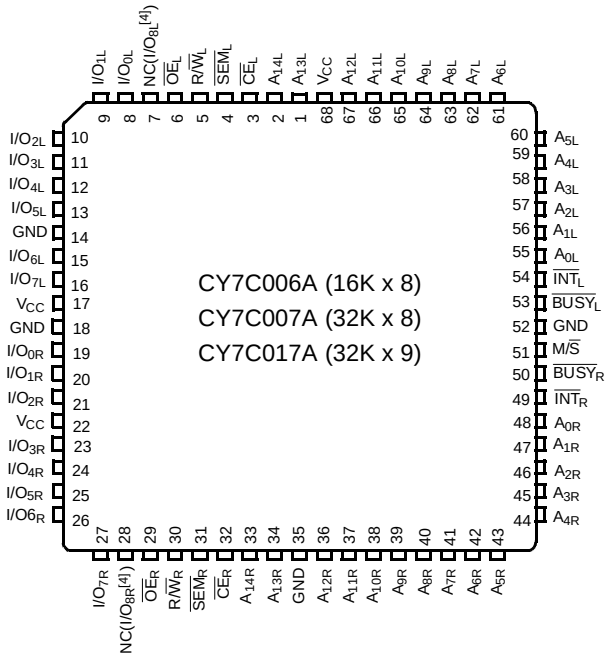
The CY7C006A, CY7C007A, and CY7C017A are low-power CMOS 32K x 8/9 and 16K x 8 dual-port static RAMs. Various arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The devices can be utilized as standalone 8/9-bit dual-port static RAMs or multiple devices can be combined in order to function as a 16/18-bit or wider master/slave dual-port static RAM. An M/$\overline{S}$ pin is provided for implementing 16/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: Chip Enable ($\overline{CE}$), Read or Write Enable (R/$\overline{W}$), and Output Enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The Interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a Chip Select ($\overline{CE}$) pin.

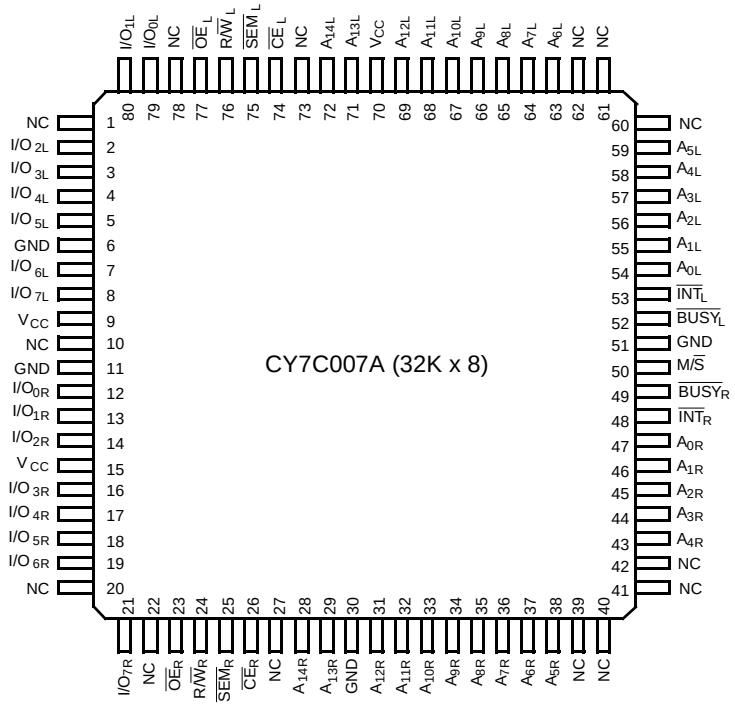
The CY7C006A, CY7C007A, and CY7C017A are available in 68-pin PLCC packages, the CY7C006A is also available in 64-pin TQFP, and the CY7C007A is also available in 80-pin TQFP packages.

Pin Configurations

68-Pin PLCC
Top View



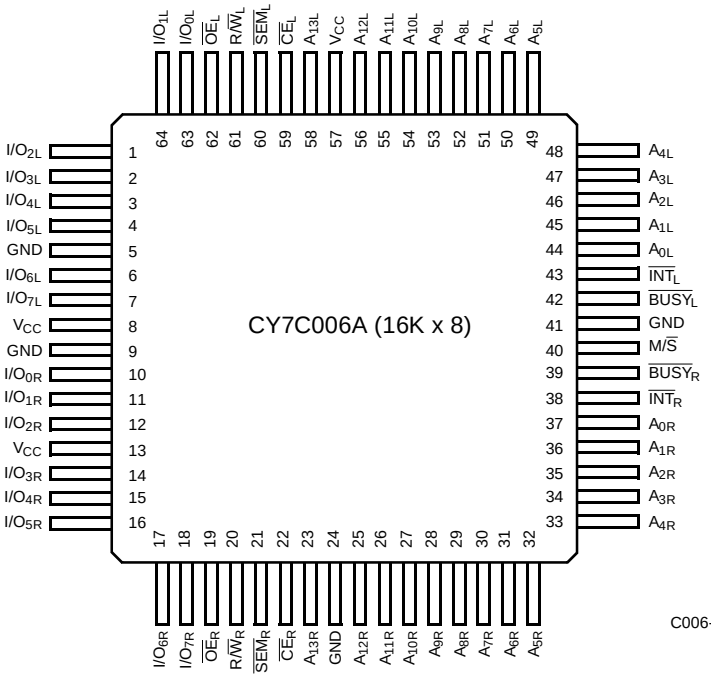
80-Pin TQFP
Top View



Note:
4. This pin is I/O for CY7C017A only.

Pin Configurations (continued)

64-Pin TQFP
Top View



Selection Guide

	CY7C006A CY7C007A CY7C017A -12[1]	CY7C006A CY7C007A CY7C017A -15	CY7C006A CY7C007A CY7C017A -20
Maximum Access Time (ns)	12	15	20
Typical Operating Current (mA)	195	190	180
Typical Standby Current for I_{SB1} (mA) (Both Ports TTL level)	55	50	45
Typical Standby Current for I_{SB3} (mA) (Both Ports CMOS level)	0.05	0.05	0.05

Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L}–A_{14L}	A_{0R}–A_{14R}	Address
I/O_{0L}–I/O_{8L}	I/O_{0R}–I/O_{8R}	Data Bus Input/Output (I/O_0–I/O_7 for x8 devices and I/O_0–I/O_8 for x9)
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground
NC		No Connect

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.3V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage[5]..... –0.5V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >2001V

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description		CY7C006A CY7C007A CY7C017A									Unit
			-12[1]			-15			-20			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage (V_{CC}=Min., I_{OH}= –4.0 mA)		2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage (V_{CC}=Min., I_{OH}= +4.0 mA)				0.4			0.4			0.4	V
V_{IH}	Input HIGH Voltage		2.2			2.2			2.2			V
V_{IL}	Input LOW Voltage				0.8			0.8			0.8	V
I_{OZ}	Output Leakage Current		–10		10	–10		10	–10		10	µA
I_{CC}	Operating Current (V_{CC} = Max., I_{OUT} = 0 mA) Outputs Disabled	Com'l.		195	325		190	280		180	275	mA
		Ind.					215	305				mA
I_{SB1}	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ & $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Com'l.		55	75		50	70		45	65	mA
		Ind.					65	95				mA
I_{SB2}	Standby Current (One Port TTL Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Com'l.		125	205		120	180		110	160	mA
		Ind.					135	205				mA
I_{SB3}	Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC}$ – 0.2V, f = 0	Com'l.		0.05	0.5		0.05	0.5		0.05	0.5	mA
		Ind.					0.05	0.5				mA
I_{SB4}	Standby Current (One Port CMOS Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}[6]	Com'l.		115	185		110	160		100	140	mA
		Ind.					125	175				mA

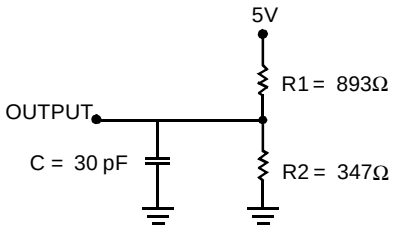
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

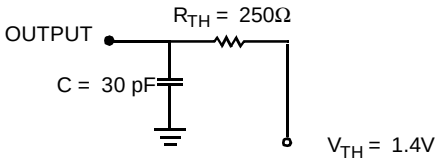
Notes:

5. Pulse width < 20 ns.
6. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.
7. Tested initially and after any design or process changes that may affect these parameters.

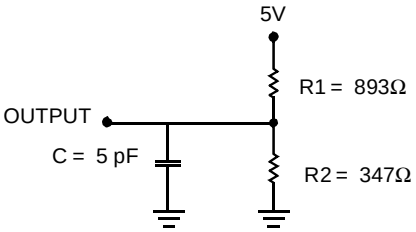
AC Test Loads and Waveforms



(a) Normal Load (Load 1)

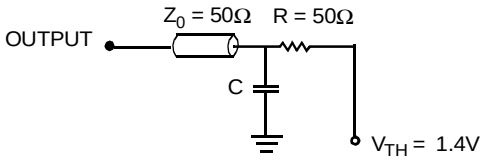


(b) Thévenin Equivalent (Load 1)

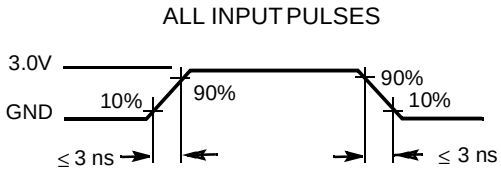


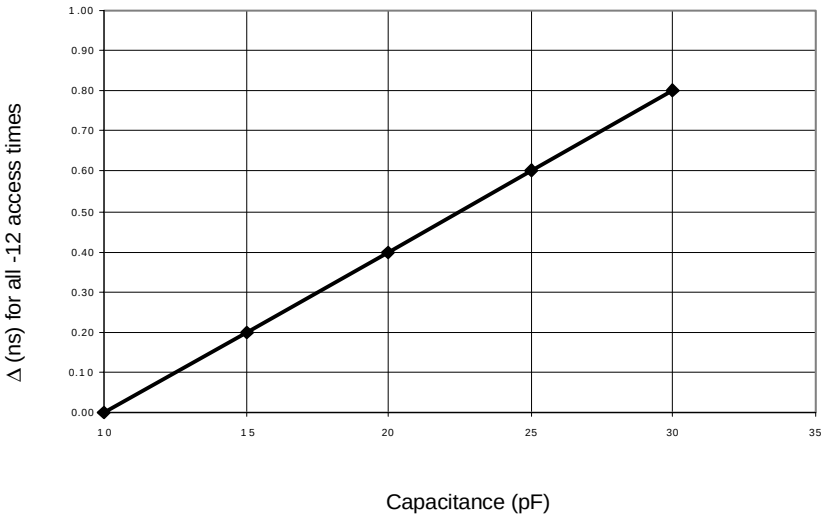
(c) Three-State Delay (Load 2)
(Used for t_{LZ}, t_{HZ}, t_{HZWE}, & t_{LZWE} including scope and jig)

AC Test Loads (Applicable to -12 only)[8]



(a) Load 1 (-12 only)





(b) Load Derating Curve

Note:
8. Test Conditions: C = 10 pF.

Switching Characteristics Over the Operating Range[9]

Parameter	Description	CY7C006A CY7C007A CY7C017A						Unit
		–12[1]		–15		–20		
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Output Hold From Address Change	3		3		3		ns
t_{ACE}[10]	$\overline{CE}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10		12	ns
t_{LZOE}[11, 12, 13]	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}[11, 12, 13]	$\overline{OE}$ HIGH to High Z		10		10		12	ns
t_{LZCE}[11, 12, 13]	$\overline{CE}$ LOW to Low Z	3		3		3		ns
t_{HZCE}[11, 12, 13]	$\overline{CE}$ HIGH to High Z		10		10		12	ns
t_{PU}[13]	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}[13]	$\overline{CE}$ HIGH to Power-Down		12		15		20	ns
t_{ABE}[10]	Byte Enable Access Time		12		15		20	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCE}[10]	$\overline{CE}$ LOW to Write End	10		12		15		ns
t_{AW}	Address Valid to Write End	10		12		15		ns
t_{HA}	Address Hold From Write End	0		0		0		ns
t_{SA}[10]	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	Write Pulse Width	10		12		15		ns
t_{SD}	Data Set-Up to Write End	10		10		15		ns
t_{HD}[16]	Data Hold From Write End	0		0		0		ns
t_{HZWE}[12, 13]	R/$\overline{W}$ LOW to High Z		10		10		12	ns
t_{LZWE}[12, 13]	R/$\overline{W}$ HIGH to Low Z	3		3		3		ns
t_{WDD}[14]	Write Pulse to Data Delay		25		30		45	ns
t_{DDD}[14]	Write Data Valid to Read Data Valid		20		25		30	ns
BUSY TIMING[15]								
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		12		15		20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		12		15		20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		12		15		20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		12		15		17	ns
t_{PS}	Port Set-Up for Priority	5		5		5		ns

Notes:

9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
10. To access RAM, $\overline{CE}$=L, $\overline{SEM}$=H. To access semaphore, $\overline{CE}$=H and $\overline{SEM}$=L. Either condition must be valid for the entire t_{SCE} time.
11. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
12. Test conditions used are Load 3.
13. This parameter is guaranteed but not tested.
14. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
15. Test conditions used are Load 2.
16. For 15 ns industrial parts t_{HD} Min. is 0.5 ns.

Switching Characteristics Over the Operating Range[9] (continued)

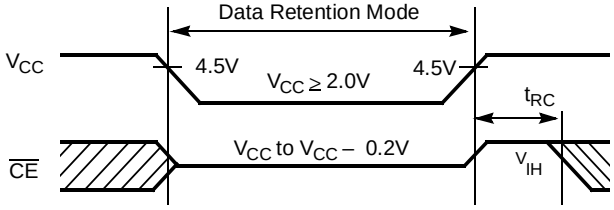
Parameter	Description	CY7C006A CY7C007A CY7C017A						Unit
		–12[1]		–15		–20		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WB}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave)	0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	11		13		15		ns
t_{BDD}[17]	$\overline{BUSY}$ HIGH to Data Valid		12		15		20	ns
INTERRUPT TIMING[15]								
t_{INS}	$\overline{INT}$ Set Time		12		15		20	ns
t_{INR}	$\overline{INT}$ Reset Time		12		15		20	ns
SEMAPHORE TIMING								
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		10		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		ns
t_{SAA}	SEM Address Access Time		12		15		20	ns

Data Retention Mode

The CY7C006A, CY7C007A, and CY7C017A are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip enable ($\overline{CE}$) must be held HIGH during data retention, within V_{CC} to V_{CC} – 0.2V.
2. $\overline{CE}$ must be kept between V_{CC} – 0.2V and 70% of V_{CC} during the power-up and power-down transitions.
3. The RAM can begin operation >t_{RC} after V_{CC} reaches the minimum operating voltage (4.5 volts).

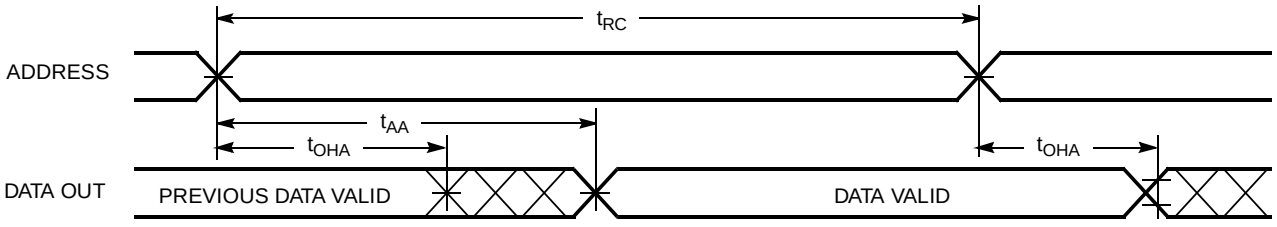
Timing



Parameter	Test Conditions[18]	Max.	Unit
ICC_{DR1}	@ VCC_{DR} = 2V	1.5	mA

Switching Waveforms

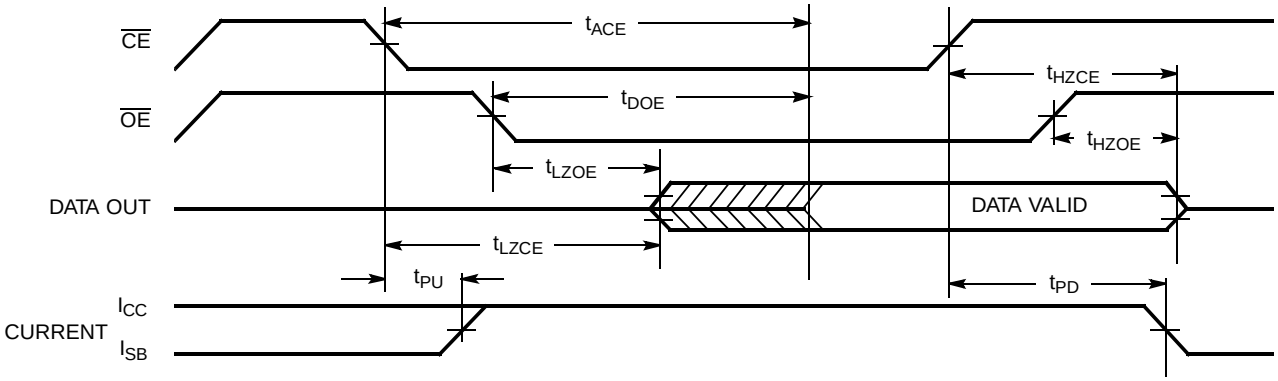
Read Cycle No. 1 (Either Port Address Access)[19, 20, 21]



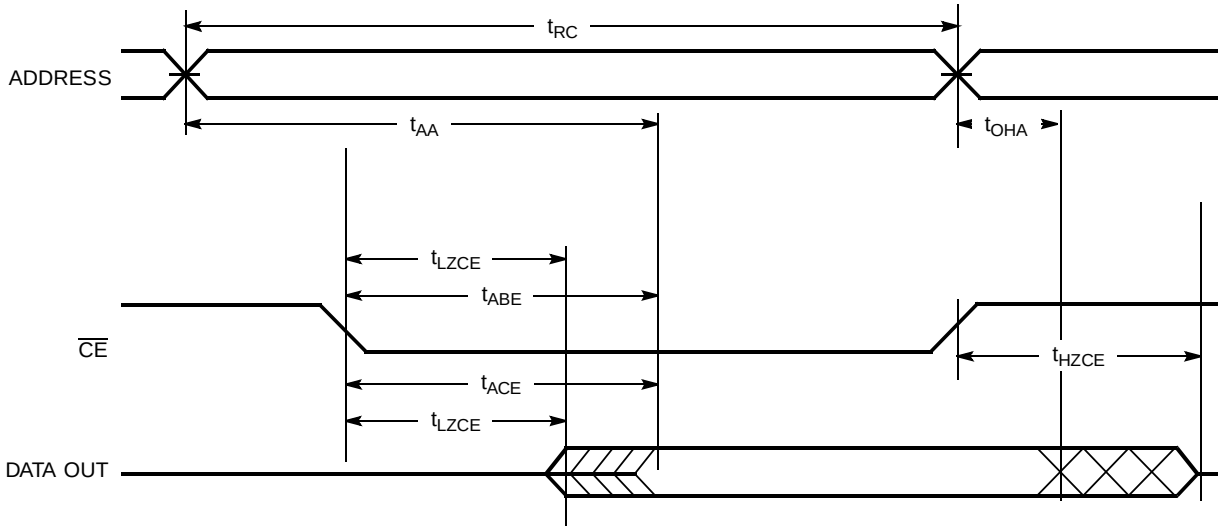
Notes:
17. t_{BDD} is a calculated parameter and is the greater of t_{WDD}–t_{PWE} (actual) or t_{DDD}–t_{SD} (actual).
18. $\overline{CE}$ = V_{CC}, V_{in} = GND to V_{CC}, T_A = 25°C. This parameter is guaranteed but not tested.
19. R/$\overline{W}$ is HIGH for read cycles.
20. Device is continuously selected $\overline{CE}$ = V_{IL}. This waveform cannot be used for semaphore reads.
21. $\overline{OE}$ = V_{IL}.

Switching Waveforms (continued)

Read Cycle No. 2 (Either Port $\overline{CE}$/$\overline{OE}$ Access)[19, 22, 23]



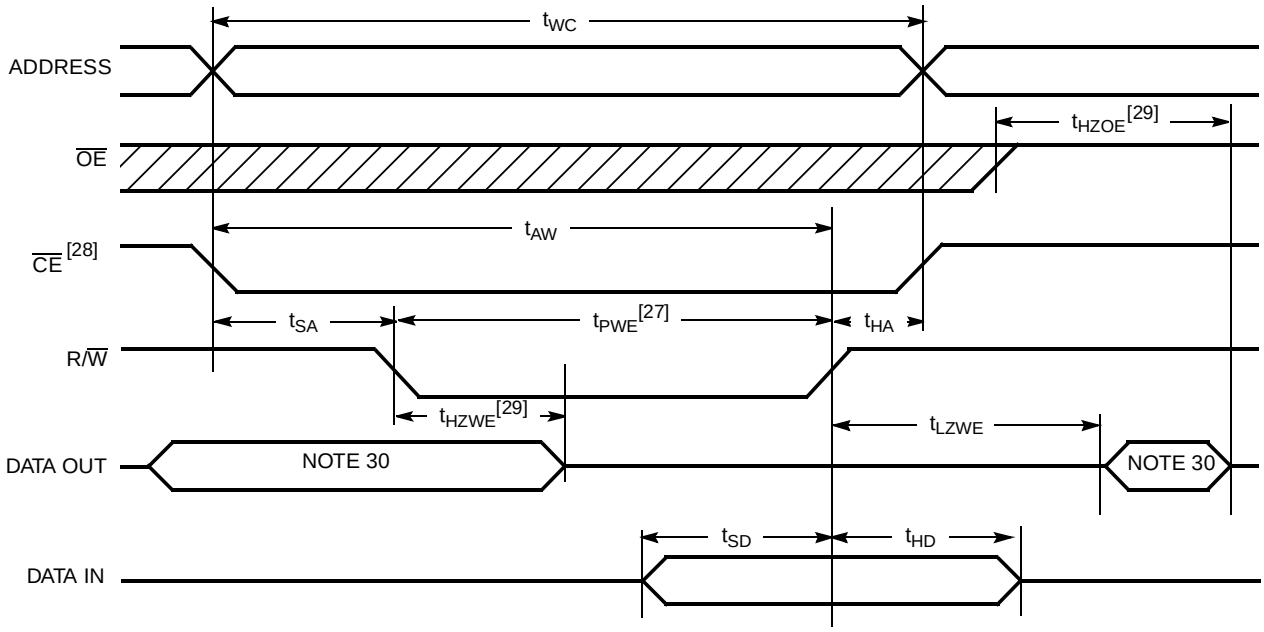
Read Cycle No. 3 (Either Port)[19, 21, 22, 23]



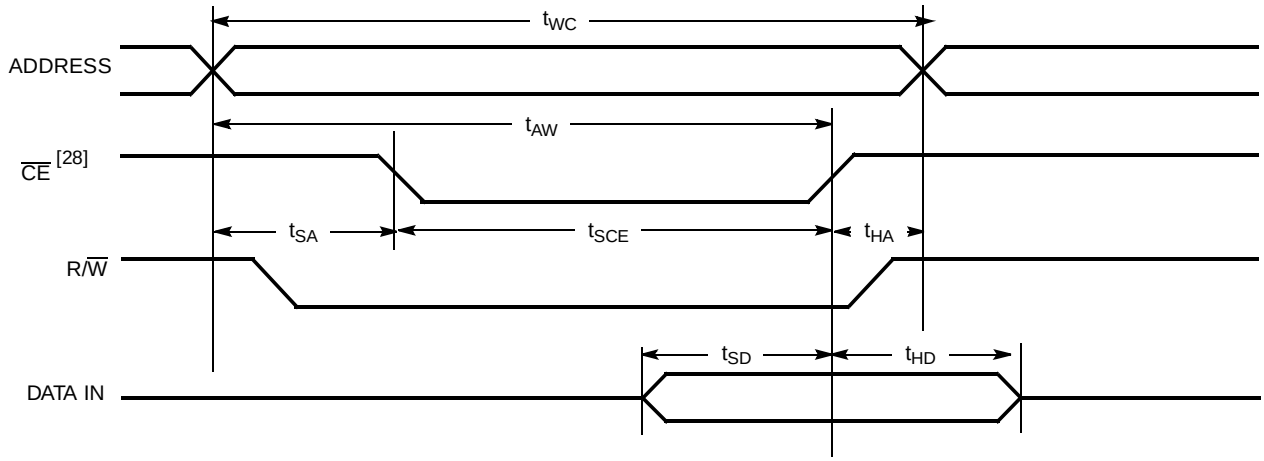
Notes:
22. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
23. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$.

Switching Waveforms (continued)

Write Cycle No. 1: R/$\overline{W}$ Controlled Timing [24, 25, 26, 27]



Write Cycle No. 2: $\overline{CE}$ Controlled Timing [24, 25, 26, 31]

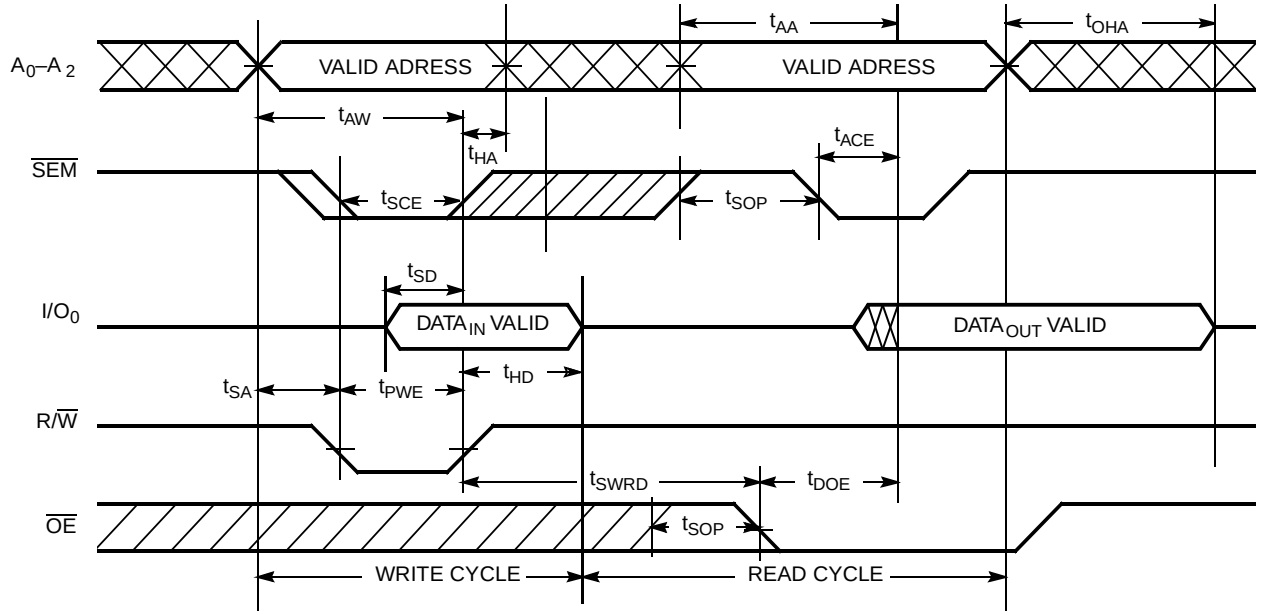


Notes:

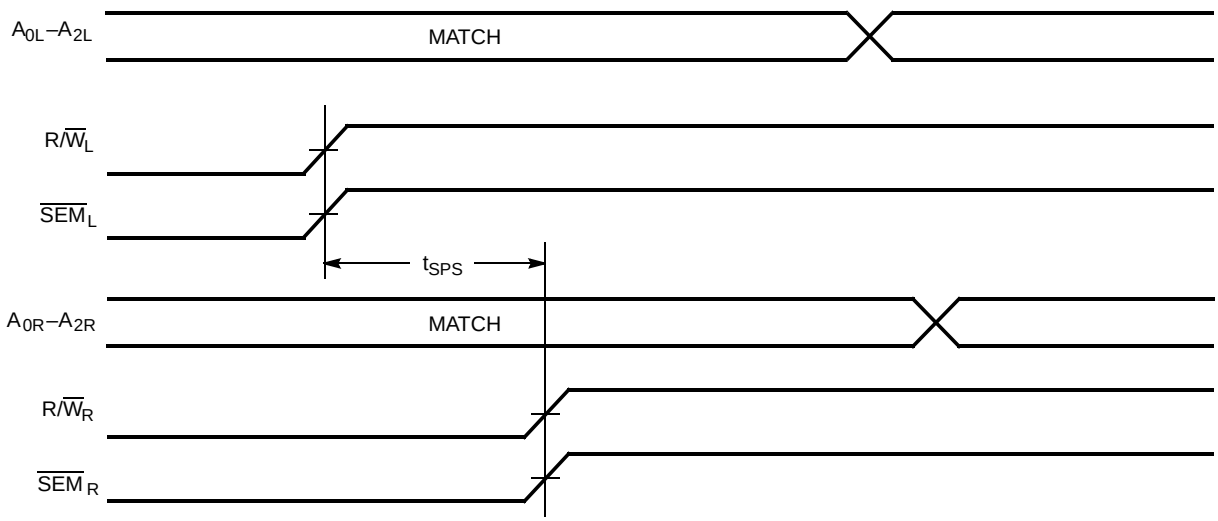
24. R/$\overline{W}$ must be HIGH during all address transitions.
25. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW $\overline{CE}$ or $\overline{SEM}$.
26. t_{HA} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ or ($\overline{SEM}$ or R/$\overline{W}$) going HIGH at the end of write cycle.
27. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or ($t_{HZWE} + t_{SD}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
28. To access RAM, $\overline{CE} = V_{IL}$, $\overline{SEM} = V_{IH}$.
29. Transition is measured ±500 mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
30. During this period, the I/O pins are in the output state, and input signals must not be applied.
31. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[32]



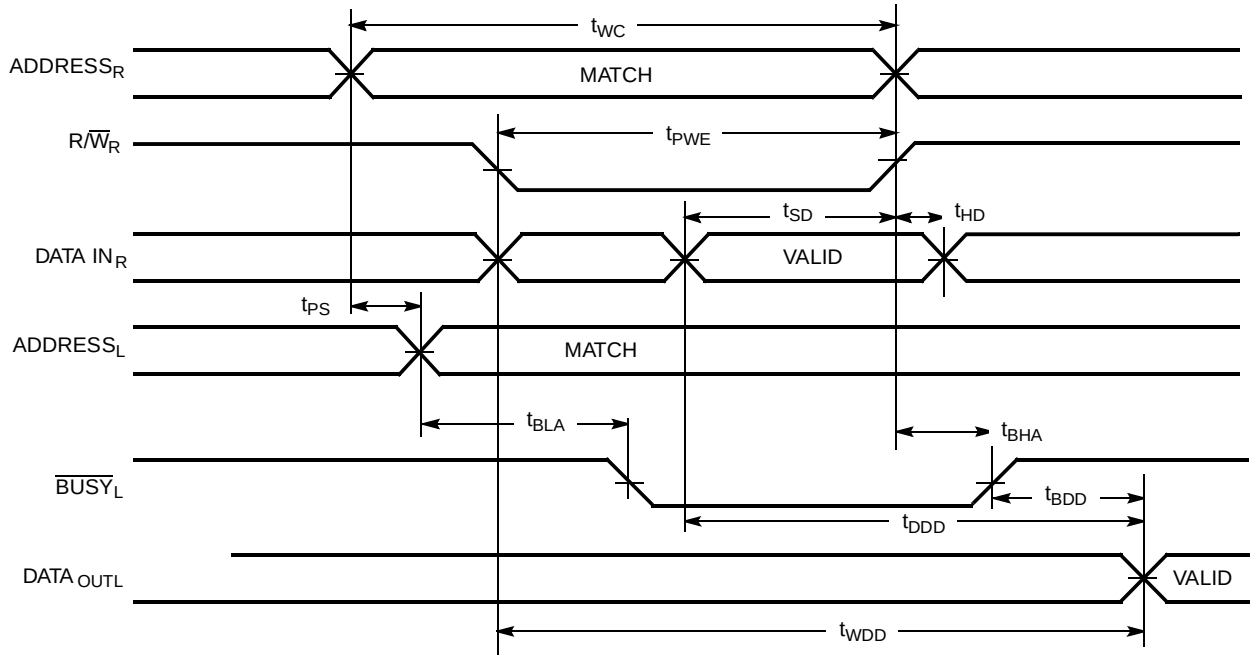
Timing Diagram of Semaphore Contention[33, 34, 35]



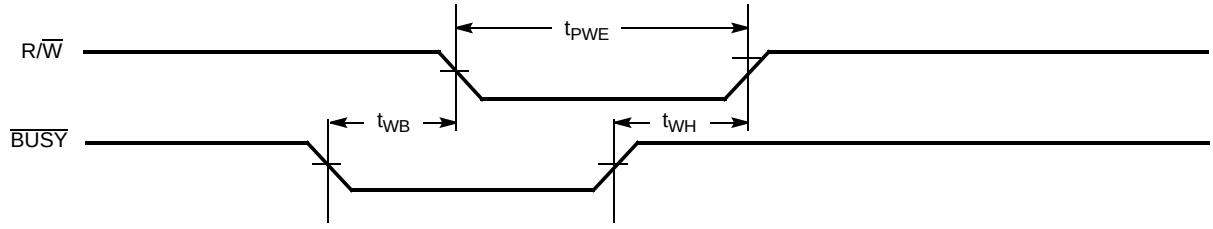
Notes:
32. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
33. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH.
34. Semaphores are reset (available to both ports) at cycle start.
35. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but which side will get the semaphore is unpredictable.

Switching Waveforms (continued)

Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[36]



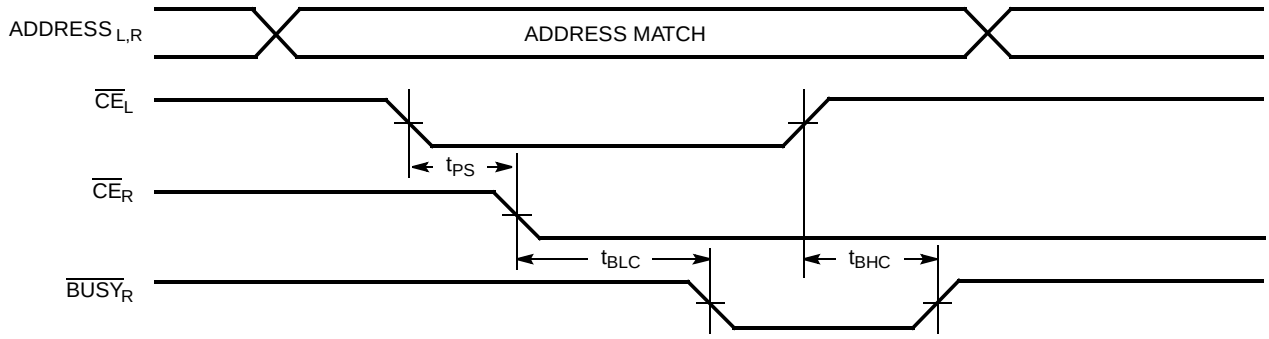
Write Timing with Busy Input (M/$\overline{S}$=LOW)



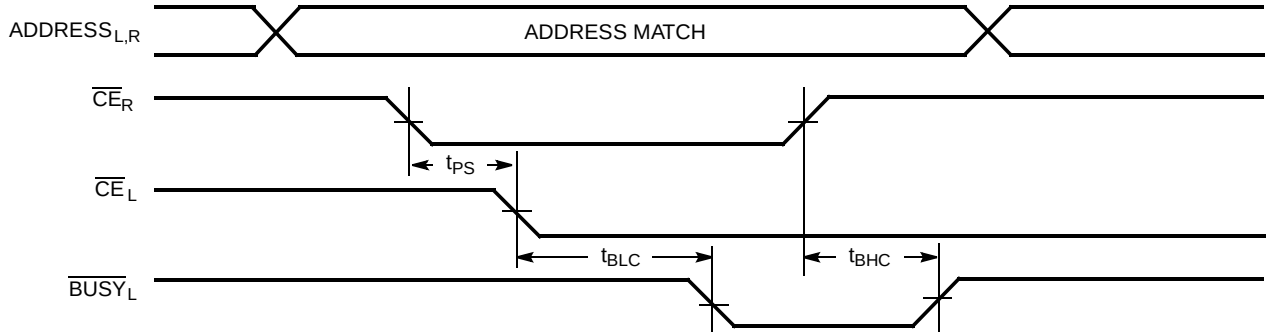
Note:
36. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

Switching Waveforms (continued)

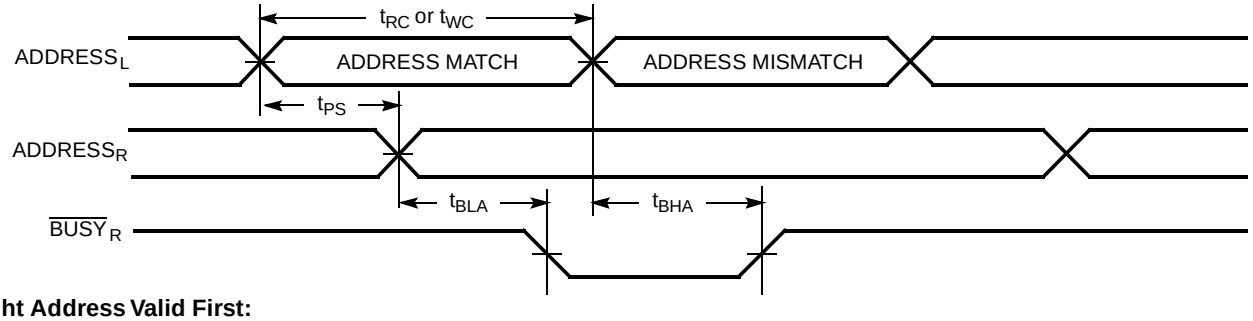
Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[37]
$\overline{CE}_L$ Valid First:



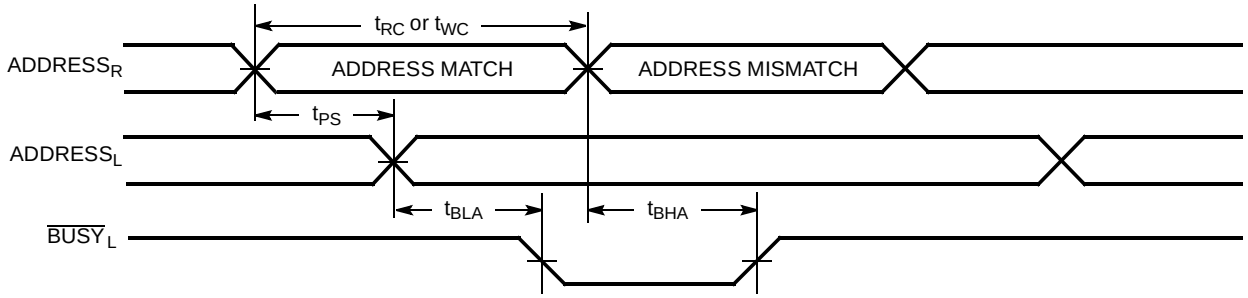
$\overline{CE}_R$ Valid First:



Busy Timing Diagram No. 2 (Address Arbitration)[37]
Left Address Valid First:



Right Address Valid First:

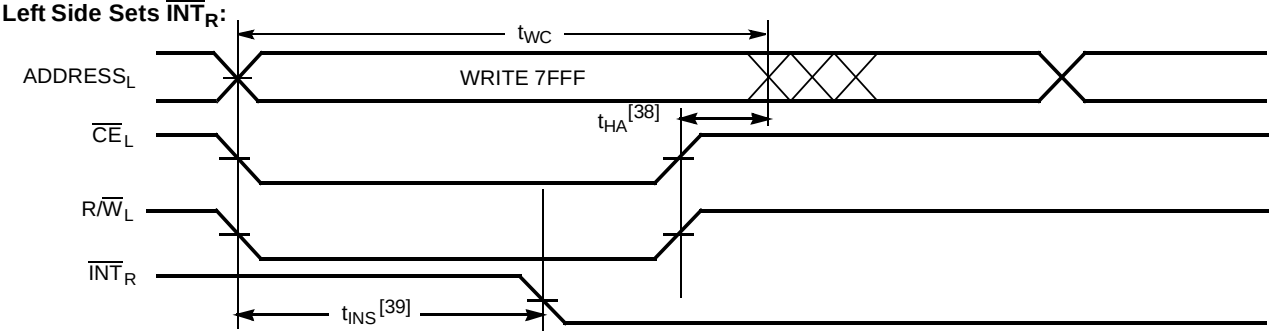


Note:
37. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ will be asserted.

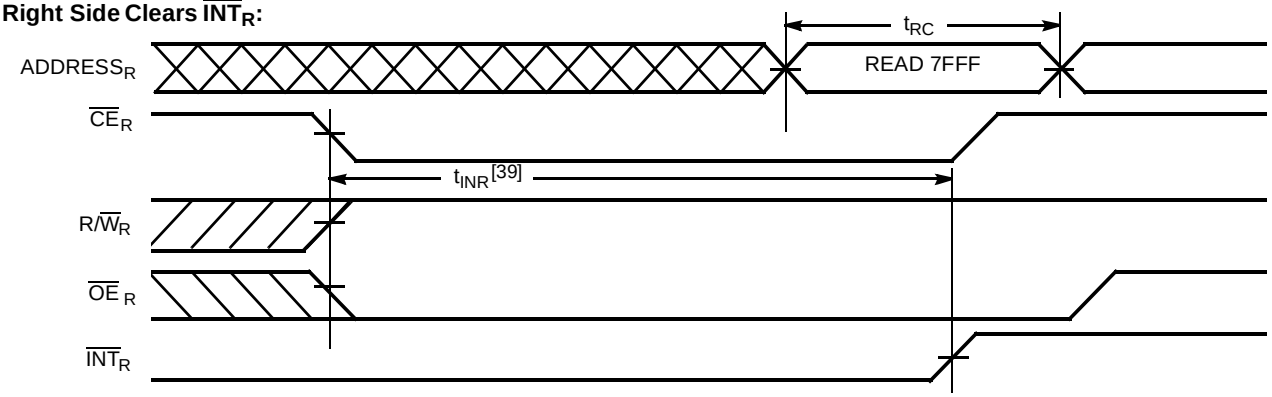
Switching Waveforms (continued)

Interrupt Timing Diagrams

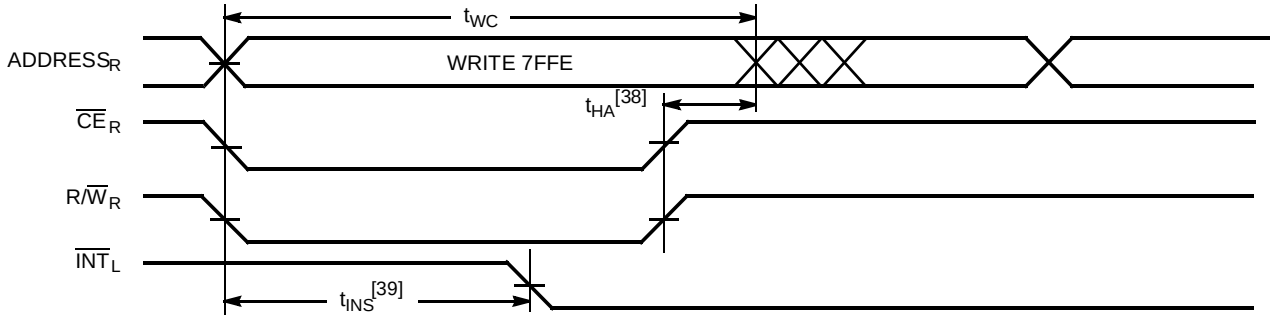
Left Side Sets $\overline{INT}_R$:



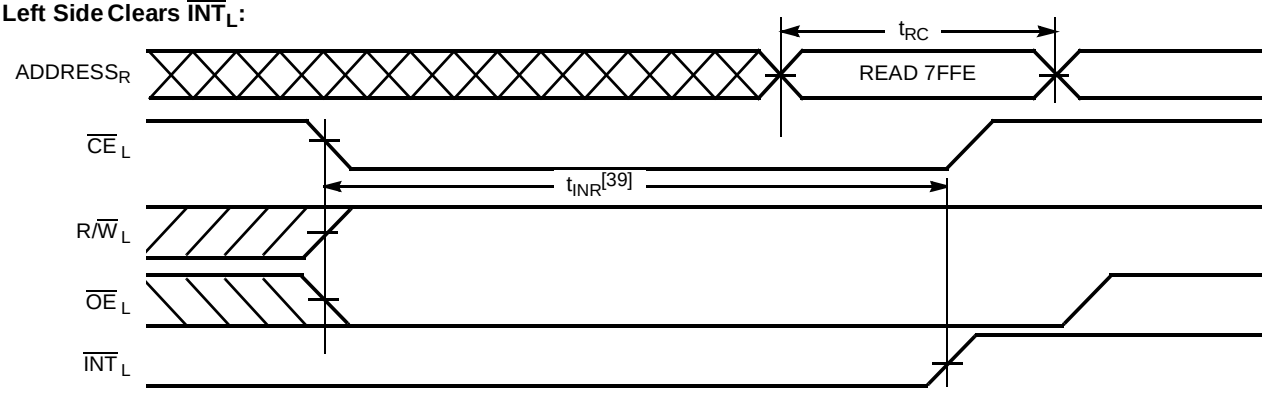
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$:



Notes:

38. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
39. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

Architecture

The CY7C006A, CY7C007A, and CY7C017A consist of an array of 32K/16K words of 8 bits and 32K words of 9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the devices can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The devices also have an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the R/$\overline{W}$ pin (see Write Cycle No. 1 waveform) or the $\overline{CE}$ pin (see Write Cycle No. 2 waveform). Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin, and $\overline{OE}$ must also be asserted.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (7FFF) is the mailbox for the right port and the second-highest memory location (7FFE) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy are summarized in *Table 2.*

Busy

The CY7C006A, CY7C007A, and CY7C017A provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other, the busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not predictable which port will get that permission. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW.

Master/Slave

A M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the $\overline{BUSY}$ input has settled (t_{BLC} or t_{BLA}), otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/$\overline{S}$ pin allows the device to be used as a master and, therefore, the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C006A, CY7C007A, and CY7C017A provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip select for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an available semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Table 1. Non-Contending Read/Write

Inputs				Outputs	Operation
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O_0–I/O_8	
H	X	X	H	High Z	Deselected: Power-Down
H	H	L	L	Data Out	Read Data in Semaphore Flag
X	X	H	X	High Z	I/O Lines Disabled
H	⎍	X	L	Data In	Write into Semaphore Flag
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Not Allowed

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$=$\overline{BUSY}_R$=HIGH)

	Left Port					Right Port				
Function	R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L–14L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R–14R}$	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	X	7FFF	X	X	X	X	X	L[41]
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	X	X	L	L	7FFF	H[40]
Set Left $\overline{INT}_L$ Flag	X	X	X	X	L[40]	L	L	X	7FFE	X
Reset Left $\overline{INT}_L$ Flag	X	L	L	7FFE	H[41]	X	X	X	X	X

Table 3. Semaphore Operation Example

Function	I/O_0–I/O_8 Left	I/O_0–I/O_8Right	Status
No action	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left Port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free

Notes:
40. If $\overline{BUSY}_R$ = L, then no change.
41. If $\overline{BUSY}_L$ = L, then no change.

Ordering Information

16K x8 Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12[1]	CY7C006A-12AC	A65	64-Pin Thin Quad Flat Pack	Commercial
	CY7C006A-12JC	J81	68-Pin Plastic Leaded Chip Carrier	Commercial
15	CY7C006A-15AC	A65	64-Pin Thin Quad Flat Pack	Commercial
	CY7C006A-15AI	A65	64-Pin Thin Quad Flat Pack	Industrial
	CY7C006A-15JC	J81	68-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C006A-15JI	J81	68-Pin Plastic Leaded Chip Carrier	Industrial
20	CY7C006A-20AC	A65	64-Pin Thin Quad Flat Pack	Commercial
	CY7C006A-20JC	J81	68-Pin Plastic Leaded Chip CarrieR	Commercial

32K x8 Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12[1]	CY7C007A-12AC	A80	80-Pin Thin Quad Flat Pack	Commercial
	CY7C007A-12JC	J81	68-Pin Plastic Leaded Chip Carrier	Commercial
15	CY7C007A-15AC	A80	80-Pin Thin Quad Flat Pack	Commercial
	CY7C007A-15AI	A80	80-Pin Thin Quad Flat Pack	Industrial
	CY7C007A-15JC	J81	68-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C007A-15JI	J81	68-Pin Plastic Leaded Chip Carrier	Industrial
20	CY7C007A-20AC	A80	80-Pin Thin Quad Flat Pack	Commercial
	CY7C007A-20JC	J81	68-Pin Plastic Leaded Chip CarrieR	Commercial

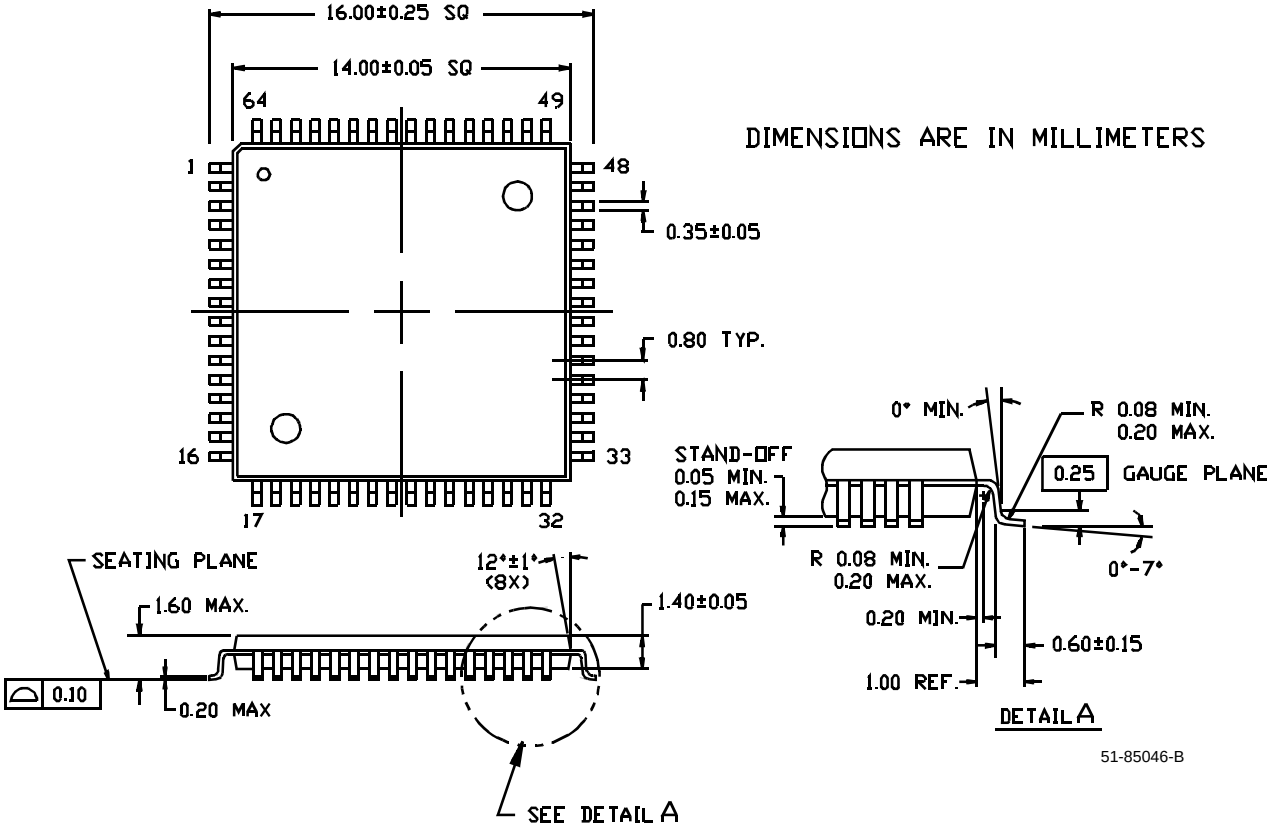
32K x9 Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12[1]	CY7C017A-12JC	J81	68-Pin Plastic Leaded Chip Carrier	Commercial
15	CY7C017A-15JC	J81	68-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C017A-15JI	J81	68-Pin Plastic Leaded Chip Carrier	Industrial
20	CY7C017A-20JC	J81	68-Pin Plastic Leaded Chip Carrier	Commercial

Document #: 38–00831–A

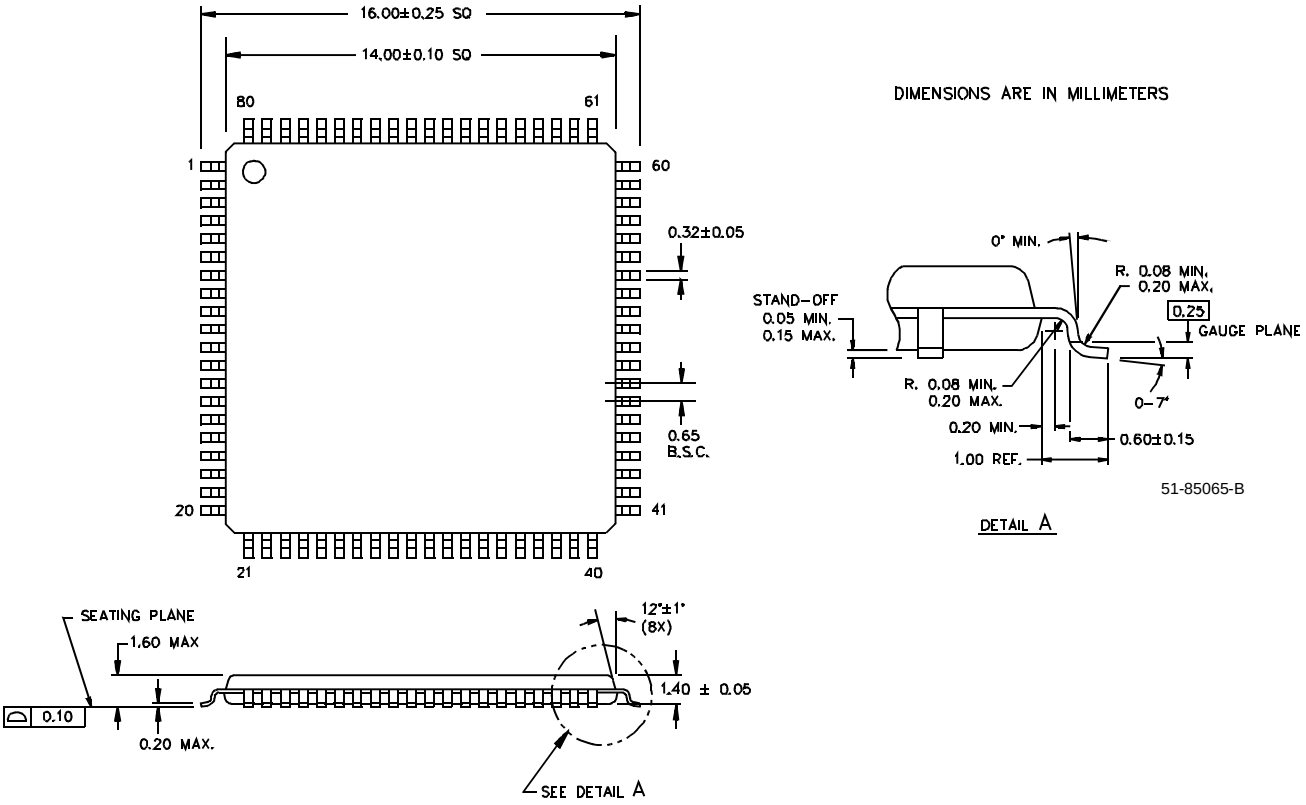
Package Diagrams

64-Lead Thin Plastic Quad Flat Pack (14 x 14 x 1.4 mm) A65



Package Diagrams (continued)

80-Pin Thin Plastic Quad Flat Pack A80



68-Lead Plastic Leaded Chip Carrier J81