



Nine Output, 3.3V SDRAM Buffer for 2 DIMMs or 4 SO-DIMMs

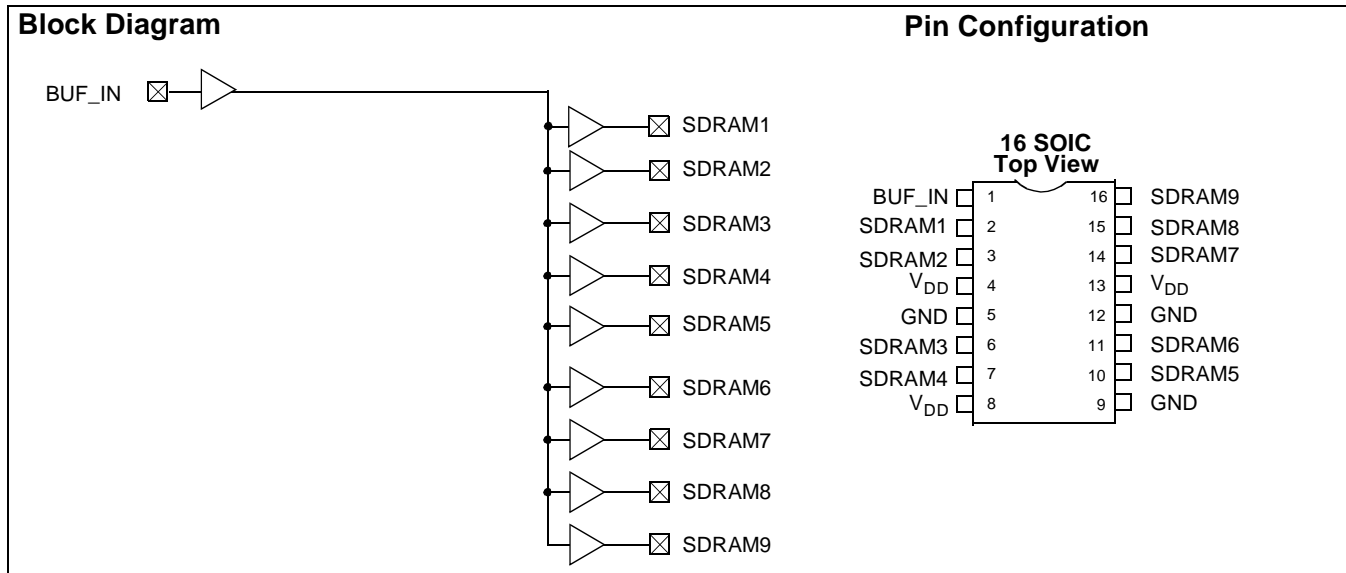
Features

- One input to nine output buffer/driver
- Supports two SDRAM DIMMs or four SO-DIMMs with one additional output for feedback to an external or chipset PLL
- Low power consumption for mobile applications
 - Less than 25 mA at 66.6 MHz with unloaded outputs
- 8.7-ns Input-Output delay
- Buffers all frequencies from DC to 100 MHz
- Output-output skew less than 250 ps
- Multiple V_{DD} and V_{SS} pins for noise and EMI reduction
- Space-saving 16-pin 150-mil SOIC package
- 3.3V operation

Functional Description

The CY2309NZ is a low-cost SDRAM buffer designed to distribute high-speed clocks in mobile PC systems and desktop PC systems with SDRAM support. The part has nine outputs, eight of which can be used to drive 2 DIMMs or 4 SO-DIMMs, and the remaining can be used for external feedback to a PLL. The device operates at 3.3V and outputs can run up to 100 MHz, making it compatible with Pentium II® processors and 100-MHz chipsets. The CY2309NZ can be used in conjunction with the CY2281, CY2282, CY2283, CY2284 or similar clock synthesizers for a full Pentium II motherboard solution.

The CY2309NZ is designed for low EMI and power optimization. It has multiple V_{SS} and V_{DD} pins for noise optimization and consumes less than 25 mA at 66.6 MHz, making it ideal for the low power requirements of mobile systems. It is available in an ultra-compact 150-mil 16-pin SOIC package.



Pin Description for CY2309NZ

Signal	Pin	Description
V_{DD}	4, 8, 13	3.3V Digital Voltage Supply
GND	5, 9, 12	Ground
BUF_IN	1	Input Clock
SDRAM [1:9]	2, 3, 6, 7, 10, 11, 14, 15, 16	SDRAM Clock Outputs

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Maximum Ratings

Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Input Voltage (Except REF) -0.5V to $V_{DD} + 0.5V$
 DC Input Voltage REF -0.5V to 7V

Storage Temperature -65°C to +150°C
 Max. Soldering Temperature (10 sec.) 260°C
 Junction Temperature 150°C
 Static Discharge Voltage
 (per MIL-STD-883, Method 3015) >2,000V

Operating Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance		30	pF
C_{IN}	Input Capacitance		7	pF
BUF_IN, SDRAM [1:9]	Operating Frequency	DC	100	MHz

Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage ^[1]			0.8	V
V_{IH}	Input HIGH Voltage ^[1]		2.0		V
I_{IL}	Input LOW Current	$V_{IN} = 0V$		50.0	μA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$		100.0	μA
V_{OL}	Output LOW Voltage ^[2]	$I_{OL} = 8\text{ mA}$		0.4	V
V_{OH}	Output HIGH Voltage ^[2]	$I_{OH} = -8\text{ mA}$	2.4		V
I_{DD}	Supply Current	Unloaded outputs at 66.66 MHz, SEL inputs at V_{DD} or GND		35	mA

Switching Characteristics ^[3] Over the Operating Range

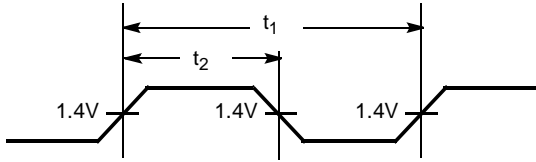
Parameter	Name	Description	Min.	Typ.	Max.	Unit
	Duty Cycle ^[2] = $t_2 \div t_1$	Measured at 1.4V	40.0	50.0	60.0	%
t_3	Rise Time ^[2]	Measured between 0.8V and 2.0V			1.50	ns
t_4	Fall Time ^[2]	Measured between 0.8V and 2.0V			1.50	ns
t_5	Output to Output Skew ^[2]	All outputs equally loaded			250	ps
t_6	Propagation Delay, BUF_IN Rising Edge to SDRAM Rising Edge ^[2]	Measured at $V_{DD}/2$	1	5	8.7	ns

Notes:

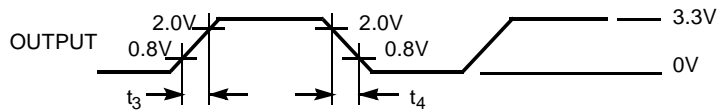
1. BUF_IN input has a threshold voltage of $V_{DD}/2$.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.
3. All parameters specified with loaded outputs.

Switching Waveforms

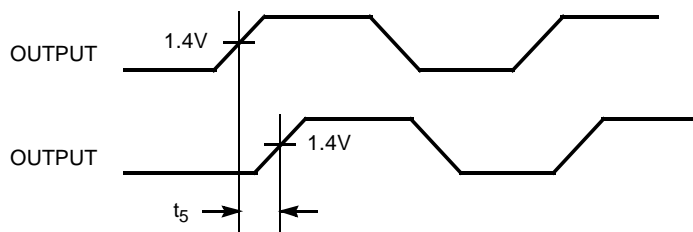
Duty Cycle Timing



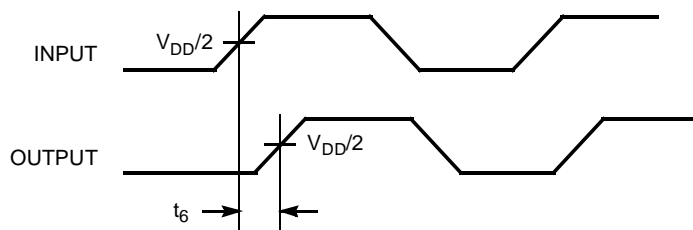
All Outputs Rise/Fall Time

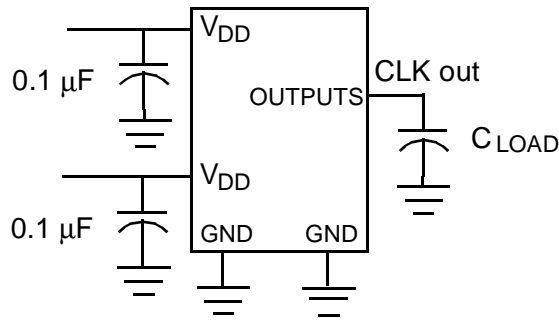


Output-Output Skew



Input-Output Propagation Delay



Test Circuits

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2309NZSC-1H	S16	16-pin 150-mil SOIC	Commercial

Document #: 38-00709-C

Package Diagram
16-Lead (150-Mil) Molded SOIC S16
