

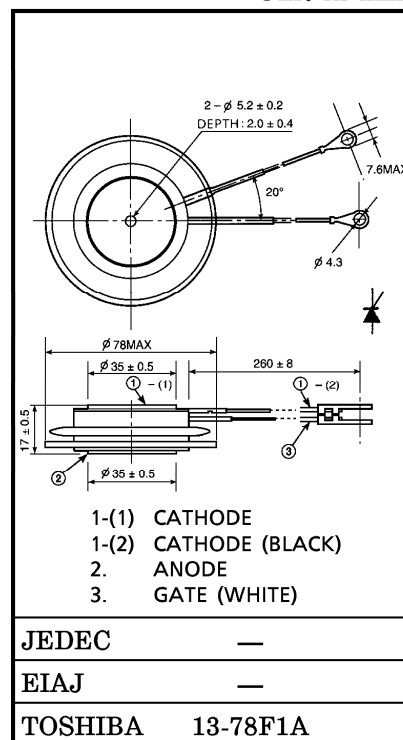
TOSHIBA ALLOY-FREE THYRISTOR

SF800U33

HIGH POWER CONTROL APPLICATIONS

- Repetitive Peak Off-State Voltage : V_{DRM}
- Repetitive Peak Reverse Voltage : V_{RRM}
- Average On-State Current : $I_T(AV) = 800A$
- Critical Rate of Rise of On-State Current : $di / dt = 200A / \mu s$
- Critical Rate of Rise of Off-State Voltage : $dv / dt = 500V / \mu s$
- Flat Package

Unit in mm



Weight : 250g

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MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage and Repetitive Peak Reverse Voltage	V_{DRM} V_{RRM}	1600	V
Non-Repetitive Peak Reverse Voltage (Non-Repetitive < 5ms, $T_j = 0 \sim 125^\circ\text{C}$)	V_{RSM}	1700	V
R.M.S On-State Current	$I_T(\text{RMS})$	1260	A
Average On-State Current	$I_T(\text{AV})$	800	A
Peak One Cycle Surge On-State Current (Non-Repetitive)	I_{TSM}	12000 (50Hz) 13200 (60Hz)	A
I^2t Limit Value	I^2t	7.2×10^5	A^2s
Critical Rate of Rise of On-State Current (Note)	di/dt	200	$\text{A} / \mu\text{s}$
Peak Gate Power Dissipation	P_{GM}	20	W
Average Gate Power Dissipation	$P_G(\text{AV})$	4	W
Peak Forward Gate Current	I_{GM}	4	A
Peak Forward Gate Voltage	V_{FGM}	20	V
Peak Reverse Gate Voltage	V_{RGM}	5	V
Junction Temperature	T_j	$-40 \sim 125$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	$-40 \sim 125$	$^\circ\text{C}$
Mounting Force	—	14.7 ± 1.5	kN

Note : $V_D = 800\text{V}$, $f = 50\text{Hz}$, $T_j = 120^\circ\text{C}$, Gate Supply ($V_G = 15\text{V}$, $R_G = 8\Omega$, $t_r \leq 1\mu\text{s}$)

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Repetitive Peak Off-State Current and Repetitive Peak Reverse Current	I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM} = 1600V$ $T_j = 125^\circ C$	—	35	mA
Peak On-State Voltage	V_{TM}	$I_{TM} = 2500A, T_j = 25^\circ C$	—	1.95	V
Gate Trigger Voltage	V_{GT}	$V_D = 6V, R_L = 6\Omega$	$T_j = -40^\circ C$	—	5.0
			$T_j = 25^\circ C$	—	4.0
Gate Trigger Current	I_{GT}		$T_j = -40^\circ C$	—	460
			$T_j = 25^\circ C$	—	320
Gate Non-Trigger Voltage	V_{GD}	$V_D = 800V, T_j = 125^\circ C$	0.2	—	V
Gate Non-Trigger Current	I_{GD}		5	—	mA
Delay Time	t_d	$V_D = 800V, T_j = 25^\circ C$ Gate Supply ($V_G = 15V, R_G = 8\Omega, t_r \leq 1\mu s$)	—	4	μs
Gate Turn-On Time	t_{gt}		—	6	μs
Holding Current	I_H	$T_j = 25^\circ C, R_L = 6\Omega$	—	300	mA
Critical Rate of Rise of Off-State Voltage	dv/dt	$V_{DRM} = 1100V, T_j = 125^\circ C$ Gate Open, Exponential Rise	500	—	V/ μs
Thermal Resistance (Junction to Case)	$R_{th(j-f)}$	DC	—	0.04	$^\circ C/W$

