Supertex inc.

HT01

T-52-11

8-Channel Logic To High-Voltage Level Translator

Ordering Information

Part Number/Package				
20 Lead CERDIP	20 Lead Plastic DIP	20 Terminal Ceramic LCC	Plastic SOW-20*	Die in waffle pack
HT0130D	HT0130P	HT0130LC	HT0130WG	HT0130X

*Same as SO-20 0.300 mil wide body.

Features

- ☐ Operating voltage up to 300V
- ☐ 5V to 15V logic input capability
- ☐ Output swings below GND if required
- ☐ Drives high-voltage P-Channel MOS from logic level signal
- ☐ Surface mount packaging available
- ☐ No "floating logic" required
- ☐ 8 independent channels

Applications

- ☐ ATE systems
- ☐ Printers/plotters
- ☐ P-Channel MOSFET control

Absolute Maximum Ratings[1,2]

Supply voltage, V_{DD}		V_{NN} - 0.3V to +16V
Supply Voltage, V_{PP}		V_{NN} - 0.3V to + 300V
Supply Voltage, V_{NN}		-16V to 0.3V
Logic inputs levels	V_{IN}	V_{NN} - 0.3V to V_{DD} + 0.3V
	V_{OUTPUT}	V_{PP} + 0.3V max
I_{OUT} — DC per Channel		30mA
Continuous total power dissipation[2]		700mW
Operating temperature range		0°C to 70°C
Storage temperature range		-65°C to + 150°C

Note 1: All voltages are referenced to chip ground.

Note 2: For operation above 25°C ambient derate lineraly to 85°C at 8mW/°C.

General Description

The Supertex HT01 8-channel Level Translator is designed to implement the necessary level translation between logic level signals and voltage swings required to drive high-voltage P-Channel MOSFET transistors. This device is intended to provide gate drive signals to devices such as the Supertex AP01 P-Channel MOSFET Array in applications requiring active pull-up to a high-voltage (V_{PP}) line of up to 300 volts. Logic input can be from 5 volts to 15 volts and is referenced to the logic supply (V_{DD}).

When an input is switched to 4.2 volts below the V_{DD} supply, the corresponding output will typically switch from V_{PP} to V_{PP} -14 volts. If the V_{PP} supply remains above 12 volts, the negative supply (V_{NN}) would be connected to system ground (GND). If variations of the V_{PP} supply level require the P-Channel MOSFET gate drive to swing below GND in order to turn on, connect the V_{NN} pin to a negative supply of up to -15 volts. The logic inputs can remain between V_{DD} and system ground (GND) and still provide correct operation.

In an OFF condition, the HT01 is a low power device. In an ON condition, each channel will dissipate power determined by the V_{PP} and V_{NN}voltage. Internal power dissipation must be considered when the application requires that more than one channel be active at one time, especially at higher V_{PP} voltage values.

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Electrical Characteristics (over recommended operating conditions unless noted)

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DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current			0.001	mA	All OFF
			0.6	3.50	mA	1 ch ON, no load
I_{PP}	V_{PP} Supply Current			0.001	mA	All OFF
			0.4	1.0	mA	1 ch ON, no load
I_{NN}	V_{NN} Supply Current			0.001	mA	All OFF
			1.0	4.50	mA	1 ch ON, no load
I_{SOURCE}	Output current	135	200		µA	Capacitive load
I_{SINK}	Output current	66	100		µA	Capacitive load
V_{ON}	Output voltage	V_{PP} - 17		V_{PP} - 10	V	V_{DD} = 4.75V
		V_{PP} - 17		V_{PP} - 12.5	V	V_{DD} = 15V
V_{OFF}	Output voltage	V_{PP} - 0.5			V	
V_Z	Zener voltage	11	14	17	V	Output to V_{PP}

AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{ON}	Turn on time, any channel		5		µs	V_{DD} = 10V, V_{NN} = GND
Δt_{ON}	Variation in t_{ON}, any 2 channels		5		%	V_{DD} = 10V, V_{NN} = GND
t_{OFF}	Turn off time, any channel		3		µs	V_{DD} = 10V, V_{NN} = GND
Δt_{OFF}	Variation in t_{OFF}, any 2 channels		5		%	V_{DD} = 10V, V_{NN} = GND

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	4.75		15	V
V_{PP}	Positive high voltage supply	V_{NN} + 12		275	V
V_{NN}	Negative supply	-15		0	V
V_{IH}	High-level input voltage	V_{DD} - 1.2		V_{DD}	V
V_{IL}	Low-level input voltage	0		V_{DD} - 4.2	V
T_A	Operating free-air temperature	0		+70	°C

Function Table

Input Condition	Output Stage
High level	V_{PP}
Low level	V_{PP} - V_Z

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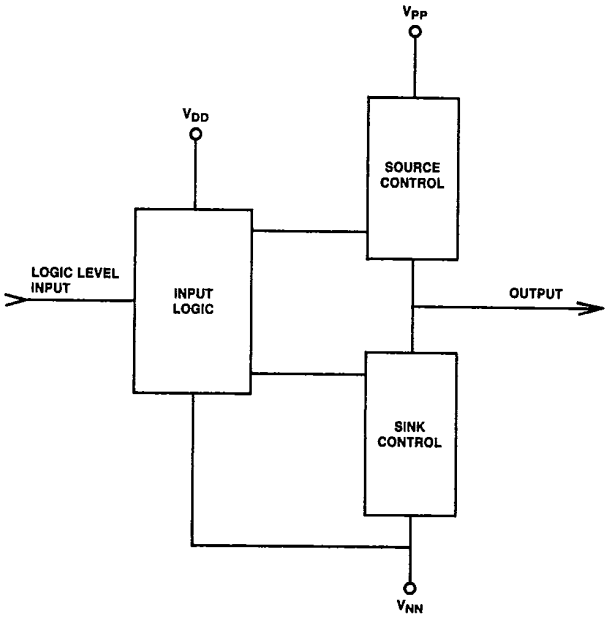
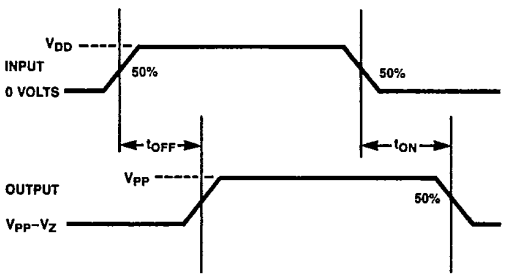
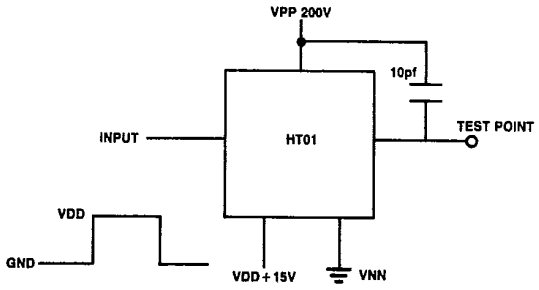
Functional Block Diagram



(One of eight channels within the HT01)

Switching Waveforms and Test Circuit





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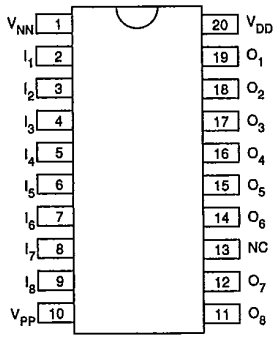
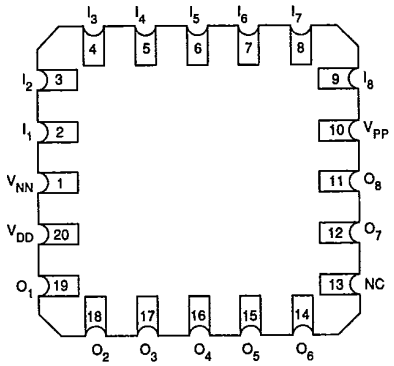
Pin Configuration



top view

20-pin DIP/SOW-20



bottom view

20-pin LCC