

# DATA SHEET



## **PCA9540** 2-channel I<sup>2</sup>C multiplexer

Product data  
Supersedes data of 2001 Feb 08

2002 May 13

## 2-channel I<sup>2</sup>C multiplexer

# PCA9540

### FEATURES

- 1-of-2 bi-directional translating multiplexer
- I<sup>2</sup>C interface logic; compatible with SMBus standards
- Channel selection via I<sup>2</sup>C bus
- Power up with all multiplexer channels deselected
- Low R<sub>dsON</sub> switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant Inputs
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 100 V MM per JESD22-A115 and 1000 V per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Package Offer: SO8, TSSOP8

### DESCRIPTION

The PCA9540 is a 1-of-2 bi-directional translating multiplexer, controlled via the I<sup>2</sup>C bus. The SCL/SDA upstream pair fans out to two SCx/SDx downstream pairs, or channels. Only one SCx/SDx channel is selected at a time, determined by the contents of the programmable control register.

A power-on reset function puts the registers in their default state and initializes the I<sup>2</sup>C state machine with no channels selected.

The pass gates of the multiplexer are constructed such that the V<sub>DD</sub> pin can be used to limit the maximum high voltage which will be passed by the PCA9540. This allows the use of different bus voltages on each SCx/SDx pair, so that 1.8 V, 2.5, or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors can pull the bus up to the desired voltage level for this channel. All I/O pins are 5 V tolerant.

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
8-Pin Plastic SO	-40 to +85 °C	PCA9540D	SOT96-1
8-Pin Plastic TSSOP	-40 to +85 °C	PCA9540DP	SOT505-1

Standard packing quantities and other packaging data is available at [www.philipslogic.com/packaging](http://www.philipslogic.com/packaging).

### PIN CONFIGURATION

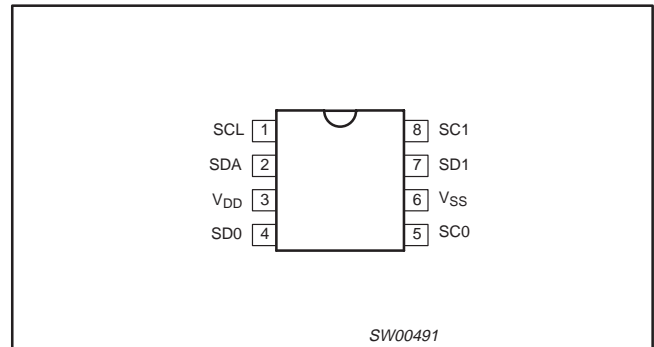


Figure 1. Pin configuration

### PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	SCL	Serial clock line
2	SDA	Serial data line
3	V <sub>DD</sub>	Supply voltage
4	SD0	Serial data 0
5	SC0	Serial clock 0
6	V <sub>SS</sub>	Supply ground
7	SD1	Serial data 1
8	SC1	Serial clock 1

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## BLOCK DIAGRAM

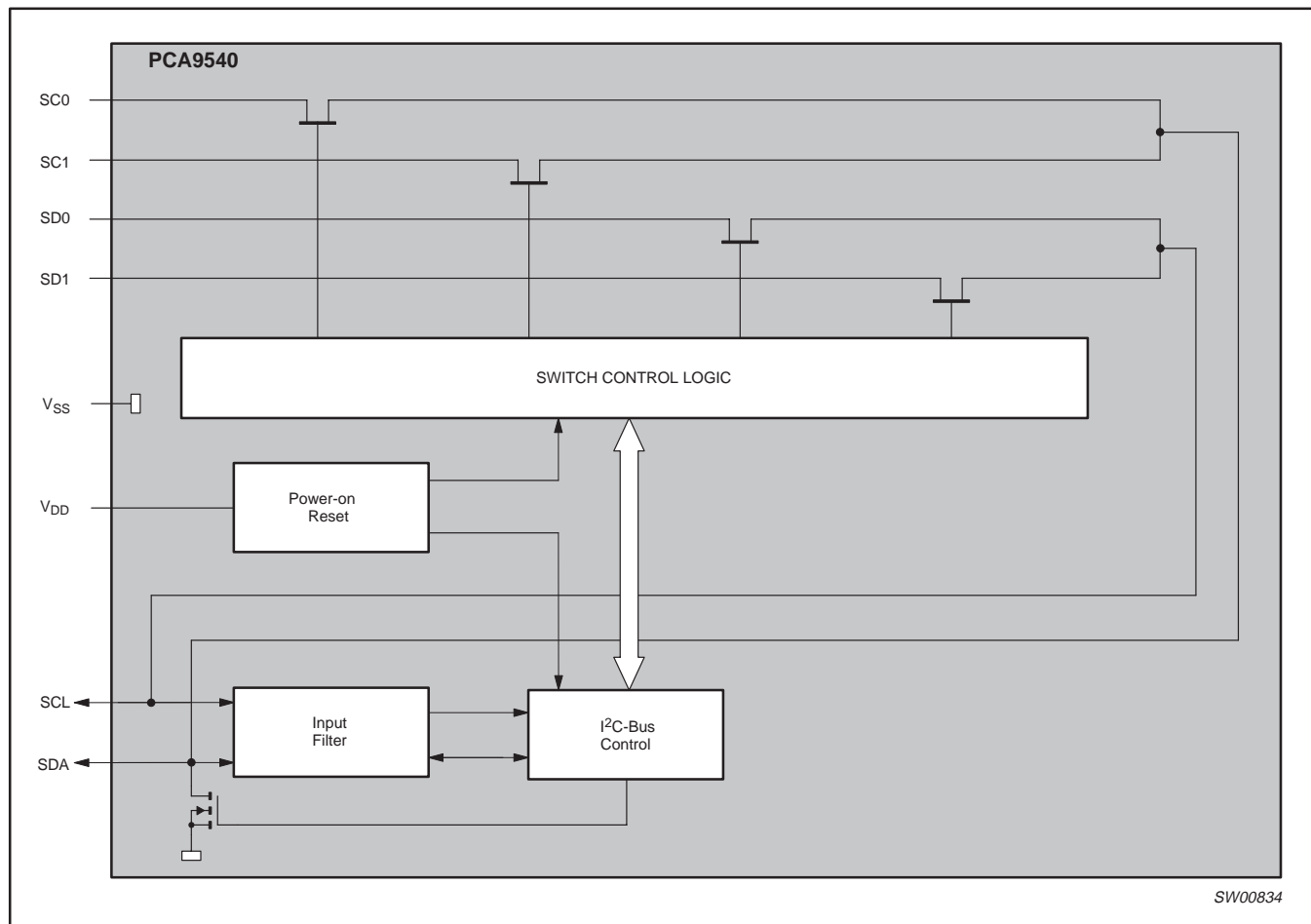


Figure 2. Block diagram

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## DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9540 is shown in Figure 3.

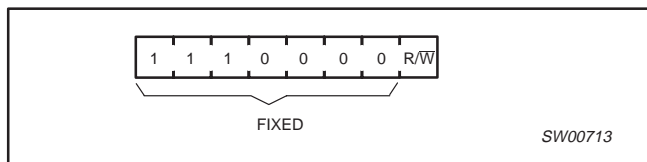


Figure 3. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1, a read is selected while a logic 0 selects a write operation.

## CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9540 which will be stored in the Control Register. If multiple bytes are received by the PCA9540, it will save the last byte received. This register can be written and read via the I<sup>2</sup>C bus.

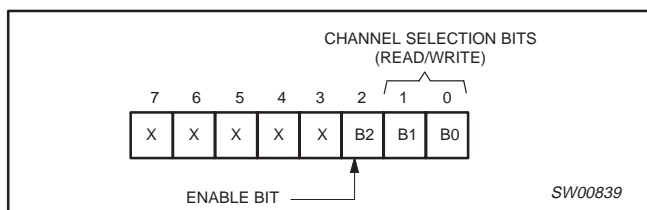


Figure 4. Control register

## CONTROL REGISTER DEFINITION

A SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9540 has been addressed. The 2 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a stop condition has been placed on the I<sup>2</sup>C bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 1. Control Register; Write — Channel Selection/Read — Channel Status

D7	D6	D5	D4	D3	B2	B1	B0	COMMAND
X	X	X	X	X	0	X	X	No channel selected
X	X	X	X	X	1	0	0	Channel 0 enabled
X	X	X	X	X	1	0	1	Channel 1 enabled
X	X	X	X	X	1	1	X	No channel selected

## POWER-ON RESET

When power is applied to V<sub>DD</sub>, an internal Power On Reset holds the PCA9540 in a reset state until V<sub>DD</sub> has reached V<sub>POR</sub>. At this point, the reset condition is released and the PCA9540 registers and I<sup>2</sup>C state machine are initialized to their default states, all zeroes causing all the channels to be deselected.

## VOLTAGE TRANSLATION

The pass gate transistors of the PCA9540 are constructed such that the V<sub>DD</sub> voltage can be used to limit the maximum voltage that will be passed from one I<sup>2</sup>C bus to another.

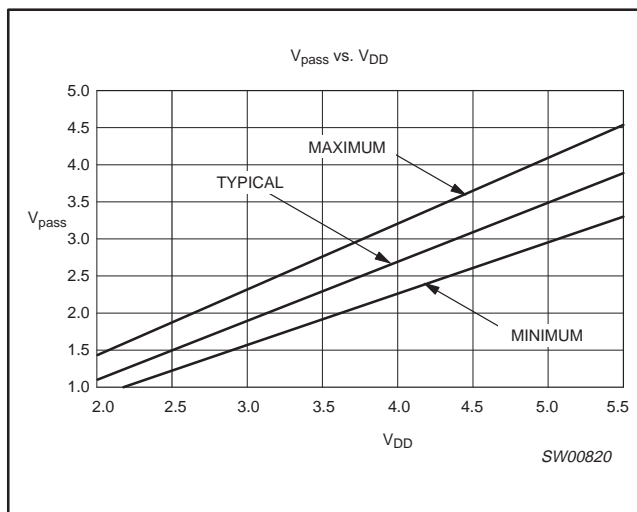


Figure 5. V<sub>pass</sub> voltage

Figure 5 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in the DC Characteristics section of this datasheet). In order for the PCA9540 to act as a voltage translator, the V<sub>pass</sub> voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then V<sub>pass</sub> should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Figure 5, we see that V<sub>pass</sub> (max.) will be at 2.7 V when the PCA9540 supply voltage is 3.5 V or lower so the PCA9540 supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 12).

More Information can be found in Application Note AN262 PCA954X family of I<sup>2</sup>C/SMBus multiplexers and switches.

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## CHARACTERISTICS OF THE I<sup>2</sup>C-BUS

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 6).

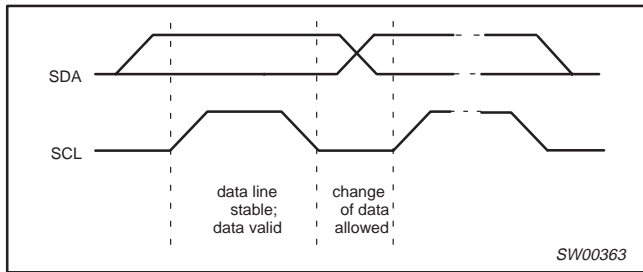


Figure 6. Bit transfer

## Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 7).

## System configuration

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 8).

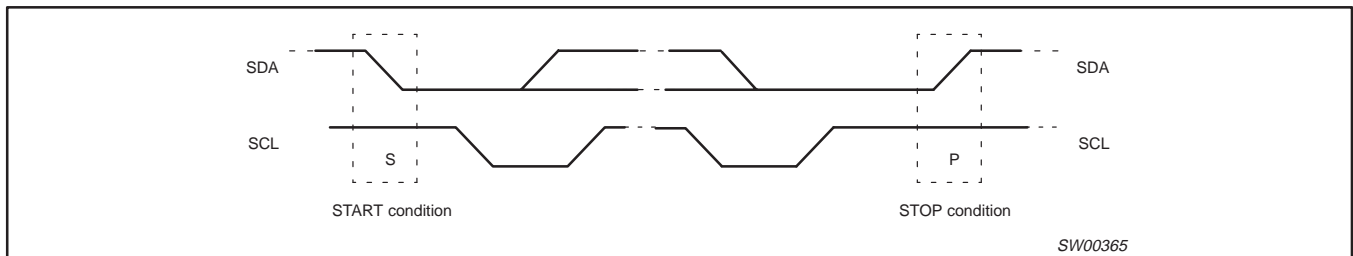


Figure 7. Definition of start and stop conditions

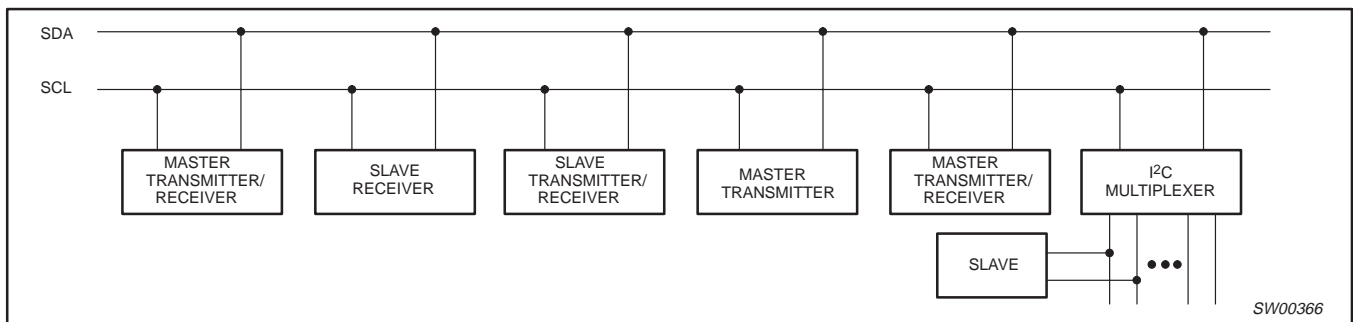


Figure 8. System configuration

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## Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

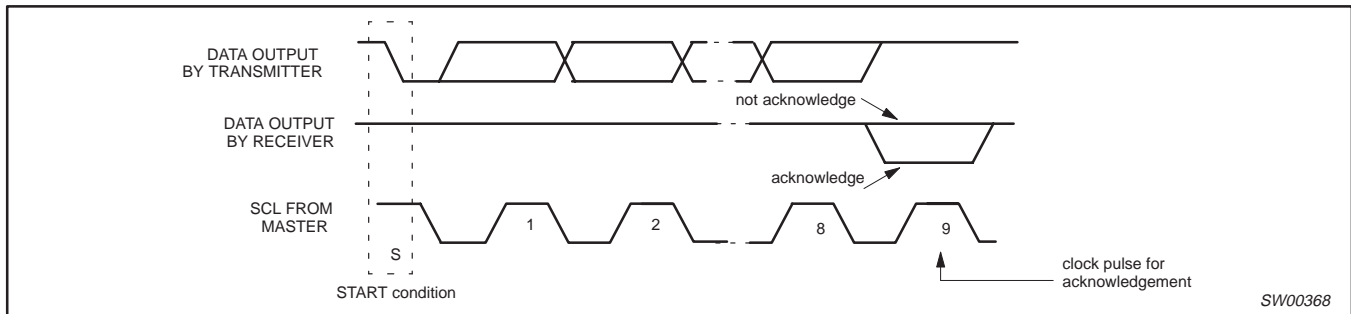


Figure 9. Acknowledgement on the I<sup>2</sup>C-bus

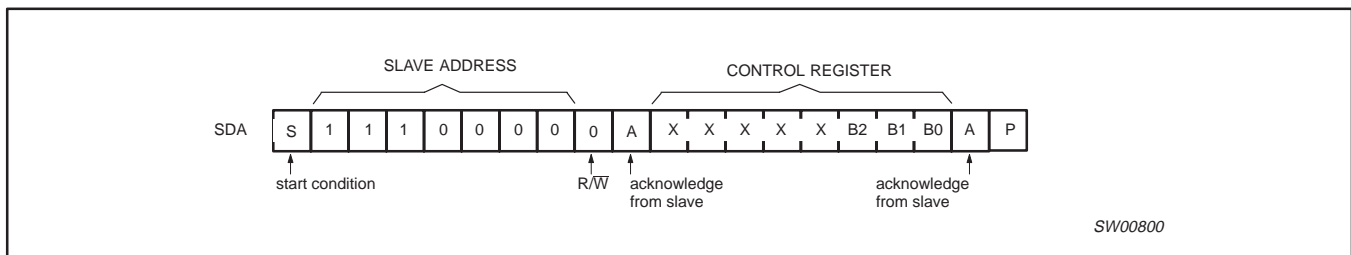


Figure 10. WRITE control register

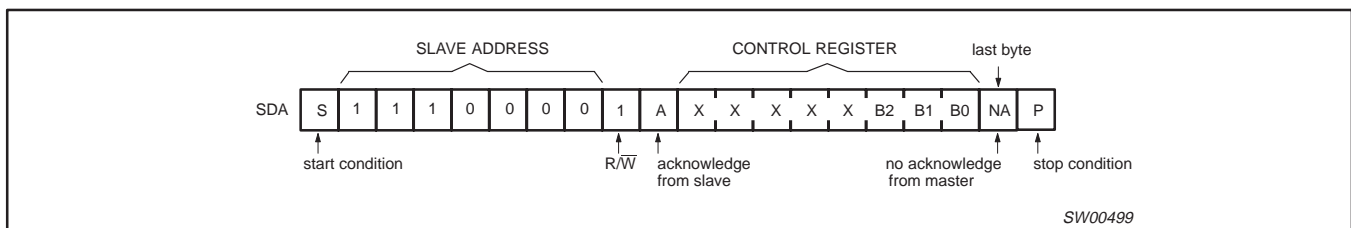


Figure 11. READ control register

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## TYPICAL APPLICATION

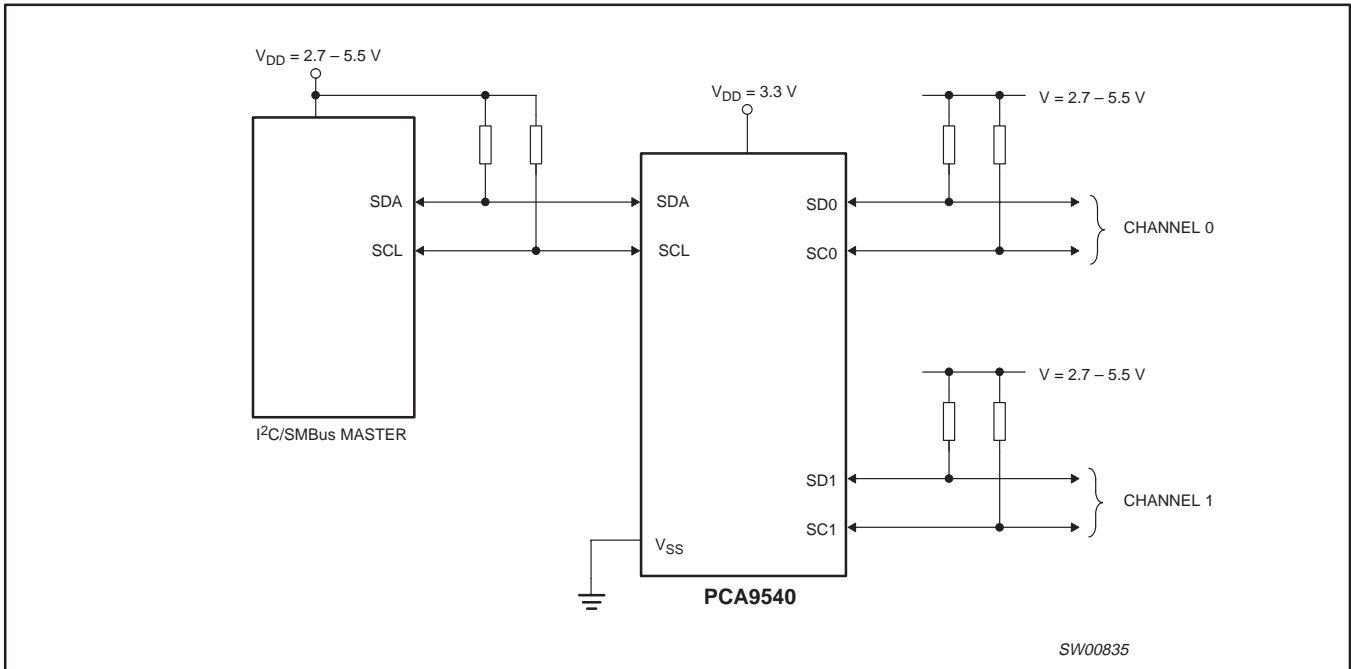


Figure 12. Typical application

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**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>DD</sub>	DC supply voltage		-0.5 to +7.0	V
V <sub>I</sub>	DC input voltage		-0.5 to +7.0	V
I <sub>I</sub>	DC input current		±20	mA
I <sub>O</sub>	DC output current		±25	mA
I <sub>DD</sub>	Supply current		±100	mA
I <sub>SS</sub>	Supply current		±100	mA
P <sub>tot</sub>	total power dissipation		400	mW
T <sub>stg</sub>	Storage temperature range		-60 to +150	°C
T <sub>amb</sub>	Operating ambient temperature		-40 to +85	°C

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

**DC CHARACTERISTICS**V<sub>DD</sub> = 2.3 to 3.6 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 to +85 °C; unless otherwise specified. (See page 9 for V<sub>DD</sub> = 3.6 to 5.5 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>Supply</b>						
V <sub>DD</sub>	Supply voltage		2.3	—	3.6	V
I <sub>DD</sub>	Supply current	Operating mode; V <sub>DD</sub> = 3.6 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 100 kHz	—	50	100	μA
I <sub>stb</sub>	Standby current	Standby mode; V <sub>DD</sub> = 3.6 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 0 kHz	—	20	100	μA
V <sub>POR</sub>	Power-on reset voltage	no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	1.6	2.1	V
<b>Input SCL; input/output SDA</b>						
V <sub>IL</sub>	LOW level input voltage		-0.5	—	0.3 V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH level input voltage		0.7 V <sub>DD</sub>	—	6	V
I <sub>OL</sub>	LOW level output current	V <sub>OL</sub> = 0.4 V	3	—	—	mA
		V <sub>OL</sub> = 0.6 V	6	—	—	mA
I <sub>L</sub>	Leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-1	—	+1	μA
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = V <sub>SS</sub>	—	7	8	pF
<b>Pass Gate</b>						
R <sub>ON</sub>	Switch resistance	V <sub>CC</sub> = 3.0 to 3.6 V, V <sub>O</sub> = 0.4 V, I <sub>O</sub> = 15 mA	5	20	31	Ω
		V <sub>CC</sub> = 2.3 to 2.7 V, V <sub>O</sub> = 0.4 V, I <sub>O</sub> = 10 mA	7	26	55	
V <sub>Pass</sub>	Switch output voltage	V <sub>swin</sub> = V <sub>DD</sub> = 3.3 V; I <sub>swout</sub> = -100 μA	—	2.2	—	V
		V <sub>swin</sub> = V <sub>DD</sub> = 3.0 to 3.6 V; I <sub>swout</sub> = -100 μA	1.6	—	2.8	
		V <sub>swin</sub> = V <sub>DD</sub> = 2.5 V; I <sub>swout</sub> = -100 μA	—	1.5	—	
		V <sub>swin</sub> = V <sub>DD</sub> = 2.3 to 2.7 V; I <sub>swout</sub> = -100 μA	1.1	—	2.0	
I <sub>L</sub>	Leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-1	—	+1	μA
C <sub>io</sub>	Input/output capacitance	V <sub>I</sub> = V <sub>SS</sub>	—	2.5	5	pF



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**DC CHARACTERISTICS** $V_{DD} = 3.6$  to  $5.5$  V;  $V_{SS} = 0$  V;  $T_{amb} = -40$  to  $+85$  °C; unless otherwise specified. (See page 8 for  $V_{DD} = 2.3$  to  $3.6$  V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>Supply</b>						
$V_{DD}$	Supply voltage		3.6	—	5.5	V
$I_{DD}$	Supply current	Operating mode; $V_{DD} = 5.5$ V; no load; $V_I = V_{DD}$ or $V_{SS}$ ; $f_{SCL} = 100$ kHz	—	580	700	$\mu$ A
$I_{stb}$	Standby current	Standby mode; $V_{DD} = 5.5$ V; no load; $V_I = V_{DD}$ or $V_{SS}$	—	100	200	$\mu$ A
$V_{POR}$	Power-on reset voltage	no load; $V_I = V_{DD}$ or $V_{SS}$	—	1.6	2.1	V
<b>Input SCL; input/output SDA</b>						
$V_{IL}$	LOW level input voltage		-0.5	—	$0.3 V_{DD}$	V
$V_{IH}$	HIGH level input voltage		$0.7 V_{DD}$	—	6	V
$I_{OL}$	LOW level output current	$V_{OL} = 0.4$ V	3	—	—	mA
		$V_{OL} = 0.6$ V	6	—	—	$\mu$ A
$I_{IL}$	LOW level input current	$V_I = V_{SS}$	-10	—	10	mA
$I_{IH}$	HIGH level input current	$V_I = V_{DD}$	—	—	500	$\mu$ A
$C_i$	Input capacitance	$V_I = V_{SS}$	—	6	8	pF
<b>Pass Gate</b>						
$R_{ON}$	Switch resistance	$V_{CC} = 4.5$ to $5.5$ V; $V_O = 0.4$ V; $I_O = 15$ mA	4	11	24	$\Omega$
$V_{Pass}$	Switch output voltage	$V_{swin} = V_{DD} = 5.0$ V; $I_{swout} = -100$ $\mu$ A	—	3.5	—	V
		$V_{swin} = V_{DD} = 4.5$ to $5.5$ V; $I_{swout} = -100$ $\mu$ A	2.6	—	4.5	V
$I_L$	Leakage current	$V_I = V_{DD}$ or $V_{SS}$	-1	—	+1	$\mu$ A
$C_{io}$	Input/output capacitance	$V_I = V_{SS}$	—	2.5	5	pF

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## AC CHARACTERISTICS

SYMBOL	PARAMETER	STANDARD-MODE I <sup>2</sup> C-BUS		FAST-MODE I <sup>2</sup> C-BUS		UNIT
		MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Propagation delay from SDA to SD <sub>n</sub> or SCL to SC <sub>n</sub>	—	0.3 <sup>1</sup>	—	0.3 <sup>1</sup>	ns
f <sub>SCL</sub>	SCL clock frequency	0	100	0	400	kHz
t <sub>BUF</sub>	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs
t <sub>HD;STA</sub>	Hold time (repeated) START condition After this period, the first clock pulse is generated	4.0	—	0.6	—	μs
t <sub>LOW</sub>	LOW period of the SCL clock	4.7	—	1.3	—	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock	4.0	—	0.6	—	μs
t <sub>SU;STA</sub>	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
t <sub>SU;STO</sub>	Set-up time for STOP condition	4.0	—	0.6	—	μs
t <sub>HD;DAT</sub>	Data hold time	0 <sup>2</sup>	3.45	0 <sup>2</sup>	0.9	μs
t <sub>SU;DAT</sub>	Data set-up time	250	—	100	—	ns
t <sub>R</sub>	Rise time of both SDA and SCL signals	—	1000	20 + 0.1C <sub>b</sub> <sup>3</sup>	300	ns
t <sub>F</sub>	Fall time of both SDA and SCL signals	—	300	20 + 0.1C <sub>b</sub> <sup>3</sup>	300	μs
C <sub>b</sub>	Capacitive load for each bus line	—	400	—	400	μs
t <sub>SP</sub>	Pulse width of spikes which must be suppressed by the input filter	—	50	—	50	ns
t <sub>VD;DATL</sub>	Data valid (HL)	—	1	—	1	μs
t <sub>VD;DATH</sub>	Data valid (LH)	—	0.6	—	0.6	μs
t <sub>VD;ACK</sub>	Data valid Acknowledge	—	1	—	1	μs

**NOTES:**

1. Pass gate propagation delay is calculated from the 20 Ω typical R<sub>ON</sub> and and the 15 pF load capacitance.
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IHmin</sub> of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
3. C<sub>b</sub> = total capacitance of one bus line in pF.

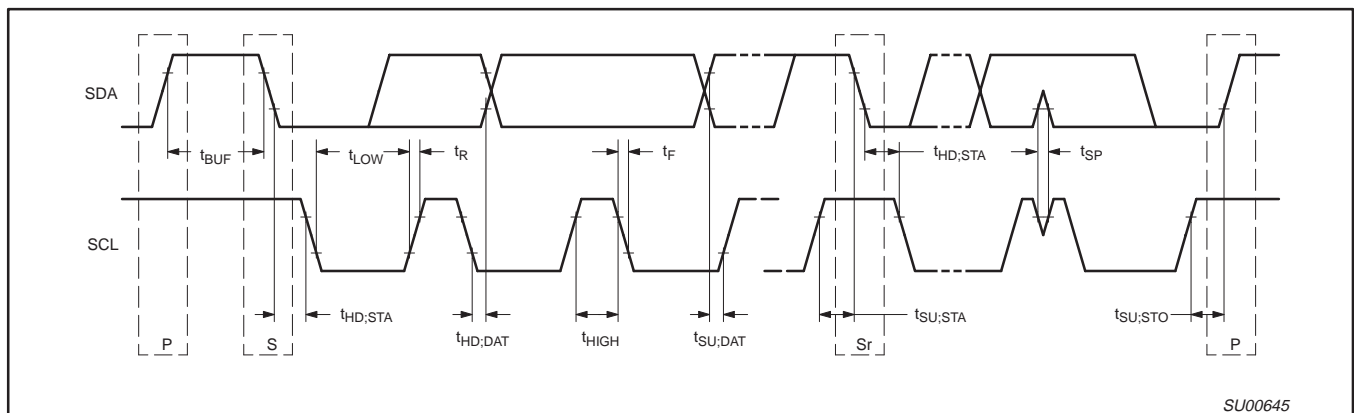


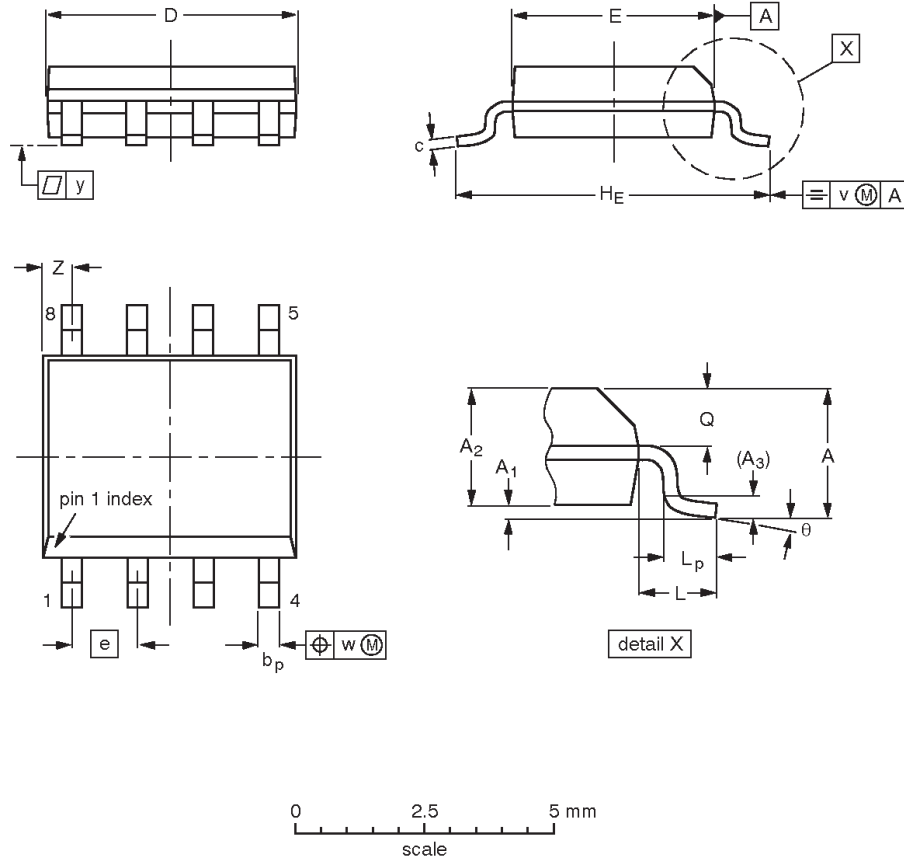
Figure 13. Definition of timing on the I<sup>2</sup>C-bus

# 2-channel I<sup>2</sup>C multiplexer

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**SO8:** plastic small outline package; 8 leads; body width 3.9 mm

**SOT96-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	HE	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

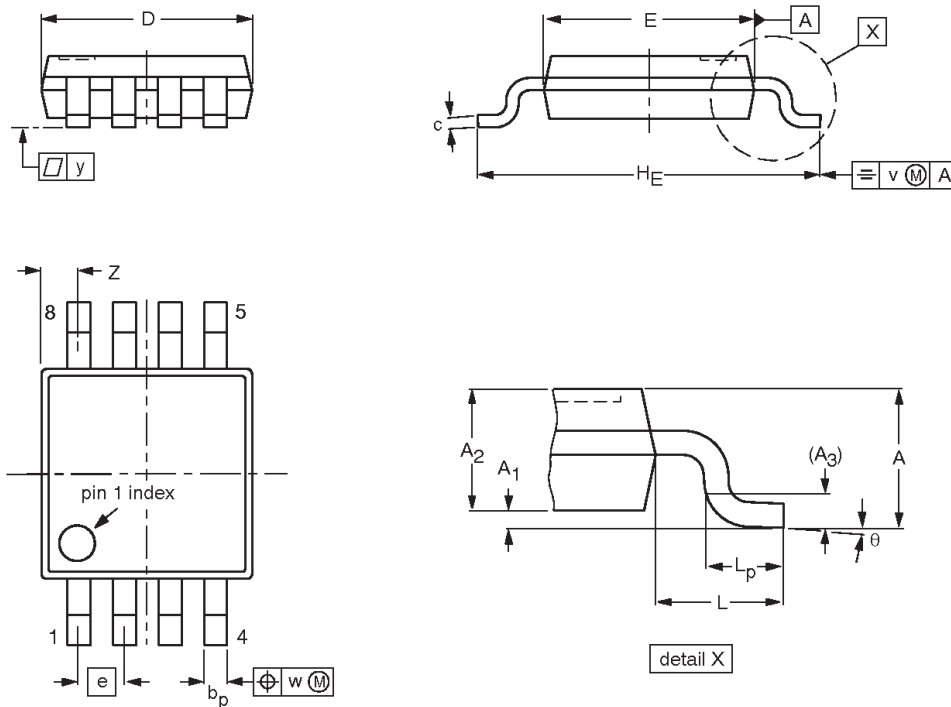
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				97-05-22 99-12-27

# 2-channel I<sup>2</sup>C multiplexer

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TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sub>max.</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.10 2.90	3.10 2.90	0.65	5.10 4.70	0.94	0.70 0.40	0.1	0.1	0.1	0.70 0.35	6° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT505-1						99-04-09

2-channel I<sup>2</sup>C multiplexer

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Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

## Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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