MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order Number: MPC991/D
Rev 0, 08/2001

Low Voltage PLL Clock Driver

MPC991

LOW VOLTAGE PLL CLOCK DRIVER

The MPC991 is a 3.3 V compatible, PLL based ECL/PECL clock driver. The fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC991 makes the device ideal for Workstation, Mainframe Computer and Telecommunication applications. The MPC991 offers a differential ECL/PECL input for applications which need to lock to an existing clock signal. It also offers a secondary single–ended ECL clock for system test capabilities.

- Fully Integrated PLL
- Output Frequency up to 400 MHz
- ECL/PECL Inputs and Outputs
- Operates from a 3.3 V Supply
- Output Frequency Configurable
- TQFP Packaging
- ±50 ps Cycle–to–Cycle Jitter

FA SUFFIX
52–LEAD TQFP PACKAGE
CASE 848D–03

The MPC991 offers three banks of outputs which can each be programmed via the the four fsel pins of the device. There are 16 different output frequency configurations available in the device. The configurations include output ratios of 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 4:3:1 and 4:3:2. The programming table in this data sheet illustrates the various programming options. The SYNC output monitors the relationship between the Qa and Qc output banks. The output pulses per the timing diagrams in this data sheet signal the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies (i.e., 3:2 or 4:3 relationships). The Sync_Sel input toggles the Qd outputs between sync signals and extensions to the Qc bank of outputs.

The MPC991 provides a separate output for the feedback to the PLL. This allows for the feedback frequency to be programmed independently of the other outputs allowing for unique input vs output frequency relationships. The fselFB inputs provide 6 different feedback frequencies from the QFB differential output pair.

The MPC991 features an external differential ECL/PECL feedback to the PLL. This external feedback feature allows the MPC991 to be used as a “zero” delay buffer. The propagation delay between the input reference and the output is dependent on the input reference frequency. The selection of higher reference frequencies will provide near zero delay through the device.

The PLL_En, Ref_Sel and the Test_Clk input pins provide a means of bypassing the PLL and driving the output buffers directly. This allows the user to single step a design during system debug. Note that the Test_Clk input is routed through the dividers so that depending on the programming several edges on the Test_Clk input will be needed to get corresponding edge transitions on the outputs. The VCO_Sel input provides a means of recentering the VCO to provide a broader range of VCO frequencies for stable PLL operation.

If the frequency select or the VCO_Sel pins are changed during operation, a master reset signal must be applied to ensure output synchronization and phase–lock. If the VCO is driven beyond its maximum frequency, the VCO can outrun the internal dividers when the VCO_Sel pin is low. This will also prevent the PLL from achieving lock. Again, a master reset signal will need to be applied to allow for phase–lock. The device employs a power–on reset circuit which will ensure output synchronization and PLL lock on initial power–up.

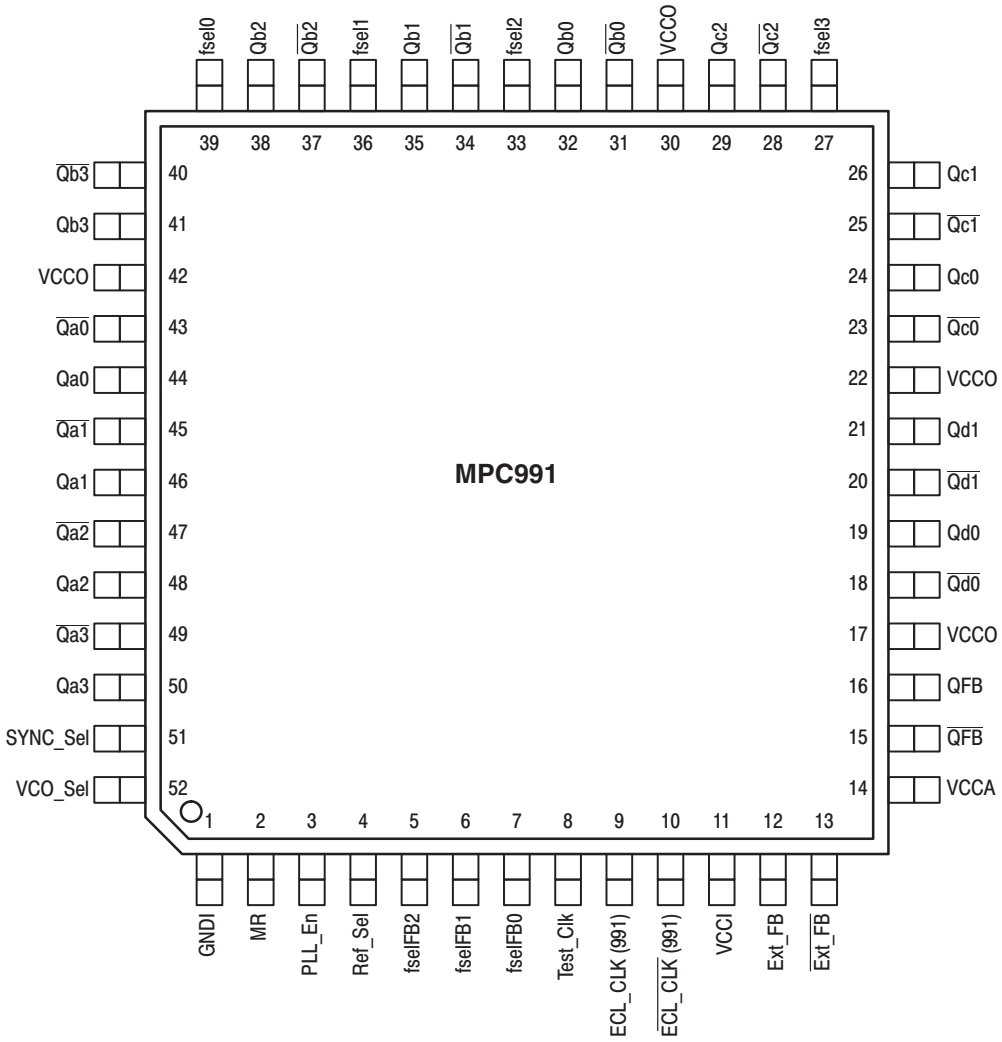


Figure 1. 52–Lead Pinout (Top View)

FUNCTION TABLE 1

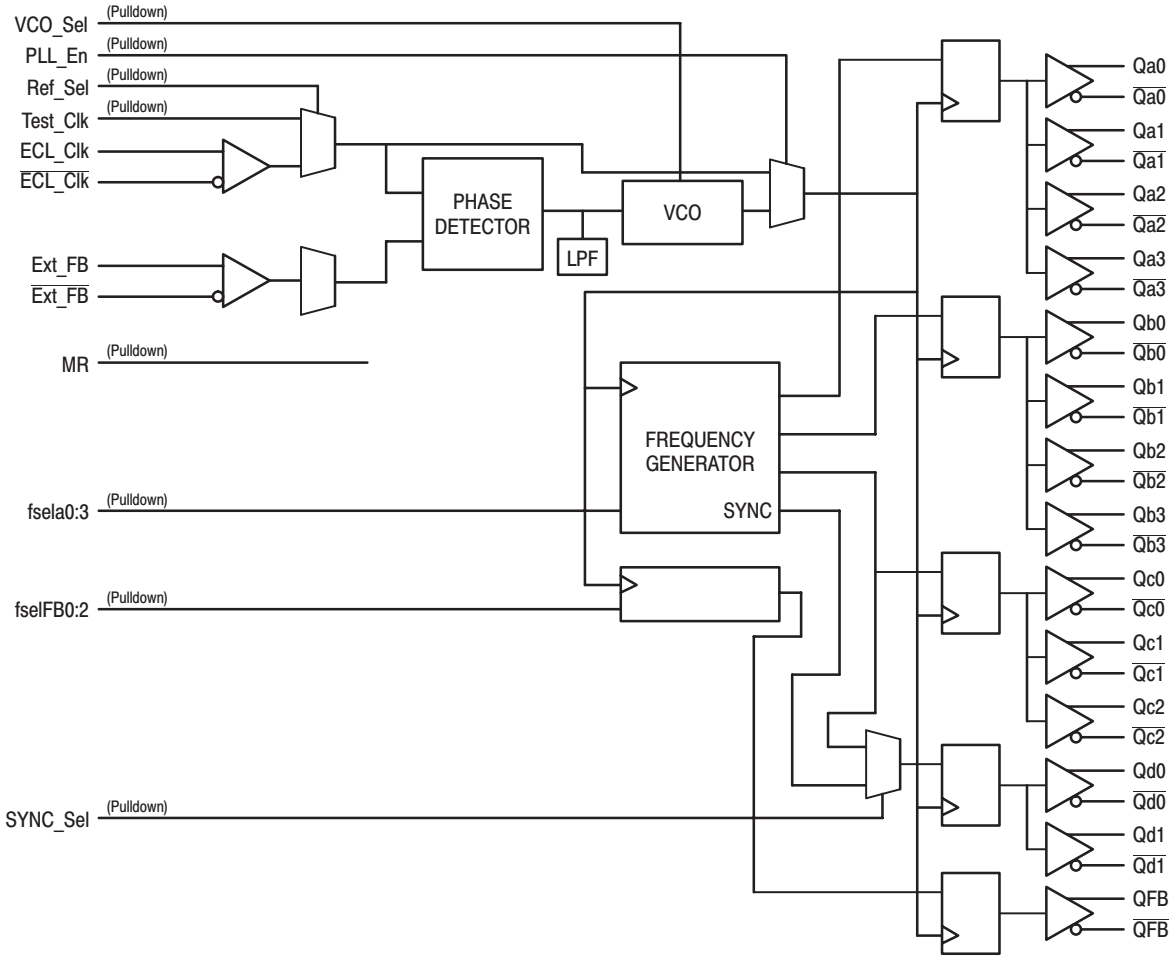
INPUTS				OUTPUTS		
fsel3	**fsel2**	**fsel1**	**fsel0**	**Qa**	**Qb**	**Qc**
0	0	0	0	÷2	÷2	÷2
0	0	0	1	÷2	÷2	÷4
0	0	1	0	÷2	÷4	÷4
0	0	1	1	÷2	÷2	÷6
0	1	0	0	÷2	÷6	÷6
0	1	0	1	÷2	÷4	÷6
0	1	1	0	÷2	÷4	÷8
0	1	1	1	÷2	÷6	÷8
1	0	0	0	÷2	÷2	÷8
1	0	0	1	÷2	÷8	÷8
1	0	1	0	÷4	÷4	÷6
1	0	1	1	÷4	÷6	÷6
1	1	0	0	÷4	÷6	÷8
1	1	0	1	÷6	÷6	÷8
1	1	1	0	÷6	÷8	÷8
1	1	1	1	÷8	÷8	÷8

FUNCTION TABLE 2

fselFB2	fselFB1	fselFB0	QFB
0	0	0	÷2
0	0	1	÷4
0	1	0	÷6
0	1	1	÷8
1	0	0	÷8
1	0	1	÷16
1	1	0	÷24
1	1	1	÷32

FUNCTION TABLE 3

Control Pin	Logic '0'	Logic '1'
PLL_En	Enable PLL	Bypass PLL
VCO_Sel	fVCO	fVCO/2
Ref_Sel	ECL/PECL	Test_Clk
MR	—	Reset Outputs
SYNC_Sel	SYNC Outputs	Match Qc Outputs



NOTE: ECL_Clk, Ext_FB have internal pulldowns, while $\overline{\text{ECL\_Clk}}$, $\overline{\text{Ext\_FB}}$ have external pullups to ensure stability under open input conditions.

Figure 2. MPC991 Logic Diagram

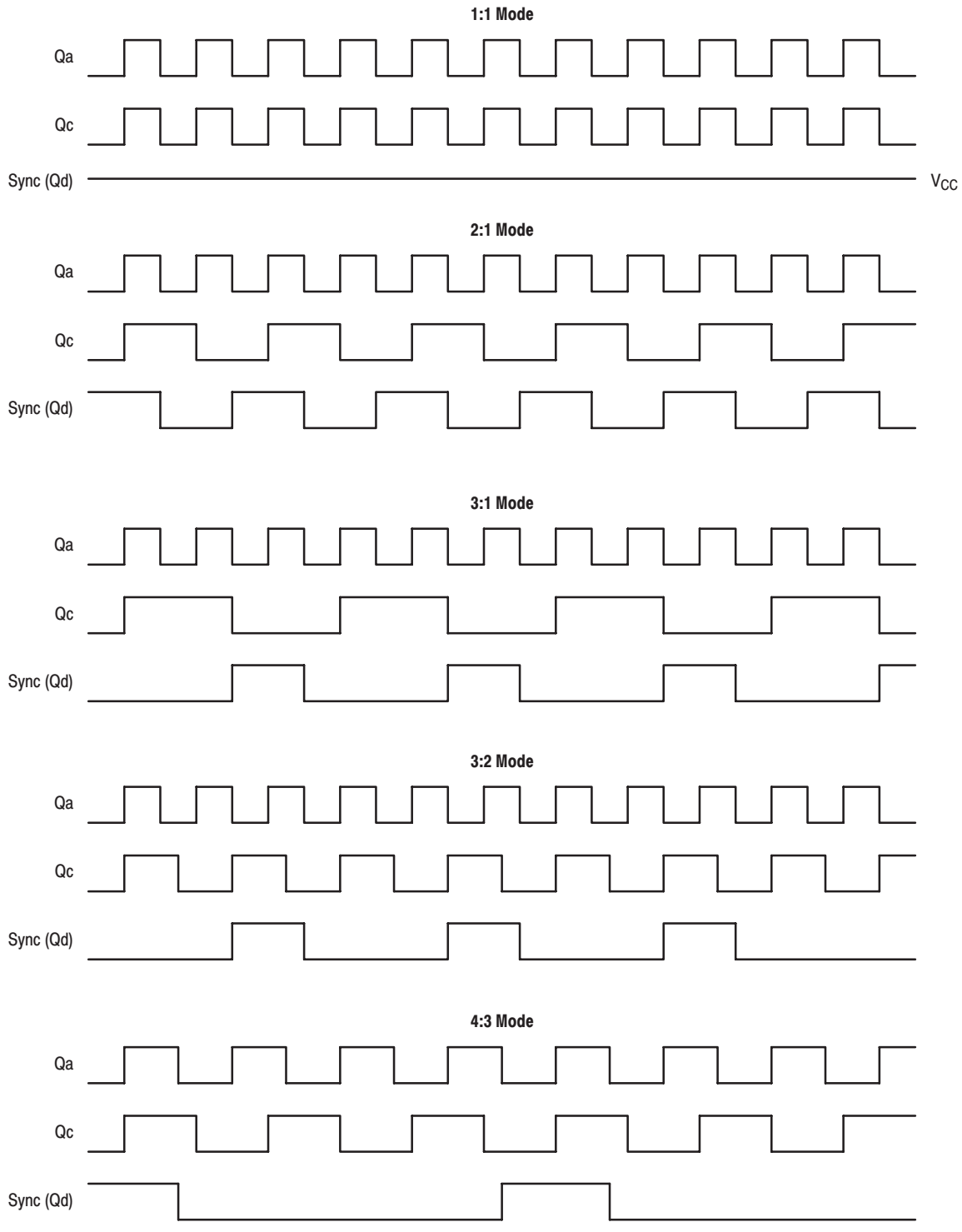


Figure 3. Timing Diagrams

ECL DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCA} = V_{CCI} = V_{CCO} = 0 V, GNDI = –3.3 V ±5%, Note 1.)

Symbol	Characteristic	0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.3		–0.7	–1.3	–1.0	–0.7	–1.3		–0.7	V
V_{OL}	Output LOW Voltage	–2.0		–1.4	–2.0	–1.7	–1.4	–2.0		–1.4	V
V_{IH}	Input HIGH Voltage	–1.1		–0.9	–1.1		–0.9	–1.1		–0.9	V
V_{IL}	Input LOW Voltage	–1.8		–1.5	–1.8		–1.5	–1.8		–1.5	V
V_{PP}	Minimum Input Swing	500			500			500			mV
V_{CMR}	Common Mode Range	V_{CC} –1.3V		V_{CC} –0.5V	V_{CC} –1.3V		V_{CC} –0.5V	V_{CC} –1.3V		V_{CC} –0.5V	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{GNDI}	Power Supply Current		200	240		200	240		200	240	mA

1. Refer to Motorola Application Note AN1545/D "*Thermal Data for MPC Clock Drivers*" for thermal management guidelines.

PECL DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCA} = V_{CCI} = V_{CCO} = 3.3 V ±5%, GNDI = 0 V, Note 2.)

Symbol	Characteristic	0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (Note 3.)	2.0		2.6	2.0	2.3	2.6	2.3		2.6	V
V_{OL}	Output LOW Voltage (Note 3.)	1.3		1.9	1.3	1.6	1.9	1.3		1.9	V
V_{IH}	Input HIGH Voltage (Note 3.)	2.2		2.4	2.2		2.4	2.2		2.4	V
V_{IL}	Input LOW Voltage (Note 3.)	1.5		1.8	1.5		1.8	1.5		1.8	V
V_{PP}	Minimum Input Swing	500			500			500			mV
V_{CMR}	Common Mode Range	V_{CC} –1.3V		V_{CC} –0.5V	V_{CC} –1.3V		V_{CC} –0.5V	V_{CC} –1.3V		V_{CC} –0.5V	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{GNDI}	Power Supply Current		200	240		200	240		200	240	mA

2. Refer to Motorola Application Note AN1545/D "*Thermal Data for MPC Clock Drivers*" for thermal management guidelines.
3. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CCA} = V_{CCI} = V_{CCO} = 3.3 V ±5%, Termination of 50 Ω to V_{CC} – 2.0 V)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time		0.2		1.0	ns	20% to 80%
t_{pw}	Output Duty Cycle		47.5	50	52.5	%	
t_{os}	Output-to-Output Skew	Same Frequency Different Frequencies		150 250	250 350	ps	
f_{VCO}	PLL VCO Lock Range	VCO_Sel = '0' VCO_Sel = '1'	400 200		800 400	MHz	FB ÷8 to ÷32 (Note 4.) FB ÷4 to ÷32
t_{pd}	Ref to Feedback Offset		75	250	425	ps	f_{ref} = 50MHz (Note 5.)
f_{max}	Maximum Output Frequency	Qa,Qb,Qc (÷2) Qa,Qb,Qc (÷4) Qa,Qb,Qc (÷6) Qa,Qb,Qc (÷8)			400 200 133 100	MHz	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)			±50		ps	
t_{lock}	Maximum PLL Lock Time				10	ms	

4. With VCO_Sel = '0', the PLL will be unstable with a ÷2, ÷4 and some ÷6 feedback configurations. With V_{CO_Sel} = '1', the PLL will be unstable with a ÷2 feedback ratio.
5. t_{pd} is specified for 50MHz input reference FB ÷ 8. The window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic		Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls			3.0	ns	
f_{ref}	Reference Input Frequency	Feedback divide 6	100	125	MHz	
	VCO_SEL='0'	Feedback divide 8	50	100		
		Feedback divide 16	25	50		
		Feedback divide 24	16.67	33.33		
		Feedback divide 32	12.5	25		
	VCO_SEL='1'	Feedback divide 4	50	100		
		Feedback divide 6	33.3	66.67		
		Feedback divide 8	25	50		
		Feedback divide 16	12.5	25		
		Feedback divide 24	8.33	16.67		
		Feedback divide 32	6.25	12.5		
f_{refDC}	Reference Input Duty Cycle		25	75	%	

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC991 provides a separate power supply for the internal PLL of the device. The purpose of this design technique is to allow the user to filter externally generated system noise from the internal, relatively sensitive analog PLL.

Figure 4 illustrates a suggested power supply filter using an LC filter network. The inductor value should be choosen to maximize the AC filter impedance while maintaining a low DC resistance. An inductor with a maximum DC series resistance of 5 Ω should be used. The parallel capacitor combination on the V_{CCA} pin ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

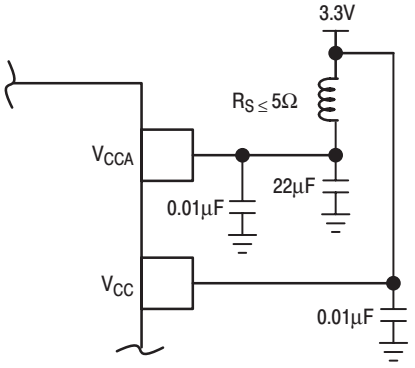
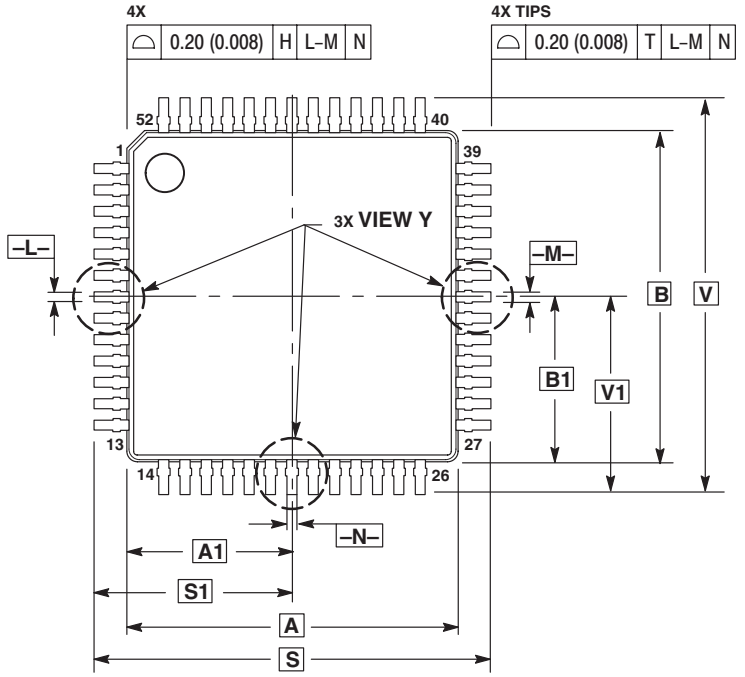
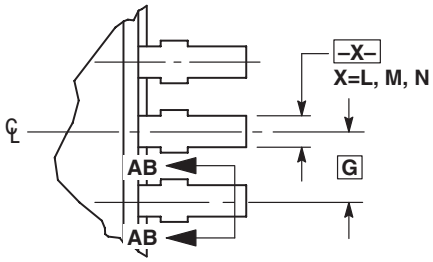


Figure 4. Power Supply Filter

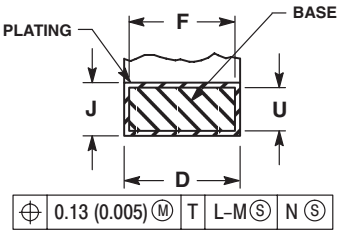
OUTLINE DIMENSIONS

FA SUFFIX
TQFP PACKAGE
CASE 848D-03
ISSUE D

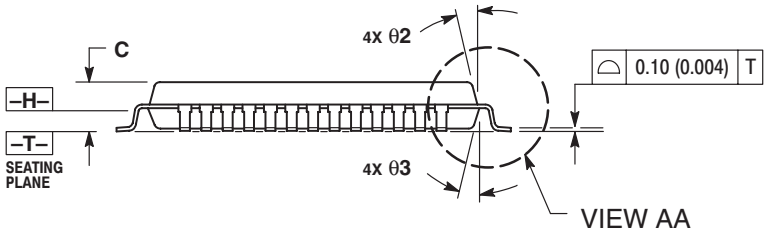




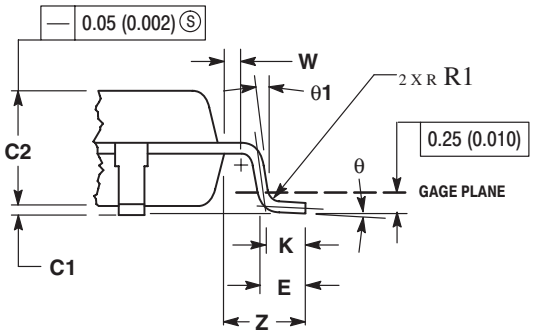
VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE



VIEW AA



VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	---	1.70	---	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	---	0°	---
θ2	12° REF		12° REF	
θ3	5°	13°	5°	13°

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