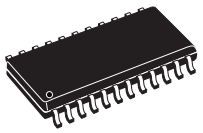
L6326

2 CHANNEL VOLTAGE SENSE AMR/GMR PREAMPLIFIERS

PRODUCT PREVIEW

- Power Supplies +5Vdc, +8Vdc
- Current bias or voltage bias (selectable) / Voltage sense architecture
- Single ended read input
- 24 pin TSSOP package, two channels
- External Resistor for read and write currents or trimmed internal resistor available (serial port selectable)
- Read channel -3dB bandwidth > 300MHz (Rmr=60 ohms, no interconnect)
- Input equivalent preamplifier voltage noise 0.5nV/rtHz typ
- Input equivalent MR bias current noise 10pA/rtHz typ
- MR bias current programmable (5 bit DAC) 1.8-8mA (GMR range), 3.8-10mA (AMR range)
- MR bias voltage programmable (5 bit DAC) 100-460mV (GMR range), 220-580mV (AMR range)
- Programmable gain (100V and 150V)
- Write frequency up to 250MHz (Lh=90nH,R=15 ohms, Ch=2pF, VDD=8V)
- Rise/Fall time <0.7ns (Iw =40mA 0-pk, Lh=90nH, Rh=15 ohms, Ch=2pF, VDD=8V)
- Write current programmable (5 bit DAC) 15-60mA
- Overshoot control 3 bit resolution (+1 bit for range)
- Bi-directional 16-bit TTLs Serial interface for head selection, read/write currents selection, chip parameters modification, chip enable, vendor code and fault status read back registers
- 2-wire mode selection (R/W, MRR)
- Bank write feature for servo write
- Digital buffered head voltage DBHV / Analog buffered head voltage ABHV pin (gain 5)
- Thermal asperity detection with adjustable sensitivity level (6 bit DAC)
- Thermal asperity correction
- Read head open/short detection
- Low supply detect and temperature monitoring (high temperature warning and Analog Temperature
- Diode Voltage measurement)
- Low write frequency detection
- WRITE to READ fast recovery 250ns (same head, including 150ns blanking period)
- GMR Low-Bias in WRITE mode with fast recovery to READ mode bias (250ns)
- Head-to-head switch in READ mode - 10µs (typ)
- Head and MR bias current switching transient current head protection
- READ-to-WRITE switching 30ns (same head)
- Programmable read bias during write and bank write operation
- ESD diodes for GMR protections
- Differential Write Driver to minimize coupling to GMR element



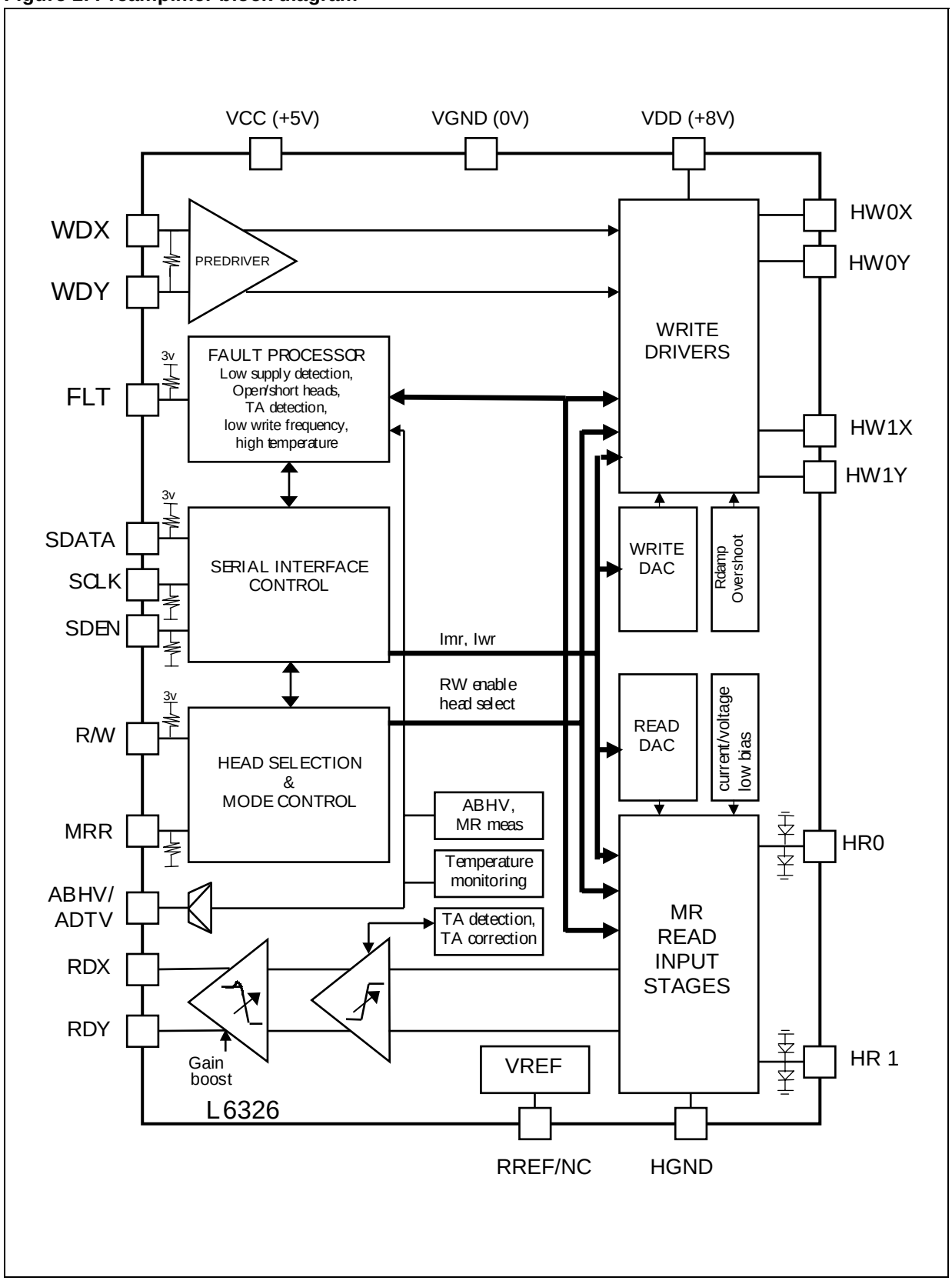
TSSOP24
ORDERING NUMBER: L6326

DESCRIPTION

The L6326 is a two channel BICMOS monolithic integrated circuit GMR pre-amplifier designed for use with four-terminal magneto-resistive (AMR and GMR heads) read/inductive write heads. The device consists of a voltage sense current bias or voltage bias (selectable), single ended input/ true differential output (RDX, RDY), low-noise high bandwidth read amplifier and includes fast current switching write drivers which support data rates up to 500 Mb/s with 90nH write heads.

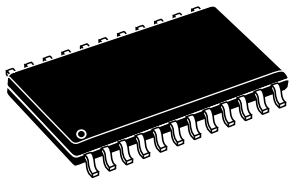
The GMR pre-amplifier provides programmable read current/voltage bias and write current (5 bit DACs), fault detection circuitry and servo writing features. Read amplifier gain, write current wave shape (overshoot and damping) can be adjusted and a thermal asperity detection and correction circuit can be enabled and programmed with different thresholds (6 bit DAC) through a 16-bit bi-directional serial interface (SDEN, SDATA, SCLK). The device operates from a +5V supply and a +8V supply (typical) for the write drivers. No external components are required if the internal trimmed resistor for reference current setting is selected.

Figure 1. Preamplifier block diagram

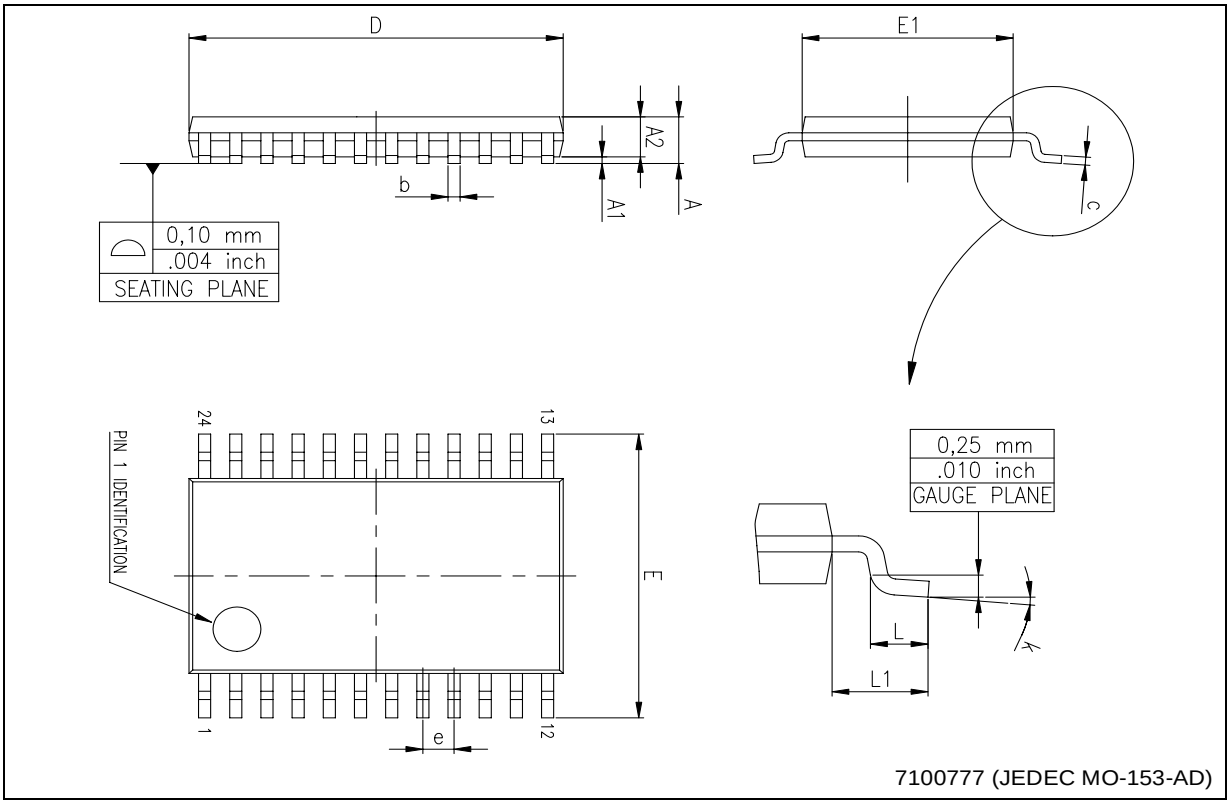


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.003		0.008
D	7.70	7.80	7.90	0.303	0.307	0.311
E		6.40			0.252	
E1	4.30	4.40	4.50	0.170	0.173	0.177
e		0.65			0.025	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0° min., 8° max.					

OUTLINE AND MECHANICAL DATA



TSSOP24
Thin Shrink Small Outline Package



7100777 (JEDEC MO-153-AD)