Integrated Circuit Systems, Inc.

ICS950403

Advance Information

AMD - K8™ System Clock Chip

Recommended Application:
AMD K8 System Clock with AMD, VIA or ALI Chipset

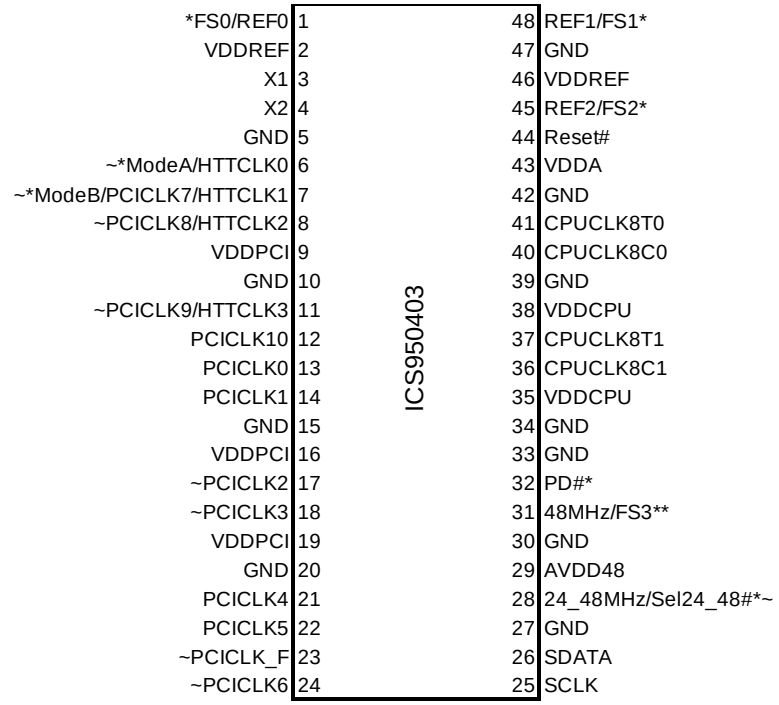
Output Features:

- 2 - Differential pair push-pull CPU clocks @ 3.3V
- 9 - PCICLK (Including 1 free running) @ 3.3V
- 3 - Selectable PCICLK/HTTCLK @ 3.3V
- 1 - HTTCLK @ 3.3V
- 1 - 48MHz @ 3.3V fixed.
- 1 - 24/48MHz @ 3.3V
- 3 - REF @ 3.3V, 14.318MHz.

Features:

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology and RESET# output to reset system
  if system malfunctions.
- Programmable watch dog safe frequency.
- Support I^2C Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.
- Supports Hyper Transport Technology (HTTCLK).

Pin Configuration



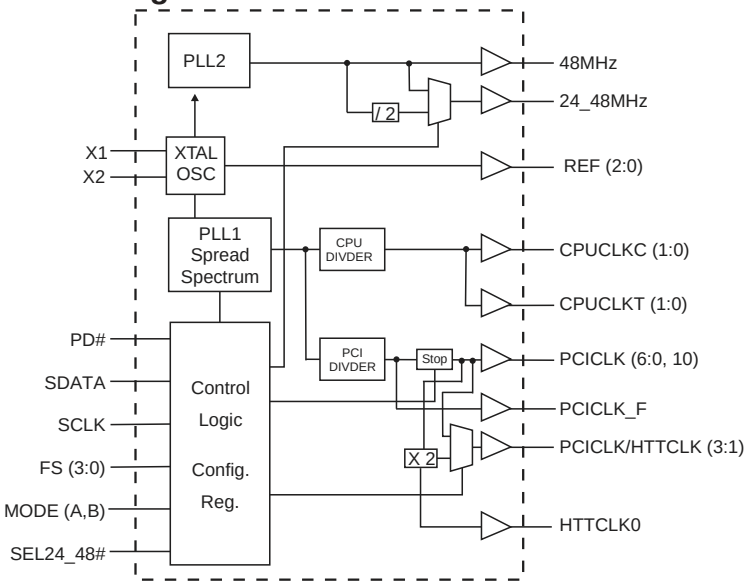
48-SSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

~ This Output has 2X Drive Strength

Block Diagram



Functionality

FS3	FS2	FS1	FS0	CPU MHz	HTT MHz	PCI MHz
0	0	0	0	100.90	67.27	33.63
0	0	0	1	133.90	66.95	33.48
0	0	1	0	168.00	67.20	33.60
0	0	1	1	202.00	67.33	33.67
0	1	0	0	100.20	66.80	33.40
0	1	0	1	133.50	66.75	33.38
0	1	1	0	166.70	66.68	33.34
0	1	1	1	200.40	66.80	33.40
1	0	0	0	150.00	60.00	30.00
1	0	0	1	180.00	60.00	30.00
1	0	1	0	210.00	70.00	35.00
1	0	1	1	240.00	60.00	30.00
1	1	0	0	270.00	67.50	33.75
1	1	0	1	233.33	66.67	33.33
1	1	1	0	266.67	66.67	33.33
1	1	1	1	300.00	75.00	37.50

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	*FS0/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
2	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
3	X1	IN	Crystal input,nominally 14.318MHz.
4	X2	OUT	Crystal output, Nominally 14.318MHz
5	GND	PWR	Ground pin.
6	~*ModeA/HTTCLK0	I/O	Mode selection latch input pin / Hyper Transport output.
7	~*ModeB/PCICLK7/HTTCLK	I/O	Mode selection latch input pin / PCI clock output / Hyper Transport output.
8	~PCICLK8/HTTCLK2	OUT	PCI clock output / Hyper Transport output.
9	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
10	GND	PWR	Ground pin.
11	~PCICLK9/HTTCLK3	OUT	PCI clock output / Hyper Transport output.
12	PCICLK10	OUT	PCI clock output.
13	PCICLK0	OUT	PCI clock output.
14	PCICLK1	OUT	PCI clock output.
15	GND	PWR	Ground pin.
16	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
17	~PCICLK2	OUT	PCI clock output.
18	~PCICLK3	OUT	PCI clock output.
19	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
20	GND	PWR	Ground pin.
21	PCICLK4	OUT	PCI clock output.
22	PCICLK5	OUT	PCI clock output.
23	~PCICLK_F	I/O	Free running PCI clock not affected by PCI_STOP#.
24	~PCICLK6	OUT	PCI clock output.
25	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
26	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
27	GND	PWR	Ground pin.
28	24_48MHz/Sel24_48#*~	I/O	24/48MHz clock output / Latched select input for 24/48MHz output. 0=48MHz, 1 = 24MHz.
29	AVDD48	PWR	Power for 24/48MHz outputs and fixed PLL core, nominal 3.3V
30	GND	PWR	Ground pin.
31	48MHz/FS3**	I/O	Frequency select latch input pin / Fixed 48MHz clock output. 3.3V
32	PD#*	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 1.8ms.
33	GND	PWR	Ground pin.
34	GND	PWR	Ground pin.
35	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
36	CPUCLK8C1	OUT	"Complementary" clocks of differential 3.3V push-pull K8 pair.
37	CPUCLK8T1	OUT	"True" clocks of differential 3.3V push-pull K8 pair.
38	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
39	GND	PWR	Ground pin.
40	CPUCLK8C0	OUT	"Complementary" clocks of differential 3.3V push-pull K8 pair.
41	CPUCLK8T0	OUT	"True" clocks of differential 3.3V push-pull K8 pair.
42	GND	PWR	Ground pin.
43	VDDA	PWR	3.3V power for the PLL core.
44	Reset#	OUT	Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low.
45	REF2/FS2*	I/O	14.318 MHz reference clock / Frequency select latch input pin.
46	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
47	GND	PWR	Ground pin.
48	REF1/FS1*	I/O	14.318 MHz reference clock / Frequency select latch input pin.

* Internal Pull-Up Resistor ** Internal Pull-Down Resistor ~ This Output has 2X Drive Strength

General Description

The **ICS950403** is a main system clock solution for desktop designs using the AMD K8 CPU. It provides all necessary clock signals for Clawhammer and Sledgehammer with AMD, VIA or ALI systems.

The **ICS950403** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Power Groups

Pin Number		Description
AVDD	GND	
2	5	Crystal
29	27, 30	48MHz fixed,
29	33	Fix Analog, Fix Digital
43	42	CPU Master Clock, CPU Analog
VDD	GND	
9	10	PCICLK/HTTCLK Outputs
16, 19	15, 20	PCICLK Outputs
35, 38	34, 39	CPU outputs
46	47	REF

Mode Functionality Tables

ModeA	ModeB	Pin7	Pin8	Pin11
0	0	HTTCLK1	HTTCLK2	PCICLK9
0	1	HTTCLK1	HTTCLK2	HTTCLK3
1	0	PCICLK7	PCICLK8	PCICLK9
1	1	HTTCLK1	PCICLK8	PCICLK9

General I^2C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	O		
	O		O
	O		O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
	O		O
	O		O
	O		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Table1: Frequency Selection Table

Bit5	Bit4	Bit3	Bit2	Bit1	CPU	HTT	PCI
	FS3	FS2	FS1	FS0	MHz	MHz	MHz
0	0	0	0	0	100.90	67.27	33.63
0	0	0	0	1	133.90	66.95	33.48
0	0	0	1	0	168.00	67.20	33.60
0	0	0	1	1	202.00	67.33	33.67
0	0	1	0	0	100.20	66.80	33.40
0	0	1	0	1	133.50	66.75	33.38
0	0	1	1	0	166.70	66.68	33.34
0	0	1	1	1	200.40	66.80	33.40
0	1	0	0	0	150.00	60.00	30.00
0	1	0	0	1	180.00	60.00	30.00
0	1	0	1	0	210.00	70.00	35.00
0	1	0	1	1	240.00	60.00	30.00
0	1	1	0	0	270.00	67.50	33.75
0	1	1	0	1	233.33	66.67	33.33
0	1	1	1	0	266.67	66.67	33.33
0	1	1	1	1	300.00	75.00	37.50
1	0	0	0	0	100.00	66.67	33.33
1	0	0	0	1	133.33	66.67	33.33
1	0	0	1	0	166.66	66.66	33.33
1	0	0	1	1	200.00	66.67	33.33
1	0	1	0	0	103.00	68.67	34.33
1	0	1	0	1	137.33	68.66	34.33
1	0	1	1	0	171.66	68.66	34.33
1	0	1	1	1	206.00	68.67	34.33
1	1	0	0	0	154.50	61.80	30.90
1	1	0	0	1	185.40	61.80	30.90
1	1	0	1	0	216.30	72.10	36.05
1	1	0	1	1	247.20	61.80	30.90
1	1	1	0	0	278.10	69.53	34.76
1	1	1	0	1	240.33	68.67	34.33
1	1	1	1	0	274.67	68.67	34.33
1	1	1	1	1	309.00	77.25	38.63

I²C Table: Functionality and Frequency Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	GSR_EN	Gear Shift Reset Enable	RW	Disable	Enable	0
Bit 6	-	-	SPREAD Enable	RW	Disable	Enable	0
Bit 5	-	-	FS4	RW	See Table1: Frequency Selection Table		0
Bit 4	-	-	FS3	RW			0
Bit 3	-	-	FS2	RW			0
Bit 2	-	-	FS1	RW			0
Bit 1	-	-	FS0	RW			0
Bit 0	-	FS Source	Frequency H/W IIC Select	RW	Latch Inputs	IIC	0

I²C Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	12	PCICLK10	Output Control	RW	Disable	Enable	1
Bit 6	24	PCICLK6	Output Control	RW	Disable	Enable	1
Bit 5	22	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 4	21	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 3	18	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 2	17	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 1	14	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 0	13	PCICLK0	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	37/36	CPUT/C_1	Output Control	RW	Disable	Enable	1
Bit 6	41/40	CPUT/C_0	Output Control	RW	Disable	Enable	1
Bit 5	45	REF2	Output Control	RW	Disable	Enable	1
Bit 4	48	REF1	Output Control	RW	Disable	Enable	1
Bit 3	1	REF0	Output Control	RW	Disable	Enable	1
Bit 2	28	24_48MHz	Output Control	RW	Disable	Enable	1
Bit 1	31	48MHz	Output Control	RW	Disable	Enable	1
Bit 0	-	WDSEN	Watchdog Soft Alarm Enable	RW	Disable	Enable	0

I²C Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	1
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

I²C Table: Read back

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WDHRB	WD Hard Alarm Status Read back	R	-	-	X
Bit 6	-	WDSRB	WD Soft Alarm Status Read back	R	-	-	X
Bit 5	-	24_48SEL	24_48SEL pin Control	R	By S/W	By Latched	1
Bit 4	-	FS3	FS3 on POR state	R	By S/W	By Latched	1
Bit 3	-	FS2	FS2 on POR state	R	By S/W	By Latched	1
Bit 2	-	FS1	FS1 on POR state	R	By S/W	By Latched	1
Bit 1	-	FS0	FS0 on POR state	R	By S/W	By Latched	1
Bit 0	-	Reserved	Reserved	R	-	-	0

I²C Table: Output Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	6	HTTCLK0	Output Control	RW	Disable	Enable	1
Bit 6	11	PCICLK9/HTTCLK3	Output Control	RW	Disable	Enable	1
Bit 5	8	PCICLK8/HTTCLK2	Output Control	RW	Disable	Enable	1
Bit 4	7	PCICLK7/HTTCLK1	Output Control	RW	Disable	Enable	1
Bit 3	23	PCICLK_F	Output Control	RW	Disable	Enable	1
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Byte Count Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	1
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

I²C Table: Vendor and Revision ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	0
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

I²C Table: Output Control Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Watchdog Timer Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	WD4	These bits represent X*290ms the watchdog timer will wait before it goes to alarm mode. Default is 16 X 290ms =4.64 seconds	RW	-	-	1
Bit 3	-	WD3		RW	-	-	0
Bit 2	-	WD2		RW	-	-	0
Bit 1	-	WD1		RW	-	-	0
Bit 0	-	WD0		RW	-	-	0

I²C Table: VCO Control Select Bit & WD Timer Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/NEN	M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	WDEN	Watchdog Enable	RW	Disable	Enable	0
Bit 5	-	WDFSEN	WD Safe Frequency Mode	RW	Latched FS/Byte0	WD B10 b(4:0)	0
Bit 4	-	WD SF4	Writing to these bit will configure the safe frequency as Byte0 bit (5:1)	RW	-	-	0
Bit 3	-	WD SF3		RW	-	-	0
Bit 2	-	WD SF2		RW	-	-	0
Bit 1	-	WD SF1		RW	-	-	0
Bit 0	-	WD SF0		RW	-	-	1

I²C Table: VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Bit 8	RW	-	-	X
Bit 6	-	M Div6	The decimal representation of M Div (6:0) + 2 is equal to reference divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 5	-	M Div5		RW	-	-	X
Bit 4	-	M Div4		RW	-	-	X
Bit 3	-	M Div3		RW	-	-	X
Bit 2	-	M Div2		RW	-	-	X
Bit 1	-	M Div1		RW	-	-	X
Bit 0	-	M Div0		RW	-	-	X

I²C Table: VCO Frequency Control Register

Byte 12		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		N Div7	The decimal representation of N Div (8:0) + 8 is equal to VCO divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 6	-		N Div6		RW	-	-	X
Bit 5	-		N Div5		RW	-	-	X
Bit 4	-		N Div4		RW	-	-	X
Bit 3	-		N Div3		RW	-	-	X
Bit 2	-		N Div2		RW	-	-	X
Bit 1	-		N Div1		RW	-	-	X
Bit 0	-		N Div0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 13		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		SSP7	These Spread Spectrum bits will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.	RW	-	-	X
Bit 6	-		SSP6		RW	-	-	X
Bit 5	-		SSP5		RW	-	-	X
Bit 4	-		SSP4		RW	-	-	X
Bit 3	-		SSP3		RW	-	-	X
Bit 2	-		SSP2		RW	-	-	X
Bit 1	-		SSP1		RW	-	-	X
Bit 0	-		SSP0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 14		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		Reserved	Reserved	RW	-	-	0
Bit 6	-		Reserved	Reserved	RW	-	-	0
Bit 5	-		SSP13	It is recommended to use ICS Spread % table for spread programming.	RW	-	-	X
Bit 4	-		SSP12		RW	-	-	X
Bit 3	-		SSP11		RW	-	-	X
Bit 2	-		SSP10		RW	-	-	X
Bit 1	-		SSP9		RW	-	-	X
Bit 0	-		SSP8		RW	-	-	X

I²C Table: Output Divider Control Register

Byte 15		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		PCI / HTTDiv3	PCICLK/HTTCLK divider ratio can be configured via these 4 bits individually.	RW	See Table 2: Divider Ratio Combination Table		X
Bit 6	-		PCI / HTTDiv2		RW			X
Bit 5	-		PCI / HTTDiv1		RW			X
Bit 4	-		PCI / HTTDiv0		RW			X
Bit 3	-		CPU Div3	CPU divider ratio can be configured via these 4 bits individually.	RW	See Table 2: Divider Ratio Combination Table		X
Bit 2	-		CPU Div2		RW			X
Bit 1	-		CPU Div1		RW			X
Bit 0	-		CPU Div0		RW			X

Table 2: Divider Ratio Combination Table

	Divider (3:2)								
Divider (1:0)	Bit	00		01		10		11	MSB
			1		2		4		8
	00	0000	2	0100	4	1000	8	1100	16
	01	0001	3	0101	6	1001	12	1101	24
	10	0010	5	0110	10	1010	20	1110	40
	11	0011	7	0111	14	1011	28	1111	56
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

I²C Table: Output Divider Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	X
Bit 6	-	Reserved	Reserved	RW	-	-	X
Bit 5	-	Reserved	Reserved	RW	-	-	X
Bit 4	-	Reserved	Reserved	RW	-	-	X
Bit 3	-	Reserved	Reserved	RW	-	-	X
Bit 2	-	Reserved	Reserved	RW	-	-	X
Bit 1	-	Reserved	Reserved	RW	-	-	X
Bit 0	-	Reserved	Reserved	RW	-	-	X

I²C Table: Output Divider Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	X
Bit 6	-	Reserved	Reserved	RW	-	-	X
Bit 5	-	Reserved	Reserved	RW	-	-	X
Bit 4	-	CPUINV	CPU Phase Invert	RW	Default	Inverse	X
Bit 3	-	Reserved	Reserved	RW	-	-	X
Bit 2	-	Reserved	Reserved	RW	-	-	X
Bit 1	-	Reserved	Reserved	RW	-	-	X
Bit 0	-	Reserved	Reserved	RW	-	-	X

I²C Table: Group Skew Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	CPUSkw3	All other clocks - CPUCLKT/C Skew Control	RW	See Table 3: 7-Steps Skew Programming Table		0
Bit 2	-	CPUSkw2		RW			0
Bit 1	-	CPUSkw1		RW			0
Bit 0	-	CPUSkw0		RW			0

Table 3: 7-Steps Skew Programming Table

7 Step	11	10	01	00	LSB
11	900 ps	750 ps	600 ps	450 ps	
10	N/A	N/A	N/A	300 ps	
01	N/A	N/A	N/A	150 ps	
00	N/A	N/A	N/A	0.0 ps	
MSB					

I²C Table: Group Skew Control Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		PCISkw3	CPU-PCICLK Skew Control	RW	See Table 3: 7-Steps Skew Programming Table		0
Bit 6		PCISkw2		RW			0
Bit 5		PCISkw1		RW			0
Bit 4		PCISkw0		RW			0
Bit 3	-	PCI/HTTSkw3	CPU-PCICLK /HTTCLK Skew Control	RW	See Table 3: 7-Steps Skew Programming Table		0
Bit 2	-	PCI/HTTSkw2		RW			0
Bit 1	-	PCI/HTTSkw1		RW			0
Bit 0	-	PCI/HTTSkw0		RW			0

I²C Table: Group Skew Control Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	1
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

I²C Table: Slew Rate Control Register

Byte 21	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	ASEL	Async Frequency Select	RW	66.0MHz	75.4MHz	0
Bit 0	-	AEN	AGP/PCI/ Freq Source Select	RW	Fix PLL	CPU PLL	1

I²C Table: Drive Strength Control Register

Byte 22	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCI9/HTT3 DrCntrl	PCICLK9/HTTCLK3 Drive Strength Control	RW	1X	2X	1
Bit 6	-	PCI6Drv	PCICLK6 Drive Strength Control	RW	1X	2X	1
Bit 5	-	PCI3Drv	PCICLK3 Drive Strength Control	RW	1X	2X	1
Bit 4	-	PCI2Drv	PCICLK2 Drive Strength Control	RW	1X	2X	1
Bit 3	-	PCIFDrv	PCICLK_F Drive Strength Control	RW	1X	2X	1
Bit 2	-	24_48Drv	24_48MHz Drive Strength Control	RW	1X	2X	1
Bit 1	-	PCI8/HTT2 DrCntrl	PCICLK8/HTTCLK2 Drive Strength Control	RW	1X	2X	1
Bit 0	-	PCI7/HTT1 DrCntrl	PCICLK7/HTTCLK1 Drive Strength Control	RW	1X	2X	1

I²C Table: Slew Rate Control Register

Byte 23	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	PCISlw1	PCICLK(1:0) Slew Rate Control	RW	-	-	1
Bit 2	-	PCISlw0		RW	-	-	0
Bit 1	-	PCISlw1	PCICLK(10, 5:4) Slew Rate Control	RW	-	-	1
Bit 0	-	PCISlw0		RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 24	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	REFSlw1	REF(2:0) Slew Rate Control	RW	-	-	1
Bit 6	-	REFSlw0		RW	-	-	0
Bit 5	-	48MSlw1	48MHz Slew Rate Control	RW	-	-	1
Bit 4	-	48MSlw0		RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

Absolute Maximum Ratings

Supply Voltage 3.8V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +3.8 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C
ESD Protection . . . . . Input ESD protection usung human body model > 1KV

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66MHz			180	mA
	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100MHz				
	$I_{DD3.3OP133}$	C_L = 0 pF; Select @ 133MHz				
Power Down	PD				600	mA
Input frequency	F_i	V_{DD} = 3.3 V;	10	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Z_O	$V_O = V_X$	15		55	Ω
Output High Voltage	V_{OH2B}		1		1.2	V
Output Low Voltage	V_{OL2B}				0.4	V
Output Low Current	I_{OL2B}	V_{OL} = 0.3 V	18			mA
Rise Edge Rate[1]		Measured from 20-80%	2		7	V/ns
Fall Edge Rate[1]		Measured from 80-20%	2		7	V/ns
V_{DIFF}		Differential Voltage, Measured @ the Hammer test load (single-ended measurement)	0.4		2.3	V
DV_{DIFF}		Change in V_{DIFF_DC} magnitude, Measured @ the Hammer test load (single-ended measurement)	-150		150	mV
V_{CM}		Common Mode Voltage, Measured @ the Hammer test load (single-ended measurement)	1.05		1.45	V
DV_{CM}		Change in Common Mode Voltage, Measured @ the Hammer test load (single-ended measurement)	-200		200	mV
Duty Cycle[1]	d_{t2B}	V_T = 50%	45		53	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	$V_T = V_X$	0		200	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

2 - V_{DIF} specifies the minimum input differential voltages (V_{TR}-V_{CP}) required for switching, where V_{TR} is the "true" input level and V_{CP} is the "complement" input level.

3 - $Vpullup_{(external)}$ = 1.5V, Min = $Vpullup_{(external)}$/2-150mV; Max=($Vpullup_{(external)}$/2)+150mV

Electrical Characteristics - PCICLK/HTTCLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.0 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-15	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	10			mA
Rise Edge Rate[1]		Measured from 20-60%	1		4	V/ns
Fall Edge Rate[1]		Measured from 60-20%	1		4	V/ns
Duty Cycle[1]	d_{t1}	V_T = 50%	45		55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	Measured on rising edge @ 1.5V			250	ps
Jitter, Accumulated[1]			-1000		1000	ps
Output Impedance	Z_O	$V_O = V_X$	12		55	W

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.0 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-15	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	10			mA
Rise Edge Rate[1]		Measured from 20-60%	1		4	V/ns
Fall Edge Rate[1]		Measured from 60-20%	1		4	V/ns
Duty Cycle[1]	d_{t1}	V_T = 50%	45		55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	Measured on rising edge @ 1.5V			250	ps
Jitter, Accumulated[1]			-1000		1000	ps
Output Impedance	Z_O	$V_O = V_X$	12		55	W

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Edge Rate[1]		Measured from 20-80%	0.5		2	V/ns
Fall Edge Rate[1]		Measured from 80-20%	0.5		2	V/ns
Duty Cycle[1]	d_{t5}	V_T = 50%	45		55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	Mesured on rising edge @ 1.5V	0		1000	ps
Jitter, Accumulated[1]			-1000		1000	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 24MHz, 48MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Edge Rate[1]		Measured from 20-80%	0.5		2	V/ns
Fall Edge Rate[1]		Measured from 80-20%	0.5		2	V/ns
Duty Cycle[1]	d_{t5}	V_T = 50%	45		55	%
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V	-1		1	ns
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	$V_T = V_X$, for 24_48MHz clock	0		500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	$V_T = V_X$, for 48MHz clock	0		200	ps
Output Impedance	Z_O	$V_O = V_X$	20		60	W

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS950403 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

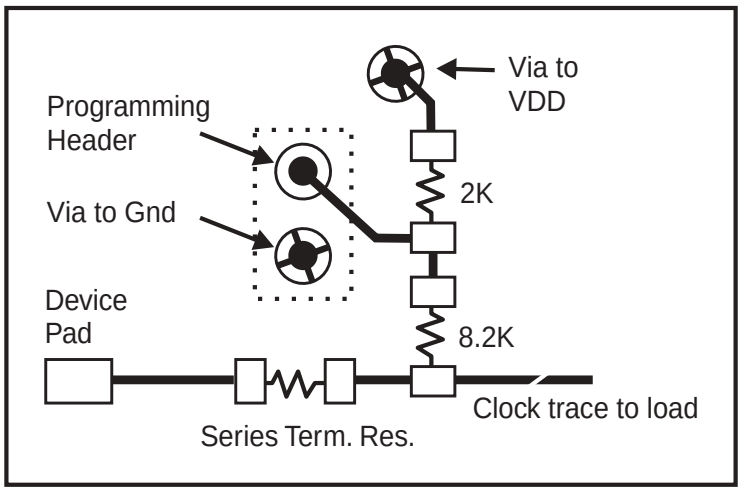
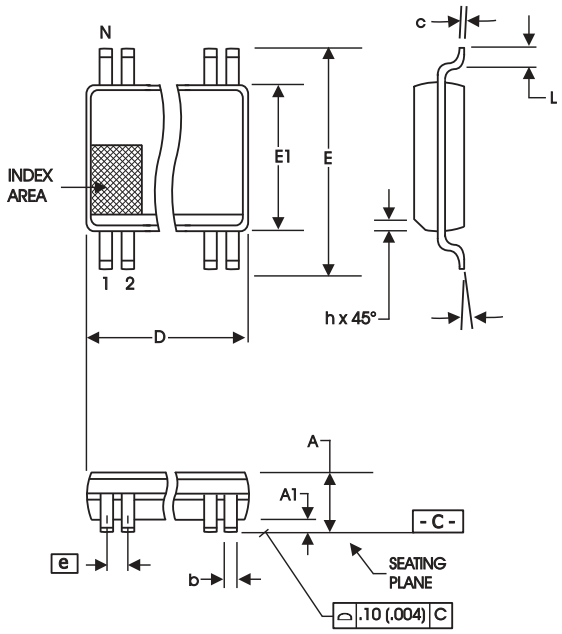


Fig. 1



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS950403yFT

Example:

ICS XXXXXX y F - T

Designation for tape and reel packaging

Package Type
F = SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix
ICS = Standard Device

0732—01/27/03