

HD74HC589

8-bit Serial of Parallel-input/Serial-output Shift Register (with 3-state outputs)

HITACHI

Description






The HD74HC589 is similar in function to the HD74HC597, which is not a 3-state device.

This device consists of an 8-bit storage latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table). The shift register output, O_H , is a three-state output, allowing this device to be used in bus-oriented systems.

Features

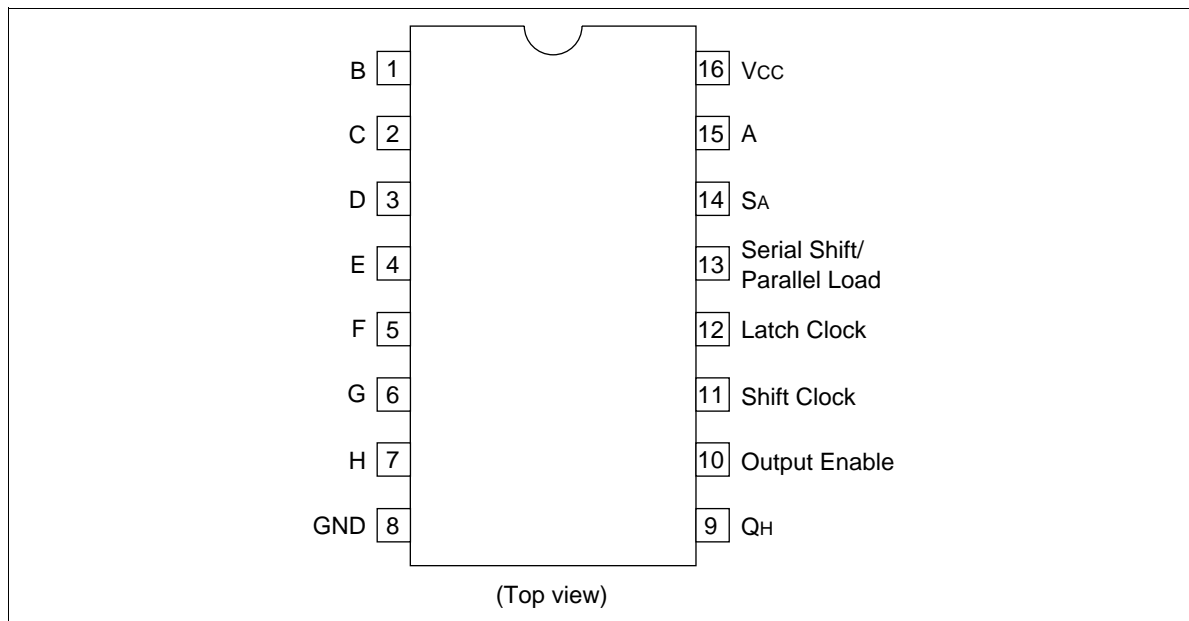
- High Speed Operation: t_{pd} (Shift Clock to Q_H) = 15 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

Function Table

Latch Clock LCK	Shift Clock SCK	Serial Shift/ Parallel Load	Output Enable OE	Function
	X	X	X	Data are loaded into input latches
	X	L	L	Data are loaded from input into shift registers
X	X	L	L	Data are transferred from input latches to shift registers
L, H, 	L, H, 	X	H	Outputs are disabled
X		H	L	Serial shift $Q_n = Q_{n-1}$, $Q_0 = \text{SER}$

HD74HC589

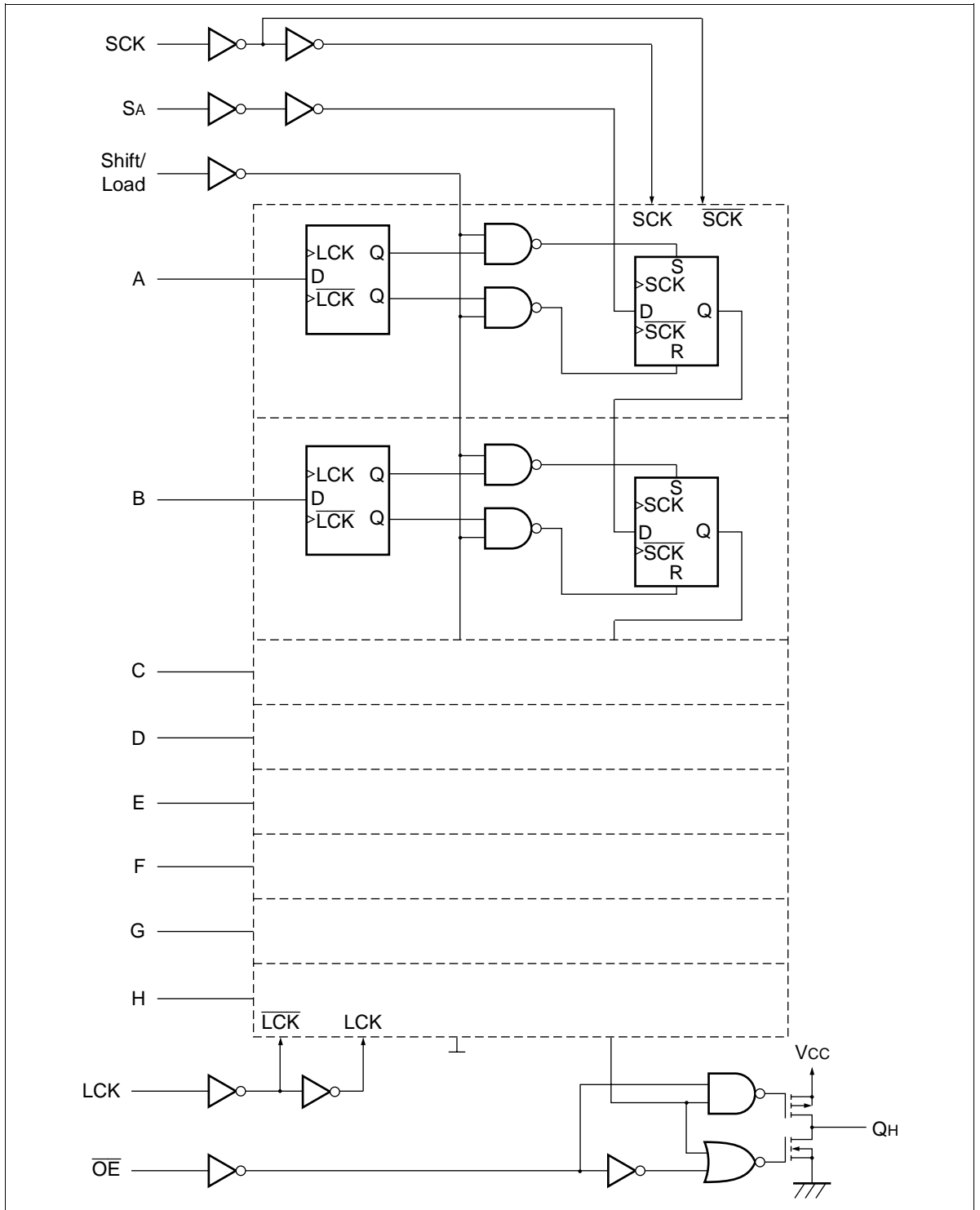
Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Output current	I_{OUT}	± 35	mA
DC current drain per V_{CC} , GND	I_{CC1} , I_{GND}	± 75	mA
DC input diode current	I_{IK}	± 20	mA
DC output diode current	I_{OK}	± 20	mA
Power Dissipation per package	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	°C

Logic Diagram



HD74HC589

DC Characteristics

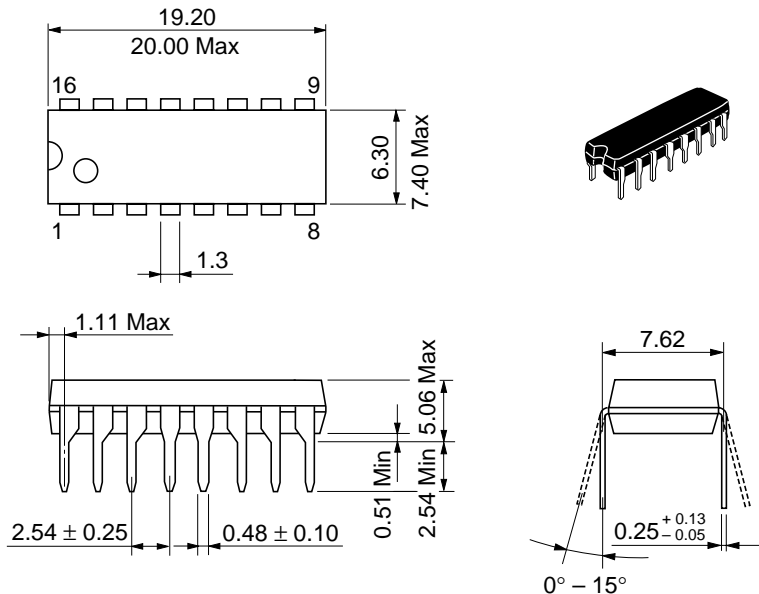
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -6 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -7.8 mA
		6.0	—	0.0	0.1	—	0.1			V
	V _{OL}	4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33	I _{OL} = 6 mA		
		6.0	—	—	0.26	—	0.33	I _{OL} = 7.8 mA		
		6.0	—	—	±0.5	—	±5.0	μA	Vin = V _{IH} or V _{IL} , Vout = V _{CC} or GND	
		Off-state output current	I _{OZ}	6.0	—	—	±0.5	—		±5.0
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, Iout = 0 μA	

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

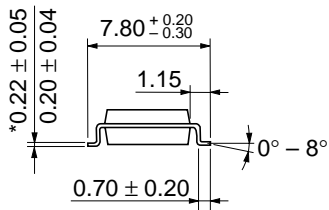
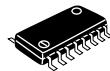
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	t_{PLH}	2.0	—	—	200	—	250	ns	Latch clock to Q_H
		4.5	—	20	40	—	50		
		6.0	—	—	34	—	43		
	t_{PHL}	2.0	—	—	175	—	220	ns	Shift clock to Q_H
		4.5	—	15	35	—	44		
		6.0	—	—	30	—	37		
t_{PLH}	2.0	—	—	175	—	220	ns	Serial shift/prallel load to Q_H	
	4.5	—	16	35	—	44			
	6.0	—	—	30	—	37			
Output enable time	t_{ZL}	2.0	—	—	150	—	190	ns	
		4.5	—	9	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	t_{LZ}	2.0	—	—	150	—	190	ns	
		4.5	—	14	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	Data to latch clock
		4.5	20	1	—	25	—		
		6.0	17	—	—	21	—		
	t_{su}	2.0	100	—	—	125	—	ns	S_A to shift clock
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
	t_{su}	2.0	100	—	—	125	—	ns	Serial shift/parallel load to shift clock
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns) (cont)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$		$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions		
			Min	Typ	Max	Min			Max	
Hold time	t_h	2.0	5	—	—	5	—	ns	Latch clock to data	
		4.5	5	0	—	5	—			
		6.0	5	—	—	5	—			
	t_h	t_h	2.0	5	—	—	5	—	ns	Shift clock to S_A
			4.5	5	—	—	5	—		
			6.0	5	—	—	5	—		
	t_h	t_h	2.0	5	—	—	5	—	ns	Shift clock to serial shift/ parallel load
			4.5	5	—	—	5	—		
			6.0	5	—	—	5	—		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns		
	t_{THL}	4.5	—	5	15	—	19			
	t_{THL}	6.0	—	—	13	—	16			
Input capacitance	C_{in}	—	—	5	10	—	10	pF		



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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