DS2148/Q48
3.3V/5V E1/T1/J1 Line Interface

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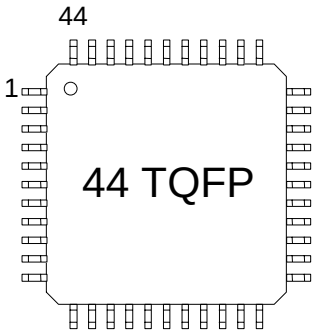
FEATURES

- Complete E1, T1, or J1 Line Interface Unit
- Supports both long and short haul trunks
- Internal software-selectable receive-side termination for 75/100/120Ω
- 3.3V or 5V (CMOS) in same device
- 32-bit or 128-bit crystal-less jitter attenuator requires only a 2.048 MHz master clock for both E1 and T1 with option to use 1.544 MHz for T1
- Generates the appropriate line build outs, with and without return loss, for E1 and DSX-1 and CSU line build outs for T1
- AMI, HDB3, and B8ZS, encoding/decoding
- 16.384 MHz, 8.192 MHz, 4.096 MHz, or 2.048 MHz clock output synthesized to recovered clock
- Programmable monitor mode for receiver
- Loopbacks and PRBS pattern generation/ detection with output for received errors
- Generates/detects in-band loop codes, 1 to 16 bits including CSU loop codes
- 8-bit parallel or serial interface with optional hardware mode
- MUX'd and Non-MUX'd parallel bus supports Intel or Motorola
- Detects/generates blue (AIS) alarms
- NRZ/bipolar interface for TX/RX data I/O
- Transmit open circuit detection
- Receive Carrier Loss (RCL) indication (G.775)
- HIGHZ State for TTIP and TRING
- 50 mA (rms) current limiter

PIN DESCRIPTION



7 mm CABGA

ORDERING INFORMATION

DS2148TN	44 pin TQFP	(–40°C to +85°C)
DS2148T	44 pin TQFP	(0° C – 70° C)
DS2148GN	7mm CABGA	(–40°C to +85°C)
DS2148G	7mm CABGA	(0° C – 70° C)
DS21Q48N	(Quad) BGA	(–40°C to +85°C)
DS21Q48	(Quad) BGA	(0° C – 70° C)

DESCRIPTION

The DS2148 is a complete selectable E1 or T1 Line Interface Unit (LIU) for short haul and long haul applications. Throughout the data sheet, J1 is represented wherever T1 exists. Receive sensitivity adjusts automatically to the incoming signal and can be programmed for 0-12 dB or 0-43 dB for E1 applications and 0-30 dB or 0-36 dB for T1 applications. The device can generate the necessary G.703 E1 waveshapes in 75 ohm or 120 ohms applications and DSX-1 line build outs or CSU line build outs of

0 dB, -7.5 dB, -15 dB, and -22.5 dB for T1 applications. The crystal-less onboard jitter attenuator requires only a 2.048 MHz MCLK for both E1 and T1 applications (with the option of using a 1.544 MHz MCLK in T1 applications). The jitter attenuator FIFO is selectable to either 32 bits or 128 bits in depth and can be placed in either the transmit or receive data paths. An n X 2.048 MHz output clock synthesized to RCLK is available for use as a backplane system clock (where n = 1, 2, 4, or 8). The DS2148 has diagnostic capabilities such as loopbacks and PRBS pattern generation/detection. 16-bit loop-up and loop-down codes can be generated and detected. The device can be controlled via an 8-bit parallel MUX'd or non-MUX'd port, serial port or used in hardware mode. The device fully meets all of the latest E1 and T1 specifications including ANSI T1.403-1999, ANSI T1.408, AT&T TR 62411, ITU G.703, G.704, G.706, G.736, G.775, G.823, I.431, O.151, O.161, ETSI ETS 300 166, JTG.703, JTI.431, JJ-20.1, TBR12, TBR13, and CTR4.

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3. INTRODUCTION

The analog AMI/HDB3 waveform off of the E1 line or the AMI/B8ZS waveform off of the T1 line is transformer coupled into the RTIP and RRING pins of the DS2148. The user has the option to use internal termination, software selectable for 75/100/120Ω applications, or external termination. The device recovers clock and data from the analog signal and passes it through the jitter attenuation MUX outputting the received line clock at RCLK and bipolar or NRZ data at RPOS and RNEG. The DS2148 contains an active filter that reconstructs the analog received signal for the nonlinear losses that occur in transmission. The receive circuitry is also configurable for various monitor applications. The device has a usable receive sensitivity of 0 dB to –43 dB for E1 and 0 dB to –36 dB for T1 which allows the device to operate on 0.63 mm (22AWG) cables up to 2.5 km (E1) and 6k feet (T1) in length. Data input at TPOS and TNEG is sent via the jitter attenuation MUX to the waveshaping circuitry and line driver. The DS2148 will drive the E1 or T1 line from the TTIP and TRING pins via a coupling transformer. The line driver can handle both CEPT 30/ISDN-PRI lines for E1 and long haul (CSU) or short haul (DSX-1) lines for T1.

3.1 DOCUMENT REVISION HISTORY

DATE	CHANGE
9-17-99	100Ω / 60Ω termination reversed in INTERNAL RX TERMINATION SELECT tables
9-28-99	Add DS21Q48 pinout
12-06-99	Correct VSM pin number in Q48 (12 x 12 BGA) from G5 to G4
03-29-00	Add timing diagram for Status Register (write access mode); Add mechanical dimensions for the quad version
05-03-00	Timing diagram for Status Register (write access mode) added. Elaboration on burst mode bit. Add mechanical dimensions for the quad version.

Figure 3-1 **DS2148 BLOCK DIAGRAM**

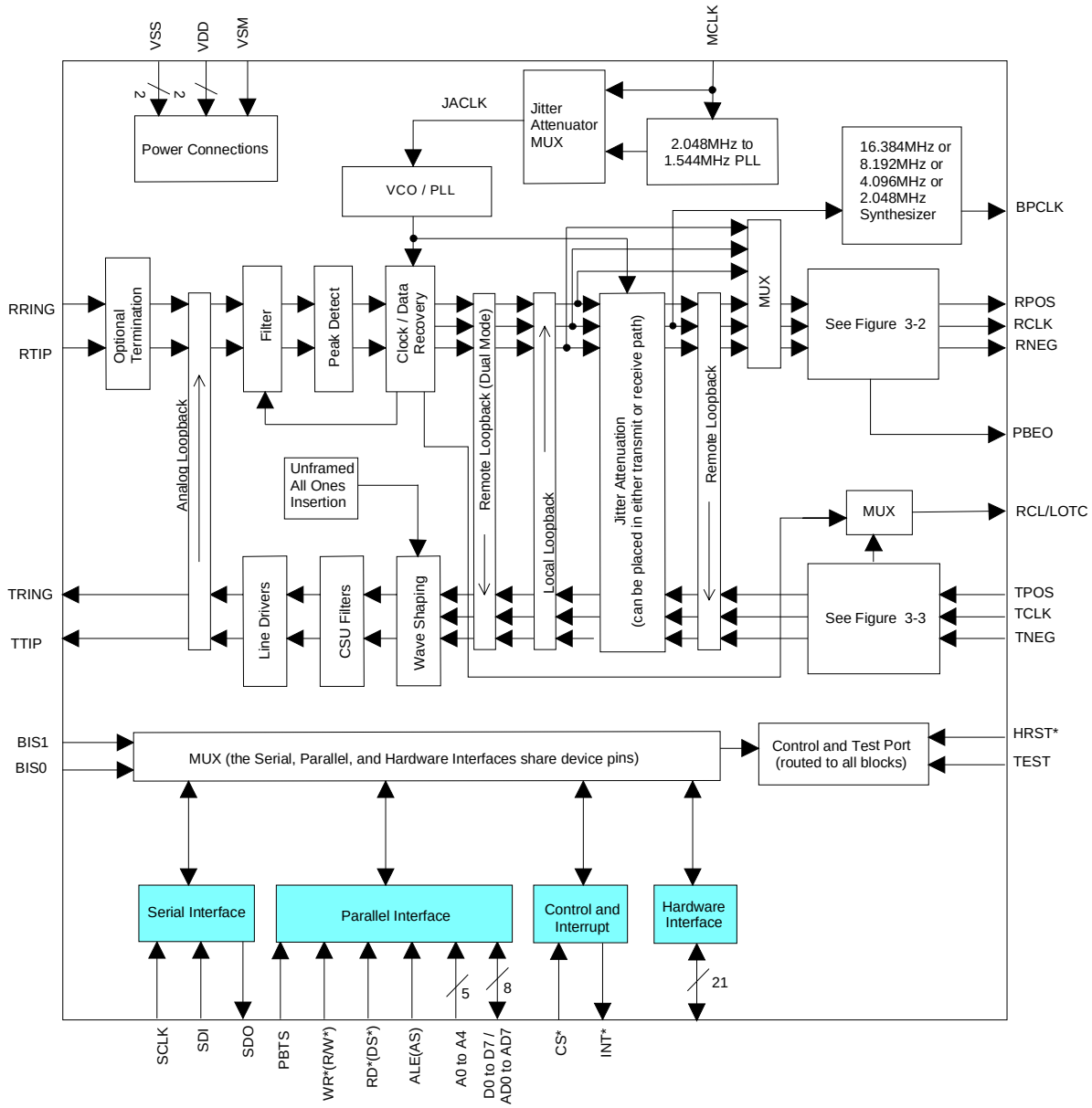


Figure 3-2 **RECEIVE LOGIC**

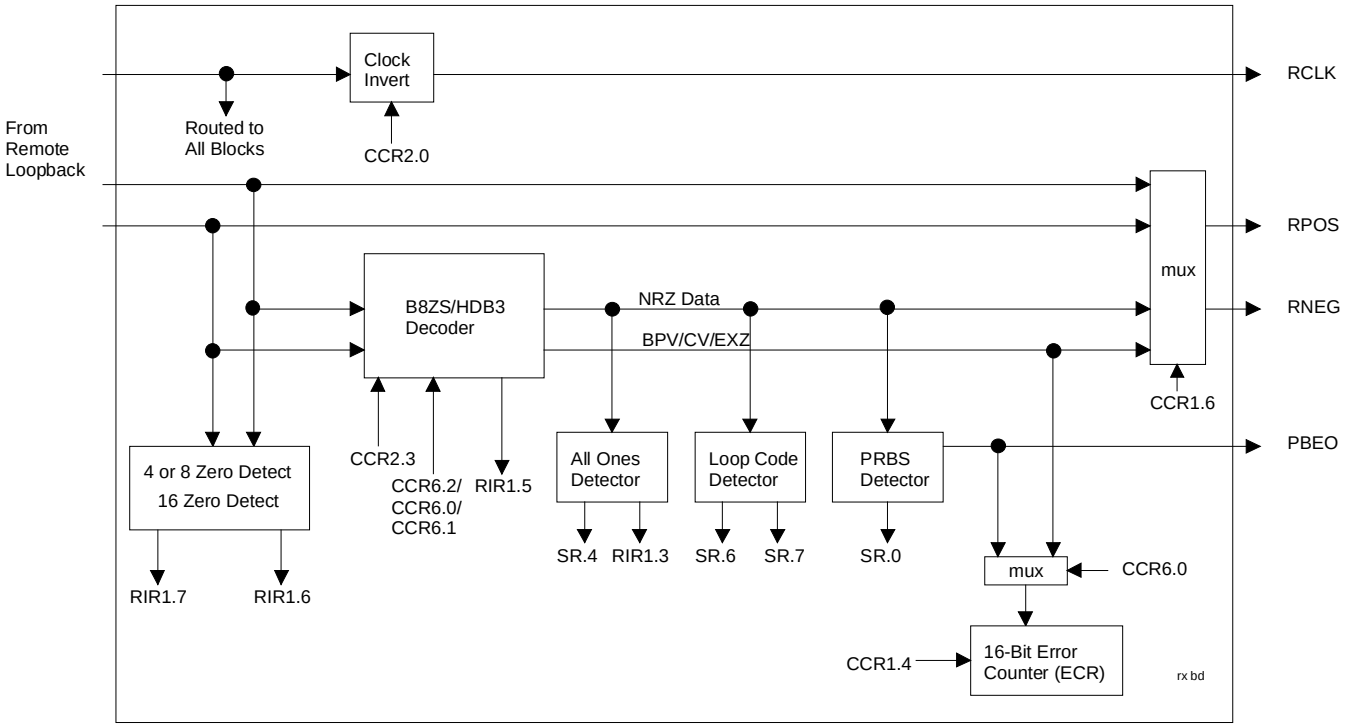
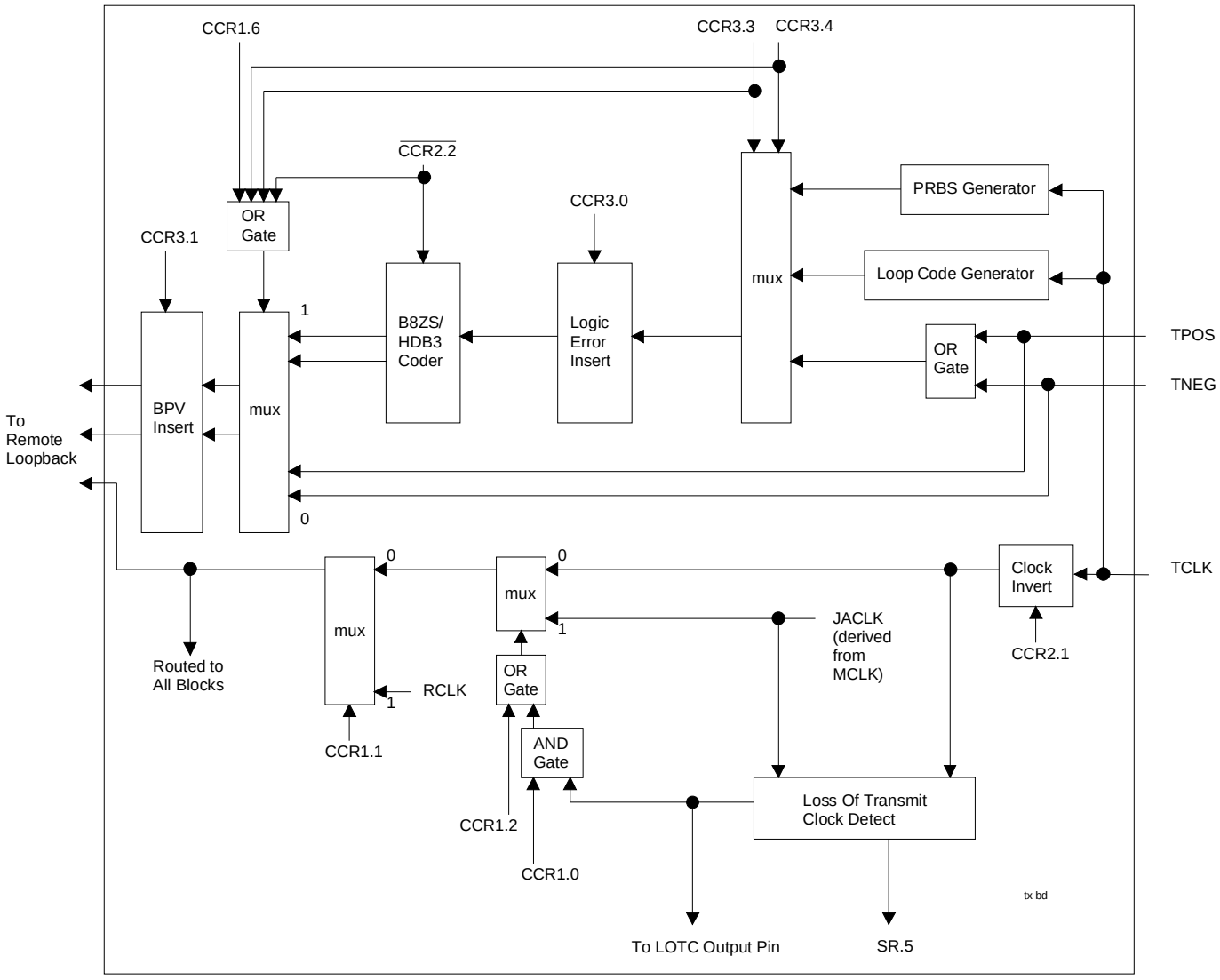


Figure 3-3 **TRANSMIT LOGIC**



4. PIN DESCRIPTION

The DS2148 can be controlled in a Parallel Port Mode, a Serial Port Mode, or a Hardware Mode. See Table 4-1. The Parallel and Serial Port Modes are described in Section 3, and the Hardware Mode is described below.

Table 4-1 **BUS INTERFACE SELECTION**

BIS1	BIS0	BUS INTERFACE TYPE
0	0	Parallel Port Mode (multiplexed)
0	1	Parallel Port Mode (non-multiplexed)
1	0	Serial Port Mode
1	1	Hardware Mode

Table 4-2 **PIN ASSIGNMENT**

DS2148T PIN #	DS2148G PIN#	I/O	Parallel Port Mode	Serial Port Mode	Hardware Mode
1	C3	I	CS*	CS*	EGL
2	C2	I	RD*(DS*)	NA	ETS
3	B1	I	WR*(R/W*)	NA	NRZE
4	D2	I	ALE(AS)	NA	SCLKE
5	C1	I	NA	SCLK	L2
6	D3	I	NA	SDI	L1
7	D1	I/O	A4	SDO	L0
8	E1	I	A3	ICES	DJA
9	F2	I	A2	OCES	JAMUX
10	F1	I	A1	NA	JAS
11	G1	I	A0	NA	HBE
12	E3	I/O	D7/AD7	NA	CES
13	F3	I/O	D6/AD6	NA	TPD
14	G2	I/O	D5/AD5	NA	TX0
15	F4	I/O	D4/AD4	NA	TX1
16	G3	I/O	D3/AD3	NA	LOOP0
17	E4	I/O	D2/AD2	NA	LOOP1
18	G4	I/O	D1/AD1	NA	MM0
19	F5	I/O	D0/AD0	NA	MM1
20	G5	I	VSM	VSM	VSM
21	F6	-	VDD	VDD	VDD
22	G6	-	VSS	VSS	VSS
23	E5	I/O	INT*	INT*	RT1
24	E6	O	PBEO	PBEO	PBEO
25	F7	O	RCL/LOTC	RCL/LOTC	RCL
26	D6	I	TEST	TEST	TEST
27	D5	I	RTIP	RTIP	RTIP
28	D7	I	RRING	RRING	RRING
29	C6	I	HRST*	HRST*	HRST*
30	C7	I	MCLK	MCLK	MCLK
31	B6	O	BPCLK	BPCLK	BPCLK
32	B7	I	BIS0	BIS0	BIS0
33	A7	I	BIS1	BIS1	BIS1
34	C5	O	TTIP	TTIP	TTIP
35	B5	-	VSS	VSS	VSS
36	A6	-	VDD	VDD	VDD
37	B4	O	TRING	TRING	TRING
38	C4	O	RPOS	RPOS	RPOS
39	A4	O	RNEG	RNEG	RNEG
40	B3	O	RCLK	RCLK	RCLK
41	A3	I	TPOS	TPOS	TPOS
42	B2	I	TNEG	TNEG	TNEG
43	A2	I	TCLK	TCLK	TCLK
44	A1	I	PBTS	NA	RT0

Table 4-3 **PIN DESCRIPTIONS** (Sorted by Pin Name, DS2148T Pin Numbering)

Acronym	Pin	I/O	Description
A0 To A4	11 to 7	I	**Address Bus.** In non-multiplexed bus operation (BIS1 = 0, BIS0 = 1), serves as the address bus. In multiplexed bus operation (BIS1 = 0, BIS0 = 0), these pins are not used and should be tied low.
ALE (AS)	4	I	**Address Latch Enable (Address Strobe).** When using the parallel port (BIS1 = 0) in multiplexed bus mode (BIS0 = 0), serves to demultiplex the bus on a positive-going edge. In non-multiplexed bus mode (BIS0 = 1), should be tied low.
BIS0/ BIS1	32/ 33	I	**Bus Interface Select Bits 0 & 1.** Used to select bus interface option. See Table 4-1 for details.
BPCLK	31	O	**Back Plane Clock.** A 16.384 MHz, 8.192 MHz, 4.096 MHz, or 2.048 MHz clock output that is referenced to RCLK selectable via CCR5.7 and CCR5.6. In hardware mode, defaults to 16.384 MHz output.
CES	12	I	**Receive & Transmit Clock Edge Select.** Selects which RCLK edge to update RPOS and RNEG and which TCLK edge to sample TPOS and TNEG. CES combines TCES (CCR2.1) and RCES (CCR2.0) 0 = update RNEG/RPOS on rising edge of RCLK; sample TPOS/TNEG on falling edge of TCLK 1 = update RNEG/RPOS on falling edge of RCLK; sample TPOS/TNEG on rising edge of TCLK
CS*	1	I	**Chip Select.** Must be low to read or write to the device. CS* is an active low signal.
D0 / AD0 To D7 / AD7	19 to 12	I/O	**Data Bus / Address/Data Bus.** In non-multiplexed bus operation (BIS1 = 0, BIS0 = 1), serves as the data bus. In multiplexed bus operation (BIS1 = 0, BIS0 = 0), serves as an 8-bit multiplexed address/data bus.
DJA	8	I	**Disable Jitter Attenuator.** 0 = jitter attenuator enabled 1 = jitter attenuator disabled
EGL	1	I	**Receive Equalizer Gain Limit.** This bit controls the sensitivity of the receive equalizer. See Table 4-6.
ETS	2	I	**E1/T1 Select.** 0 = E1 1 = T1
HBE	11	I	**Receive & Transmit HDB3/B8ZS Enable.** HBE combines RHBE (CCR2.3) and THBE (CCR2.2). 0 = enable HDB3 (E1) / B8ZS (T1) 1 = disable HDB3 (E1) / B8ZS (T1)
HRST*	29	I	**Hardware Reset.** Bringing HRST* low will reset the DS2148 setting all control bits to their default state of all zeros.
ICES	8	I	**Input Clock Edge Select.** Selects whether the serial port data input (SDI) is sampled on rising (ICES =0) or falling edge (ICES = 1) of SCLK.
INT*	23	O	**Interrupt [INT*] pin 23.** Flags host controller during conditions and change of conditions defined in the Status Register. Active low, open drain output.

Acronym	Pin	I/O	Description
JAMUX	9	I	**Jitter Attenuator MUX.** Controls the source for JACLK. See **Figure 3-1**and Table 4-9. 0 = JACLK sourced from MCLK (2.048 MHz or 1.544 MHz at MCLK) 1 = JACLK sourced from internal PLL (2.048 MHz at MCLK)
JAS	10	I	**Jitter Attenuator Select.** 0 = place the jitter attenuator on the receive side 1 = place the jitter attenuator on the transmit side
L0/L1/L2	7/ 6/ 5	I	**Transmit LIU Waveshape Select Bits 0 & 1 [H/W Mode].** These inputs determine the waveshape of the transmitter. See Table 9-1 & Table 9-2.
LOOP0/ LOOP1	16/ 17	I	**Loopback Select Bits 0 & 1 [H/W Mode].** These inputs determine the active loopback mode (if any). See Table 4-4.
MCLK	30	I	**Master Clock.** A 2.048 MHz (+/-50 ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. Use of a T1 1.544 MHz clock source is optional. See note 2 on clock accuracy at the end of this table.
MM0/ MM1	18/ 19	I	**Monitor Mode Select Bits 0 & 1 [H/W Mode].** These inputs determine if the receive equalizer is in a monitor mode. See Table **4-7**.
NA	-	I	**Not Assigned.** Should be tied low.
NRZE	3	I	**NRZ Enable [H/W Mode].** 0 = Bipolar data at RPOS/RNEG and TPOS/TNEG 1 = NRZ data at RPOS and TPOS or TNEG; RNEG outputs a positive going pulse when device receives a BPV, CV, or EXZ.
OCES	9	I	**Output Clock Edge Select.** Selects whether the serial port data output (SDO) is valid on the rising (OCES = 1) or falling edge (OCES = 0) of SCLK.
PBEO	24	O	**PRBS Bit Error Output.** The receiver will constantly search for a 2^{15}-1 or a 2^{20}-1 PRBS depending on the ETS bit setting (CCR1.7). Remains high if out of synchronization with the PRBS pattern. Goes low when synchronized to the PRBS pattern. Any errors in the received pattern after synchronization will cause a positive going pulse (with same period as E1 or T1 clock) synchronous with RCLK. PRBS bit errors can also be reported to the ECR1 and ECR2 registers by setting CCR6.2 to a logic 1.
PBTS	44	I	**Parallel Bus Type Select.** When using the parallel port (BIS1 = 0), set high to select Motorola bus timing, set low to select Intel bus timing. This pin controls the function of the RD*(DS*), ALE(AS), and WR*(R/W*) pins. If PBTS = 1 and BIS1 = 0, then these pins assume the Motorola function listed in parenthesis (). In serial port mode, this pin should be tied low.
RCLK	40	O	**Receive Clock.** Buffered recovered clock from the line. Synchronous to MCLK in absence of signal at RTIP and RRING.

Acronym	Pin	I/O	Description
RD* (DS*)	2	I	**Read Input (Data Strobe).** RD* and DS* are active low signals. DS active low when in non-multiplexed, Motorola mode. See the Bus Timing Diagrams in section 5.
RCL/ LOTC	25	O	**Receive Carrier Loss / Loss of Transmit Clock.** An output which will toggle high during a receive carrier loss (CCR2.7 = 0) or will toggle high if the TCLK pin has not been toggled for 5 µsec ± 2 µsec (CCR2.7 = 1). CCR2.7 defaults to logic 0 when in hardware mode.
RNEG	39	O	**Receive Negative Data.** Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with the bipolar data out of the line interface. Set NRZE (CCR1.6) to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See section 8.4 for details.
RPOS	38	O	**Receive Positive Data.** Updated on the rising edge (CCR2.0 = 0) or the falling edge (CCR2.0 = 1) of RCLK with bipolar data out of the line interface. Set NRZE (CCR1.6) to a one for NRZ applications. In NRZ mode, data will be output on RPOS while a received error will cause a positive-going pulse synchronous with RCLK at RNEG. See section 8.4 for details.
RT0/ RT1	44/ 23	I	**Receive LIU Termination Select Bits 0 & 1 [H/W Mode].** These inputs determine the receive termination. See Table 4-8.
RTIP/ RRING	27/ 28	I	**Receive Tip and Ring.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the line. See Section 7 for details.
SCLK	5	I	**Serial Clock.** Serial bus clock input.
SCLKE	4	I	**Receive & Transmit Synchronization Clock Enable.** SCLKE combines RSCLKE (CCR5.3) and TSCLKE (CCR5.2). 0 = disable 2.048 MHz synchronization transmit and receive mode 1 = enable 2.048 MHz synchronization transmit and receive mode
SDI	6	I	**Serial Data Input.** Sampled on rising edge (ICES = 0) or the falling edge (ICES = 1) of SCLK.
SDO	7	O	**Serial Data Output.** Valid on the falling edge (OCES = 0) or the rising edge (OCES = 1) of SCLK.
TCLK	43	I	**Transmit Clock.** A 2.048 MHz or 1.544 MHz primary clock. Used to clock data through the transmit side formatter. Can be sourced internally by MCLK or RCLK. See Common Control Register 1 and Figure 3-3.
TEST	26	I	**3-State Control.** Set high to tri-state all outputs and I/O pins (including the parallel control port). Set low for normal operation. Useful in board level testing.
TNEG	42	I	**Transmit Negative Data.** Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.

Acronym	Pin	I/O	Description
TPD	13	I	**Transmit Power Down.** 0 = normal transmitter operation 1 = powers down the transmitter and tri-states the TTIP and TRING pins
TPOS	41	I	**Transmit Positive Data.** Sampled on the falling edge (CCR2.1 = 0) or the rising edge (CCR2.1 = 1) of TCLK for data to be transmitted out onto the line.
TTIP/ TRING	34/ 37	O	**Transmit Tip and Ring [TTIP & TRING].** Analog line driver outputs. These pins connect via a step-up transformer to the line. See Section 7 for details.
TX0/ TX1	14/ 15	I	**Transmit Data Source Select Bits 0 & 1 [H/W Mode].** These inputs determine the source of the transmit data. See Table 4-5.
VDD	21/ 36	-	**Positive Supply.** 5.0 volts +/-5% or 3.3 volts +/-5%.
VSM	20	I	**Voltage Supply Mode.** Determines 3.3V or 5V mode. Tie low for 3.3V operation and high for 5V operation.
VSS	22/ 35	-	**Signal Ground.**
WR* (R/W*)	3	I	**Write Input (Read/Write).** WR* is an active low signal. See the Bus Timing Diagrams in section 12.

NOTES:

1. Serial Port Mode pins are double underlined and Hardware Mode pins are single underlined.

2. G.703 requires an accuracy of +/-50 ppm for both T1 and E1. TR62411 and ANSI specs require an accuracy of +/- 32 ppm for T1 interfaces.

3. * Denotes active low.

Table 4-4 **LOOP BACK CONTROL IN HARDWARE MODE**

LOOPBACK	SYMBOL	CONTROL BIT	LOOP1	LOOP0
Remote Loop Back	RLB	CCR6.6	1	1
Local Loop Back	LLB	CCR6.7	1	0
Analog Loop Back	ALB	CCR6.4	0	1
No Loop Back	-	-	0	0

Table 4-5 **TRANSMIT DATA CONTROL IN HARDWARE MODE**

TRANSMIT DATA	SYMBOL	CONTROL BIT	TX1	TX0
Transmit Unframed All Ones	TUA1	CCR3.7	1	1
Transmit Alternating Ones and Zeros	TAOZ	CCR3.5	1	0
Transmit PRBS	TPRBSE	CCR3.4	0	1
TPOS and TNEG	-	-	0	0

Table 4-6 **RECEIVE SENSITIVITY SETTINGS**

EGL (CCR4.4)	ETS (CCR1.7)	RECEIVE SENSITIVITY
0	0 (E1)	-12 dB (short haul)
1	0 (E1)	-43 dB (long haul)
1	1 (T1)	-30 dB (limited long haul)
0	1 (T1)	-36 dB (long haul)

Table 4-7 **MONITOR GAIN SETTINGS**

MM1 (CCR5.5)	MM0 (CCR5.4)	INTERNAL LINEAR GAIN BOOST (dB)
0	0	Normal operation (no boost)
0	1	20
1	0	26
1	1	32

Table 4-8 **INTERNAL RX TERMINATION SELECT**

RT1 (CCR5.1)	RT0 (CCR5.0)	INTERNAL RECEIVE TERMINATION CONFIGURATION
0	0	Internal receive-side termination disabled
0	1	Internal receive-side 120Ω enabled
1	0	Internal receive-side 100Ω enabled
1	1	Internal receive-side 75Ω enabled

Table 4-9 **MCLK SELECTION**

MCLK	JAMUX (CCR1.3)	ETS (CCR1.7)
2.048 MHz	0	0
2.048 MHz	1	1
1.544 MHz	0	1

Figure 4-1 **PARALLEL PORT MODE PINOUT (BIS1 = 0, BIS0 = 1 or 0)**

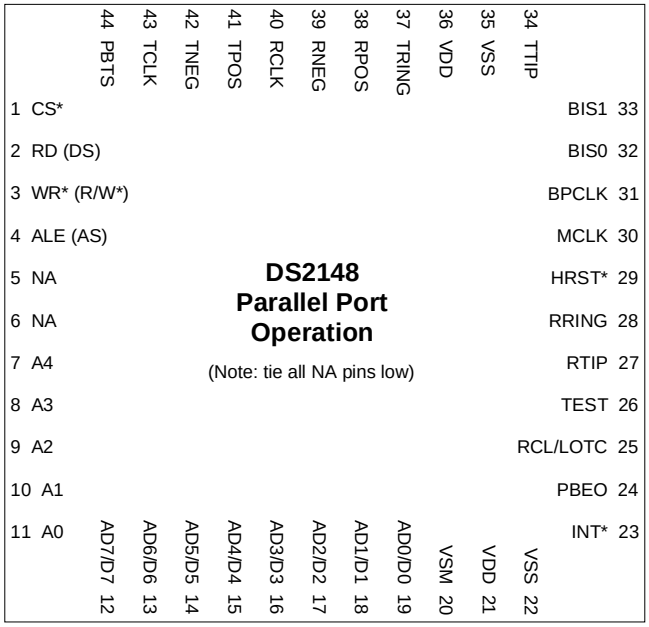


Figure 4-2 **SERIAL PORT MODE PINOUT (BIS1 = 1, BIS0 = 0)**

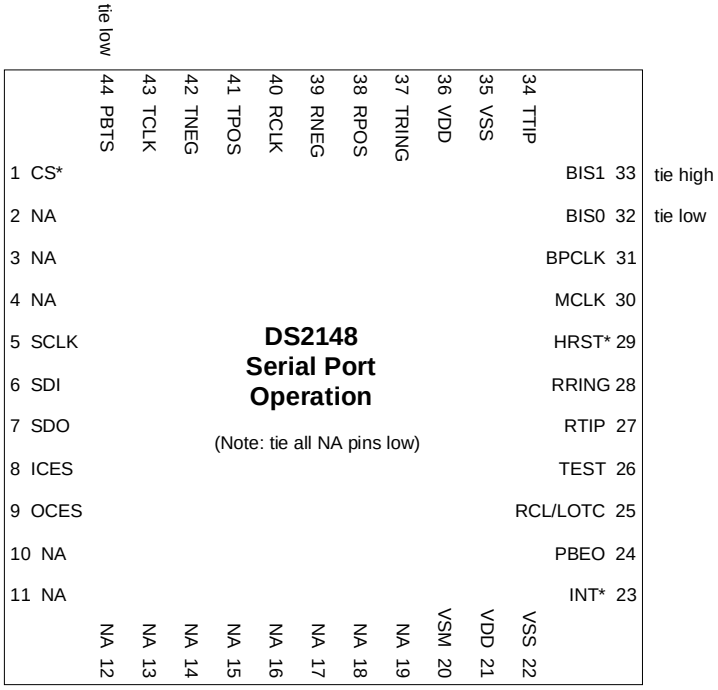
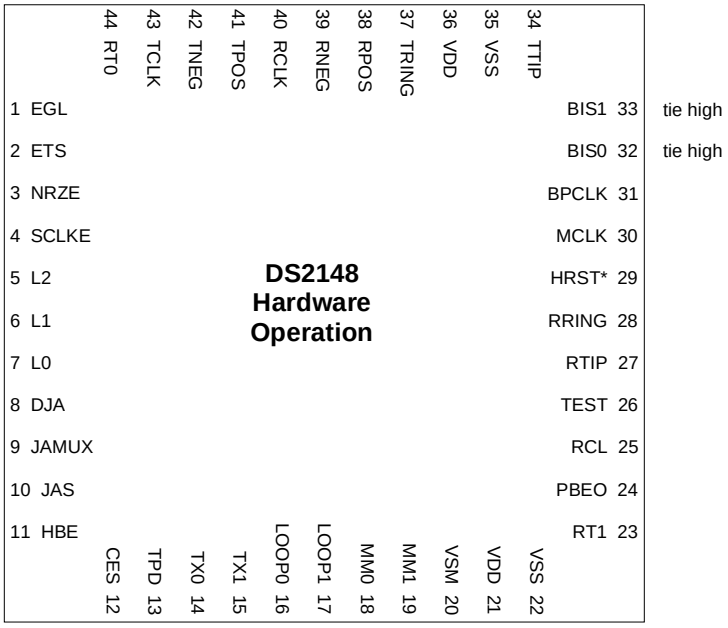


Figure 4-3 **HARDWARE MODE PINOUT (BIS1 = 1, BIS0 = 1)**



5. HARDWARE MODE

In hardware mode (BIS1 = 1, BIS0 = 1), pins 1-19, 23, 25, 31, and 44 are redefined to be used for initializing the DS2148. BPCLK (pin 31) defaults to a 16.384 MHz output when in hardware mode. The RCL/LOTC (pin 25) is designated to RCL when in hardware mode. JABDS (CCR4.2) defaults to logic 0. The RHBE (CCR2.3) and THBE (CCR2.2) control bits are combined and controlled by HBE at pin 11 while the RSCLKE (CCR5.3) and TSCLKE (CCR5.2) bits are combined and controlled by SCLKE at pin 4. TCES (CCR2.1) and RCES (CCR2.0) are combined and controlled by CES at pin 12. The transmitter functions are combined and controlled by TX1 (pin 15) and TX0 (pin 14). The loopback functions are controlled by LOOP1 (pin 17) and LOOP0 (pin 16). All other control bits default to the logic 0 setting.

5.1 Register Map

Table 5-1 **REGISTER MAP**

ACRONYM	REGISTER NAME	R/W	PARALLEL PORT MODE	SERIAL PORT MODE See notes 2 - 5 (msb) (lsb)
CCR1	Common Control Register 1	R/W	00h	B000 000R
CCR2	Common Control Register 2	R/W	01h	B000 001R
CCR3	Common Control Register 3	R/W	02h	B000 010R
CCR4	Common Control Register 4	R/W	03h	B000 011R
CCR5	Common Control Register 5	R/W	04h	B000 100R
CCR6	Common Control Register 6	R/W	05h	B000 101R
SR	Status Register	R	06h	B000 110R
IMR	Interrupt Mask Register	R/W	07h	B000 111R
RIR1	Receive Information Register 1	R	08h	B001 000R
RIR2	Receive Information Register 2	R	09h	B001 001R
IBCC	In-Band Code Control Register	R/W	0Ah	B001 010R
TCD1	Transmit Code Definition Register 1	R/W	0Bh	B001 011R
TCD2	Transmit Code Definition Register 2	R/W	0Ch	B001 100R
RUPCD1	Receive Up Code Definition Register 1	R/W	0Dh	B001 101R
RUPCD2	Receive Up Code Definition Register 2	R/W	0Eh	B001 110R
RDNCD1	Receive Down Code Definition Register 1	R/W	0Fh	B001 111R
RDNCD2	Receive Down Code Definition Register 2	R/W	10h	B010 000R
ECR1	Error Count Register 1	R	11h	B010 001R
ECR2	Error Count Register 2	R	12h	B010 010R
TEST1	Test 1	R/W	13h	B010 011R
TEST2	Test 2	R/W	14h	B010 100R
TEST2	Test 3	R/W	15h	B010 101R
-	-	-	See note 1	-

NOTES:

1. Register addresses 16h to 1Fh do not exist.
2. In the Serial Port Mode, the LSB is on the right hand side.
3. In the Serial Port Mode, data is read and written LSB first.
4. In the Serial Port Mode, the A bit (the LSB) determines whether the access is a read (R = 1) or a write (R = 0).
5. In the Serial Port Mode, the B bit (the MSB) determines whether the access is a burst access (B = 1) or a single register access (B = 0).

5.2 PARALLEL PORT OPERATION

When using the parallel interface on the DS2148 (BIS1 = 0) the user has the option for either multiplexed bus operation (BIS1 = 0, BIS0 = 0) or non-multiplexed bus operation (BIS1 = 0, BIS0 = 1). The DS2148 can operate with either Intel or Motorola bus timing configurations. If the PBTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parenthesis (). See the timing diagrams in Section 12 for more details.

5.3 SERIAL PORT OPERATION

Setting BIS1 = 1 and BIS0 = 0 enables the serial bus interface on the DS2148. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads or writes by the host. See Section 12 for the AC timing of the serial port. All serial port accesses are LSB first. See Figure 5-1, Figure 5-2, Figure 5-3, and Figure 5-4 for more details.

Reading or writing to the internal registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command byte specifies whether the access is a read (1) or a write (0). The next 5 bits identify the register address. Bit 7 is reserved and must be set to 0 for proper operation.

The last bit (MSB) of the address/command byte is the burst mode bit. When the burst bit is enabled (set to 0) and a READ operation is performed, addresses 0 through 16h are read sequentially, starting at address 0h. And when the burst bit is enabled and a WRITE operation is performed, addresses 0 through 16h are written sequentially, starting at address 0h. Burst operation is stopped once address 16h is read. See Figure 5-5 and Figure 5-6 for more details.

All data transfers are initiated by driving the CS* input low. When Input Clock-Edge Select (ICES) is low, input data is latched on the rising edge of SCLK and when ICES is high, input data is latched on the falling edge of SCLK. When Output Clock-Edge Select (OCES) is low, data is output on the falling edge of SCLK and when OCES is high, data is output on the rising edge of SCLK. Data is held until the next falling or rising edge. All data transfers are terminated if the CS* input transitions high. Port control logic is disabled and SDO is tri-stated when CS* is high.

Figure 5-1 **SERIAL PORT OPERATION FOR READ ACCESS (R=1) MODE 1**

ICES = 1 (sample SDI on the falling edge of SCLK)
OCES = 1 (update SDO on rising edge of SCLK)

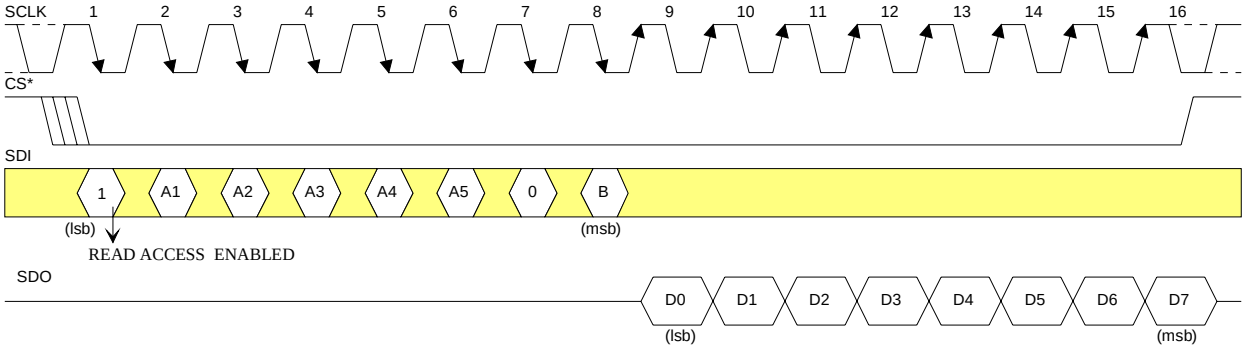


Figure 5-2 **SERIAL PORT OPERATION FOR READ ACCESS MODE 2**

ICES = 1 (sample SDI on the falling edge of SCLK)
OCES = 0 (update SDO on falling edge of SCLK)

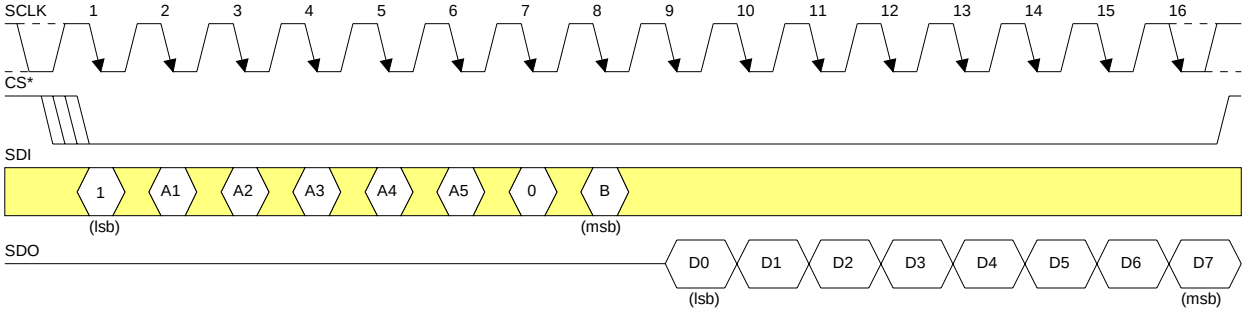


Figure 5-3 **SERIAL PORT OPERATION FOR READ ACCESS MODE 3**

ICES = 0 (sample SDI on the rising edge of SCLK)
OCES = 0 (update SDO on falling edge of SCLK)

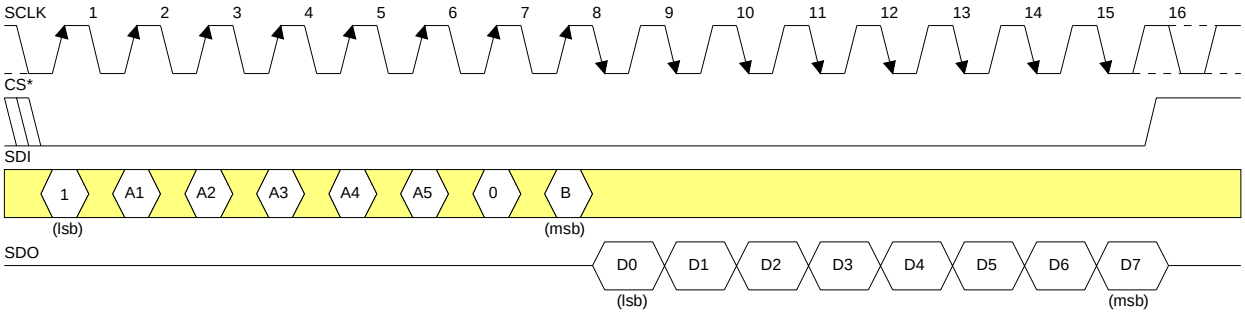


Figure 5-4 **SERIAL PORT OPERATION FOR READ ACCESS MODE 4**

ICES = 0 (sample SDI on the rising edge of SCLK)
OCES = 1 (update SDO on rising edge of SCLK)

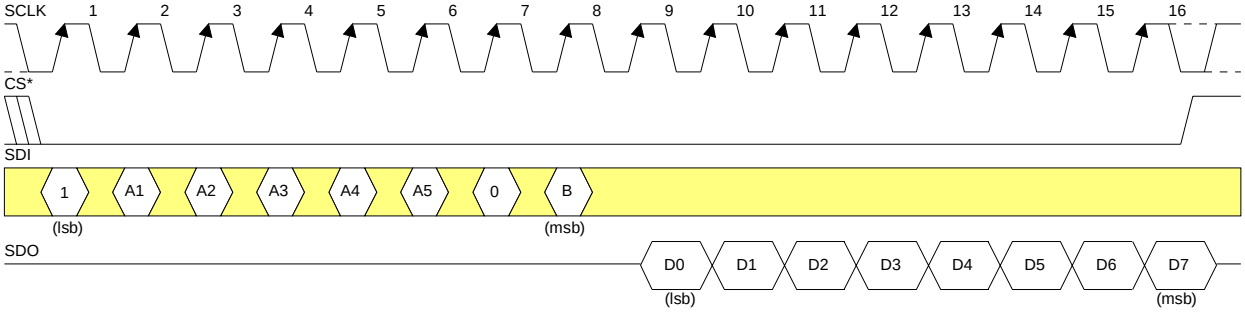
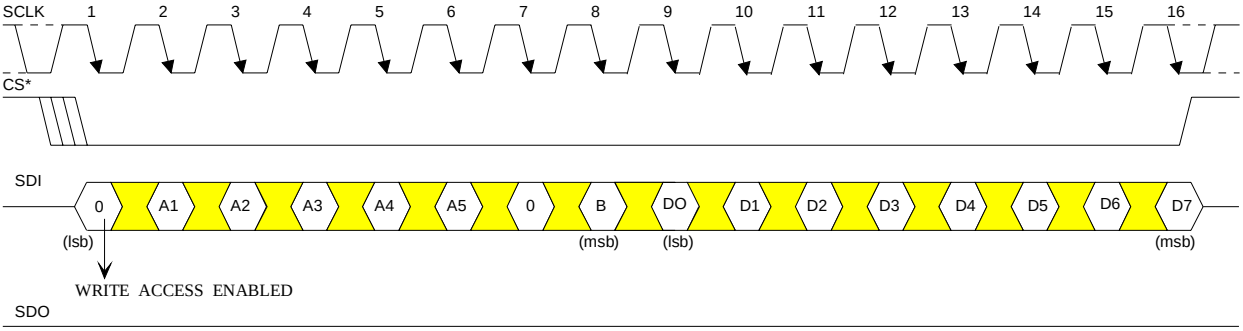


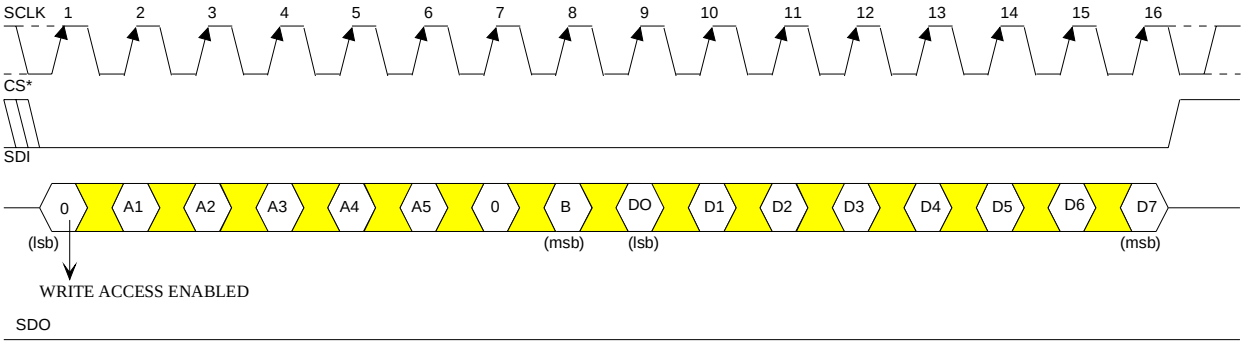
Figure 5-5 **SERIAL PORT OPERATION FOR WRITE ACCESS (R=0) MODES 1 & 2**



ICES = 1 (sample SDI on the falling edge of SCLK)

Figure 5-6 **SERIAL PORT OPERATION FOR WRITE ACCESS (R=0) MODES 3 & 4**

ICES = 0 (sample SDI on the rising edge of SCLK)



6. CONTROL REGISTERS

CCR1 (00H): COMMON CONTROL REGISTER 1

(MSB)							(LSB)
ETS	NRZE	RCLA	ECUE	JAMUX	TTOJ	TTOR	LOTCMC

SYMBOL	POSITION	NAME AND DESCRIPTION
ETS	CCR1.7	**E1/T1 Select.** 0 = E1 1 = T1
NRZE	CCR1.6	**NRZ Enable.** 0 = Bipolar data at RPOS/RNEG and TPOS/TNEG 1 = NRZ data at RPOS and TPOS or TNEG; RNEG outputs a positive going pulse when device receives a BPV, CV, or EXZ.
RCLA	CCR1.5	**Receive Carrier Loss Alternate Criteria.** 0 = RCL declared upon 255 (E1) or 192 (T1) consecutive zeros 1 = RCL declared upon 2048 (E1) or 1544 (T1) consecutive zeros
ECUE	CCR1.4	**Error Counter Update Enable.** A 0 to 1-transition forces the next clock cycle to load the error counter registers with the latest counts and reset the counters. The user must wait a minimum of two clocks cycles (976ns for E1 and 1296ns for T1) before reading the error count registers to allow for a proper update. See Section 6 for details.
JAMUX	CCR1.3	**Jitter Attenuator MUX.** Controls the source for JACLK. See **Figure 3-1**. 0 = JACLK sourced from MCLK (2.048 MHz or 1.544 MHz at MCLK) 1 = JACLK sourced from internal PLL (2.048 MHz at MCLK)
TTOJ	CCR1.2	**TCLK to JACLK.** Internally connects TCLK to JACLK. See Figure **3-3**. 0 = disabled 1 = enabled
TTOR	CCR1.1	**TCLK to RCLK.** Internally connects TCLK to RCLK**.** See Figure **3-3** 0 = disabled 1 = enabled
LOTCMC	CCR1.0	**Loss Of Transmit Clock Mux Control.** Determines whether the transmit logic should switch to JACLK if the TCLK input should fail to transition. See Figure 3-3. 0 = do not switch to JACLK if TCLK stops 1 = switch to JACLK if TCLK stops

Table 6-1 **MCLK SELECTION**

MCLK	JAMUX (CCR1.3)	ETS (CCR1.7)
2.048 MHz	0	0
2.048 MHz	1	1
1.544 MHz	0	1

CCR2 (01H): COMMON CONTROL REGISTER 2

(MSB) **(LSB)**

P25S	n/a	SCLD	CLDS	RHBE	THBE	TCES	RCES

SYMBOL	POSITION	NAME AND DESCRIPTION
P25S	CCR2.7	**Pin 25 Select.** Forced to logic 0 in hardware mode. 0 = toggles high during a Receive Carrier Loss condition 1 = toggles high if TCLK does not transition for at least 5 µs
-	CCR2.6	**Not Assigned. Should be set to zero when written to.**
SCLD	CCR2.5	**Short Circuit Limit Disable (ETS = 0).** Controls the 50 mA (rms) current limiter. 0 = enable 50 mA current limiter **1 = disable 50 mA current limiter**
CLDS	CCR2.4	**Custom Line Driver Select.** Setting this bit to a one will redefine the operation of the transmit line driver. When this bit is set to a one and CCR4.5 = CCR4.6 = CCR4.7 = 0, then the device will generate a square wave at the TTIP and TRING outputs instead of a normal waveform. When this bit is set to a one and CCR4.5 = CCR4.6 = CCR4.7 ≠ 0, then the device will force TTIP and TRING outputs to become open drain drivers instead of their normal push-pull operation. **This bit should be set to zero for normal operation of the device.** Contact the factory for more details on how to use this bit.
RHBE	CCR2.3	**Receive HDB3/B8ZS Enable.** 0 = enable HDB3 (E1) / B8ZS (T1) 1 = disable HDB3 (E1) / B8ZS (T1)
THBE	CCR2.2	**Transmit HDB3/B8ZS Enable.** 0 = enable HDB3 (E1) / B8ZS (T1) 1 = disable HDB3 (E1) / B8ZS (T1)
TCES	CCR2.1	**Transmit Clock Edge Select.** Selects which TCLK edge to sample TPOS and TNEG. 0 = sample TPOS and TNEG on falling edge of TCLK 1 = sample TPOS and TNEG on rising edge of TCLK
RCES	CCR2.0	**Receive Clock Edge Select.** Selects which RCLK edge to update RPOS and RNEG. 0 = update RPOS and RNEG on rising edge of RCLK 1 = update RPOS and RNEG on falling edge of RCLK

CCR3 (02H): COMMON CONTROL REGISTER 3

(MSB)							(LSB)
TUA1	ATUA1	TAOZ	TPRBSE	TLCE	LIRST	IBPV	IBE

SYMBOL	POSITION	NAME AND DESCRIPTION
TUA1	CCR3.7	**Transmit Unframed All Ones.** The polarity of this bit is set such that the device will transmit an all ones pattern on power-up or device reset. This bit must be set to a one to allow the device to transmit data. The transmission of this data pattern is always timed off of the JACLK (see **Figure 3-1**). 0 = transmit all ones at TTIP and TRING 1 = transmit data normally
ATUA1	CCR3.6	**Automatic Transmit Unframed All Ones.** Automatically transmit an unframed all ones pattern at TTIP and TRING during a receive carrier loss (RCL) condition. 0 = disabled 1 = enabled
TAOZ	CCR3.5	**Transmit Alternate Ones and Zeros.** Transmit a …101010… pattern at TTIP and TRING. The transmission of this data pattern is always timed off of TCLK (see **Figure 3-1**). 0 = disabled 1 = enabled
TPRBSE	CCR3.4	**Transmit PRBS Enable.** Transmit a 2^{15} –1 (E1) or a 2^{20}-1 (T1) PRBS at TTIP and TRING. 0 = disabled 1 = enabled
TLCE	CCR3.3	**Transmit Loop Code Enable.** Enables the transmit side to transmit the loop up code in the Transmit Code Definition registers (TCD1 and TCD2). See Section 6 for details. 0 = disabled **1 = enabled**
LIRST	CCR3.2	**Line Interface Reset.** Setting this bit from a zero to a one will initiate an internal reset that resets the clock recovery state machine and recenters the jitter attenuator. Normally this bit is only toggled on power-up. Must be cleared and set again for a subsequent reset.
IBPV	CCR3.1	**Insert BPV.** A 0 to 1 transition on this bit will cause a single BiPolar Violation (BPV) to be inserted into the transmit data stream. Once this bit has been toggled from a 0 to a 1, the device waits for the next occurrence of three consecutive ones to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted. See Figure 3-3.
IBE	CCR3.0	**Insert Bit Error.** A 0 to 1 transition on this bit will cause a single logic error to be inserted into the transmit data stream. This bit must be cleared and set again for a subsequent error to be inserted. See Figure 3-3.

6.1 DEVICE POWER-UP & RESET

The DS2148 will reset itself upon power-up setting all writeable registers to 00h and clear the status and information registers. CCR3.7 (TUA1) = 0 results in the LIU transmitting unframed all ones. After the power supplies have settled following power-up, initialize all control registers to the desired settings, then toggle the LIRST bit (CCR3.2). At anytime, the DS2148 can be reset to the default settings by bringing HRST* (pin 29) low (level triggered) or by powering down and powering up again.

CCR4 (03H): COMMON CONTROL REGISTER 4

(MSB)							(LSB)
L2	L1	L0	EGL	JAS	JABDS	DJA	TPD

SYMBOL	POSITION	NAME AND DESCRIPTION
L2	CCR4.7	**Line Build Out Select Bit 2.** Sets the transmitter build out; see Table 9-1 for E1 and Table 9-2 for T1.
L1	CCR4.6	**Line Build Out Select Bit 1.** Sets the transmitter build out; see Table 9-1 for E1 and Table 9-2 for T1.
L0	CCR4.5	**Line Build Out Select Bit 0.** Sets the transmitter build out; see Table 9-1 for E1 and Table 9-2 for T1.
EGL	CCR4.4	**Receive Equalizer Gain Limit.** This bit controls the sensitivity of the receive equalizer. See Table 6-2.
JAS	CCR4.3	**Jitter Attenuator Select.** 0 = place the jitter attenuator on the receive side 1 = place the jitter attenuator on the transmit side
JABDS	CCR4.2	**Jitter Attenuator Buffer Depth Select.** 0 = 128 bits 1 = 32 bits (use for delay sensitive applications)
DJA	CCR4.1	**Disable Jitter Attenuator.** 0 = jitter attenuator enabled 1 = jitter attenuator disabled
TPD	CCR4.0	**Transmit Power Down.** 0 = normal transmitter operation 1 = powers down the transmitter and tri-states the TTIP and TRING pins

Table 6-2 **RECEIVE SENSITIVITY SETTINGS**

EGL (CCR4.4)	ETS (CCR1.7)	RECEIVE SENSITIVITY
0	0 (E1)	-12 dB (short haul)
1	0 (E1)	-43 dB (long haul)
1	1 (T1)	-30 dB (limited long haul)
0	1 (T1)	-36 dB (long haul)

CCR5 (04H): COMMON CONTROL REGISTER 5

(MSB)							(LSB)
BPCS1	BPCS0	MM1	MM0	RSCLKE	TSCLKE	RT1	RT0

SYMBOL	POSITION	NAME AND DESCRIPTION
BPCS1	CCR5.7	**Back Plane Clock Select 1.** See Table 6-3 for details.
BPCS0	CCR5.6	**Back Plane Clock Select 0.** See Table 6-3 for details
MM1	CCR5.5	**Monitor Mode 1.** See Table 6-4.
MM0	CCR5.4	**Monitor Mode 0.** See Table 6-4.
RSCLKE	CCR5.3	**Receive Synchronization Clock Enable.** 0 = disable 2.048 MHz synchronization receive mode 1 = enable 2.048 MHz synchronization receive mode
TSCLKE	CCR5.2	**Transmit Synchronization Clock Enable.** 0 = disable 2.048 MHz transmit synchronization clock 1 = enable 2.048 MHz transmit synchronization clock
RT1	CCR5.1	**Receive Termination 1.** See Table 6-5 for details.
RT0	CCR5.0	**Receive Termination 0**. See Table 6-5 for details.

Table 6-3 **BACK PLANE CLOCK SELECT**

BPCS1 (CCR5.7)	BPCS0 (CCR5.6)	BPCLK FREQUENCY
0	0	16.384 MHz
0	1	8.192 MHz
1	0	4.096 MHz
1	1	2.048 MHz

Table 6-4 **MONITOR GAIN SETTINGS**

MM1 (CCR5.5)	MM0 (CCR5.4)	INTERNAL LINEAR GAIN BOOST (dB)
0	0	Normal operation (no boost)
0	1	20
1	0	26
1	1	32

Table 6-5 **INTERNAL RX TERMINATION SELECT**

RT1 (CCR5.1)	RT0 (CCR5.0)	INTERNAL RECEIVE TERMINATION CONFIGURATION
0	0	Internal receive-side termination disabled
0	1	Internal receive-side 120Ω enabled
1	0	Internal receive-side 100Ω enabled
1	1	Internal receive-side 75Ω enabled

CCR6 (05H): COMMON CONTROL REGISTER 6

(MSB)							(LSB)
LLB	RLB	ARLBE	ALB	RJAB	ECRS2	ECRS1	ECRS0

SYMBOL	POSITION	NAME AND DESCRIPTION
LLB	CCR6.7	**Local LoopBack.** In Local Loopback (LLB), transmit data will be looped back to the receive path passing through the jitter attenuator if it is enabled. Data in the transmit path will act as normal. See Figure 3-1 for details. **0 = loopback disabled** 1 = loopback enabled
RLB	CCR6.6	**Remote LoopBack.** In Remote Loopback (RLB), data output from the clock/data recovery circuitry will be looped back to the transmit path passing through the jitter attenuator if it is enabled. Data in the receive path will act as normal while data presented at TPOS and TNEG will be ignored. See Figure 3-1for details. **0 = loopback disabled** 1 = loopback enabled
ARLBE	CCR6.5	**Automatic Remote LoopBack Enable & Reset.** When this bit is set high, the device will automatically go into remote loopback when it detects loop up code programmed into the Receive Loop Up Code Definition Registers (RUPCD1 and RUPCD2) for a minimum of 5 seconds and it will also set the RIR2.1 status bit. Once in a RLB state, it will remain in this state until it has detected the loop code programmed into the Receive Loop Down Code Definition Registers (RDNCD1 and RDNCD2) for a minimum of 5 seconds at which point it will force the device out of RLB and clear RIR2.1. The automatic RLB circuitry can be reset by toggling this bit from a 1 to a 0. The action of the automatic remote loopback circuitry is logically OR'ed with the RLB (CCR6.6) control bit (i.e. either one can cause a RLB to occur).
ALB	CCR6.4	**Analog LoopBack.** In Analog Loopback (ALB), signals at TTIP and TRING will be internally connected to RTIP and RRING. The incoming signals, from the line, at RTIP and RRING will be ignored. The signals at TTIP and TRING will be transmitted as normal. See Figure 3-1for more details. **0 = loopback disabled** 1 = loopback enabled

SYMBOL	POSITION	NAME AND DESCRIPTION
RJAB	CCR6.3	**RCLK Jitter Attenuator Bypass.** This control bit allows the receive recovered clock and data to bypass the jitter attenuation while still allowing the BPCLK output to use the jitter attenuator. See Figure 3-1 for details. 0 = disabled 1 = enabled
ECRS2	CCR6.2	**Error Count Register Select 2.** See Section 8.4 for details.
ECRS1	CCR6.1	**Error Count Register Select 1.** See Section 8.4 for details.
ECRS0	CCR6.0	**Error Count Register Select 0.** See Section 8.4 for details.

7. STATUS REGISTERS

There are three registers that contain information on the current real time status of the device, Status Register (SR) and Receive Information Registers 1 & 2 (RIR1/RIR2). When a particular event has occurred (or is occurring), the appropriate bit in one of these three registers will be set to a one. Some of the bits in SR, RIR1, and RIR2 are latched bits and some are real time bits. The register descriptions below list which status bits are latched and which are real time bits. For latched status bits, when an event or an alarm occurs the bit is set to a one and will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again. Two of the latched status bits (RUA1 & RCL) will remain set after reading if the alarm is still present.

The user will always precede a read of any of the three status registers with a write. The byte written to the register will inform the DS2148 which bits the user wishes to read and have cleared. The user will write a byte to one of these registers with a one in the bit positions to be read and a zero in the other bit positions. When a one is written to a bit location, that location will be updated with the latest information. When a zero is written to a bit position, that bit position will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously with respect to their access via the parallel port. This write–read– write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS2148 with higher–order software languages.

The bits in the SR register have the unique ability to initiate a hardware interrupt via the INT* output pin. Each of the alarms and events in the SR can be either masked or unmasked from the interrupt pin via the Interrupt Mask Register (IMR). The interrupts caused by the RCL, RUA1 and LOTC bits in SR act differently than the interrupts caused by the other status bits in SR. The RCL, RUA1 and LOTC bits will force the INT* pin low whenever they change state (i.e. go active or inactive). The INT* pin will be allowed to return high (if no other interrupts are present) when the user reads the alarm bit that caused the interrupt to occur even if the alarm is still present. The other status bits in SR can force the INT* pin low when they are set. The INT* pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

Table 7-1 **RECEIVED ALARM CRITERIA**

ALARM	E1/T1	SET CRITERIA	CLEAR CRITERIA
RUA1	E1	Less than 2 zeros in 2 frames (512 bits)	More than 2 zeros in 2 frames (512 bits)
RUA1	T1	Over a 3 ms window, 5 or less zeros are received	Over a 3 ms window, 6 or more zeros are received
RCL[1]	E1	255 (or 2048)[2] consecutive zeros received (G.775)	In 255 bit times, at least 32 ones are received
RCL[1]	T1	192 (or 1544)[2] consecutive zeros are received	14 or more ones out of 112 possible bit positions are received starting with the first one received

Note 1: Receive carrier loss (RCL) is also known as loss of signal (LOS) or Red Alarm in T1.
Note 2: See CCR1.5 for details.

SR (06H): STATUS REGISTER

(MSB)							(LSB)
LUP	LDN	LOTC	RUA1	RCL	TCLE	TOCD	PRBSD

SYMBOL	POSITION	NAME AND DESCRIPTION
LUP (latched)	SR.7	**Loop Up Code Detected.** Set when the loop up code defined in registers RUPCD1 and RUPCD2 is being received. See Section 6 for details.
LDN (latched)	SR.6	**Loop Down Code Detected.** Set when the loop down code defined in registers RDNCD1 and RDNCD2 is being received. See Section 6 for details.
LOTC (real time)	SR.5	**Loss of Transmit Clock.** Set when the TCLK pin has not transitioned for 5µsec (±2µsec). Will force the LOTC pin high.
RUA1 (latched)	SR.4	**Receive Unframed All Ones.** Set when an unframed all ones code is received at RRING and RTIP. See Table 7-1for details.
RCL (latched)	SR.3	**Receive Carrier Loss.** Set when a receive carrier loss condition exists at RRING and RTIP. See Table 7-1for details.
TCLE (real time)	SR.2	**Transmit Current Limit Exceeded.** Set when the 50 mA (rms) current limiter is activated whether the current limiter is enabled or not.
TOCD (real time)	SR.1	**Transmit Open Circuit Detect.** Set when the device detects that the TTIP and TRING outputs are open circuited.
PRBSD (real time)	SR.0	**PRBS Detect.** Set when the receive-side detects a 2^{15}-1 (E1) or a 2^{20}-1 (T1) Pseudo Random Bit Sequence (PRBS).

IMR (07H): INTERRUPT MASK REGISTER

(MSB)							(LSB)
LUP	LDN	LOTC	RUA1	RCL	TCLE	TOCD	PRBSD

SYMBOL	POSITION	NAME AND DESCRIPTION
LUP	IMR.7	**Loop Up Code Detected.** 0 = interrupt masked 1 = interrupt enabled
LDN	IMR.6	**Loop Down Code Detected.** 0 = interrupt masked 1 = interrupt enabled
LOTC	IMR.5	**Loss of Transmit Clock.** 0 = interrupt masked 1 = interrupt enabled
RUA1	IMR.4	**Receive Unframed All Ones.** 0 = interrupt masked 1 = interrupt enabled
RCL	IMR.3	**Receive Carrier Loss.** 0 = interrupt masked 1 = interrupt enabled
TCLE	IMR.2	**Transmit Current Limiter Exceeded.** 0 = interrupt masked 1 = interrupt enabled
TOCD	IMR.1	**Transmit Open Circuit Detect.** 0 = interrupt masked 1 = interrupt enabled
PRBSD	IMR.0	**PRBS Detection.** 0 = interrupt masked 1 = interrupt enabled

RIR1 (08H): RECEIVE INFORMATION REGISTER 1

(MSB)							(LSB)
ZD	16ZD	HBD	RCLC	RUA1C	JALT	n/a	n/a

SYMBOL	POSITION	NAME AND DESCRIPTION
ZD (latched)	RIR1.7	**Zero Detect.** Set when a string of at least four (ETS = 0) or eight (ETS = 1) consecutive zeros (regardless of the length of the string) have been received. Will be cleared when read.
16ZD (latched)	RIR1.6	**Sixteen Zero Detect.** Set when at least sixteen consecutive zeros (regardless of the length of the string) have been received. Will be cleared when read.
HBD (latched)	RIR1.5	**HDB3/B8ZS Word Detect.** Set when an HDB3 (ETS = 0) or B8ZS (ETS = 1) code word is detected independent of whether the receive HDB3/B8ZS mode (CCR4.6) is enabled. Will be cleared when read. Useful for automatically setting the line coding.
RCLC (latched)	RIR1.4	**Receive Carrier Loss Clear.** Set when the RCL alarm has met the clear criteria defined in Table 7-1. Will be cleared when read.
RUA1C (latched)	RIR1.3	**Receive Unframed All Ones Clear.** Set when the unframed all ones signal is no longer detected. Will be cleared when read. See Table 7-1.
JALT (latched)	RIR1.2	**Jitter Attenuator Limit Trip.** Set when the jitter attenuator FIFO reaches to within 4 bits of its useful limit. Will be cleared when read. Useful for debugging jitter attenuation operation.
n/a	RIR1.1	**Not Assigned.** Could be any value when read.
n/a	RIR1.0	**Not Assigned.** Could be any value when read.

RIR2 (09H): RECEIVE INFORMAION REGISTER 2

(MSB)							(LSB)
RL3	RL2	RL1	RL0	n/a	n/a	ARLB	SEC

SYMBOL	POSITION	NAME AND DESCRIPTION
RL3 (real time)	RIR2.7	**Receive Level Bit 3.** See Table 7-2.
RL2 (real time)	RIR2.6	**Receive Level Bit 2.** See Table 7-2.
RL1 (real time)	RIR2.5	**Receive Level Bit 1.** See Table 7-2.
RL0 (real time)	RIR2.4	**Receive Level Bit 0.** See Table 7-2.
n/a	RIR2.3	**Not Assigned.** Could be any value when read.
n/a	RIR2.2	**Not Assigned.** Could be any value when read.
ARLB (real time)	RIR2.1	**Automatic Remote LoopBack Detected.** This bit will be set to a one when the automatic Remote Loopback (RLB) circuitry has detected the presence of a loop up code for 5 seconds. It will remain set until the automatic RLB circuitry has detected the loop down code for 5 seconds. See Section 6 for more details. This bit will be forced low when the automatic RLB circuitry is disabled (CCR6.5 = 0).
SEC (latched)	RIR2.0	**One Second Timer.** This bit will be set to a one on one-second boundaries as timed by the device based on the RCLK. It will be cleared when read.

Table 7-2 **RECEIVE LEVEL INDICATION**

RL3	RL2	RL1	RL0	Receive Level (dB)
0	0	0	0	Greater than -2.5
0	0	0	1	-2.5 to –5.0
0	0	1	0	-5.0 to –7.5
0	0	1	1	-7.5 to –10.0
0	1	0	0	-10.0 to –12.5
0	1	0	1	-12.5 to –15.0
0	1	1	0	-15.0 to –17.5
0	1	1	1	-20.0 to –22.5
1	0	0	0	-22.5 to –25.0
1	0	0	1	-25.0 to –27.5
1	0	1	0	-27.5 to –30.0
1	0	1	1	-30.0 to –32.5
1	1	0	0	-32.5 to –35.0
1	1	0	1	-35.0 to –37.5
1	1	1	0	-37.5 to –40.0
1	1	1	1	-40.0 to –42.5

8. DIAGNOSTICS

8.1 IN-BAND LOOP CODE GENERATION & DETECTION

The DS2148 has the ability to generate and detect a repeating bit pattern that is from one to eight or sixteen bits in length. To transmit a pattern, the user will load the pattern to be sent into the Transmit Code Definition (TCD1 and TCD2) registers and select the proper length of the pattern by setting the TC0 and TC1 bits in the In-Band Code Control (IBCC) register. When generating a 1, 2, 4, 8, or 16 bit pattern both the transmit code registers (TCD1 and TCD2) must be filled with the proper code. Generation of a 1, 3, 5, or 7-bit pattern only requires TCD1 to be filled. Once this is accomplished, the pattern will be transmitted as long as the TLCE control bit (CCR3.3) is enabled. As an example, if the user wished to transmit the standard "loop up" code for Channel Service Units which is a repeating pattern of ...10000100001... then 80h would be loaded into TCD1 and the length would set using TC1 and TC0 in the IBCC register to 5 bits.

The DS2148 can detect two separate repeating patterns to allow for both a "loop up" code and a "loop down" code to be detected. The user will program the codes to be detected in the Receive Up Code Definition (RUPCD1 and RUPCD2) registers and the Receive Down Code Definition (RDNCD1 and RDNCD2) registers and the length of each pattern will be selected via the IBCC register. The DS2148 will detect repeating pattern codes with bit error rates as high as $1x10^{-2}$. The code detector has a nominal integration period of 48 ms, hence, after about 48 ms of receiving either code, the proper status bit (LUP at SR.7 and LDN at SR.6) will be set to a one. Normally codes are sent for a period of 5 seconds. It is recommended that the software poll the DS2148 every 100 ms to 1000 ms until 5 seconds has elapsed to insure that the code is continuously present.

IBCC (0AH): IN–BAND CODE CONTROL REGISTER

(MSB)							(LSB)
TC1	TC0	RUP2	RUP1	RUP0	RDN2	RDN1	RDN0

SYMBOL	POSITION	NAME AND DESCRIPTION
TC1	IBCC.7	**Transmit Code Length Definition Bit 1.** See Table 8-1
TC0	IBCC.6	**Transmit Code Length Definition Bit 0.** See Table 8-1
RUP2	IBCC.5	**Receive Up Code Length Definition Bit 2.** See Table 8-2
RUP1	IBCC.4	**Receive Up Code Length Definition Bit 1.** See Table 8-2
RUP0	IBCC.3	**Receive Up Code Length Definition Bit 0.** See Table 8-2
RDN2	IBCC.2	**Receive Down Code Length Definition Bit 2.** See Table 8-2
RDN1	IBCC.1	**Receive Down Code Length Definition Bit 1.** See Table 8-2
RDN0	IBCC.0	**Receive Down Code Length Definition Bit 0.** See Table 8-2

Table 8-1 **TRANSMIT CODE LENGTH**

TC1	TC0	LENGTH SELECTED
0	0	5 bits
0	1	6 bits / 3 bits
1	0	7 bits
1	1	16 bits / 8 bits / 4 bits / 2 bits / 1 bits

Table 8-2 **RECEIVE CODE LENGTH**

RUP2/ RDN2	RUP1/ RDN1	RUP0/ RDN0	LENGTH SELECTED
0	0	0	1 bits
0	0	1	2 bits
0	1	0	3 bits
0	1	1	4 bits
1	0	0	5 bits
1	0	1	6 bits
1	1	0	7 bits
1	1	1	16 bits / 8 bits

TCD1 (0BH): TRANSMIT CODE DEFINITION REGISTER 1

(MSB) **(LSB)**

C7	C6	C5	C4	C3	C2	C1	C0

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	TCD1.7	**Transmit Code Definition Bit 7.** First bit of the repeating pattern.
C6	TCD1.6	**Transmit Code Definition Bit 6.**
C5	TCD1.5	**Transmit Code Definition Bit 5.**
C4	TCD1.4	**Transmit Code Definition Bit 4.**
C3	TCD1.3	**Transmit Code Definition Bit 3.**
C2	TCD1.2	**Transmit Code Definition Bit 2.** A Don't Care if a 5-bit length is selected.
C1	TCD1.1	**Transmit Code Definition Bit 1.** A Don't Care if a 5 or 6 bit length is selected.
C0	TCD1.0	**Transmit Code Definition Bit 0.** A Don't Care if a 5, 6 or 7 bit length is selected.

TCD2 (0CH): TRANSMIT CODE DEFINITION REGISTER 2

(MSB)							(LSB)
C15	C14	C13	C12	C11	C10	C9	C8

SYMBOL	POSITION	NAME AND DESCRIPTION
C15	TCD2.7	**Transmit Code Definition Bit 15**
C14	TCD2.6	**Transmit Code Definition Bit 14**
C13	TCD2.5	**Transmit Code Definition Bit 13**
C12	TCD2.4	**Transmit Code Definition Bit 12**
C11	TCD2.3	**Transmit Code Definition Bit 11**
C10	TCD2.2	**Transmit Code Definition Bit 10**
C9	TCD2.1	**Transmit Code Definition Bit 9**
C8	TCD2.0	**Transmit Code Definition Bit 8**

RUPCD1 (0DH): RECEIVE UP CODE DEFINITION REGISTER 1

(MSB)							(LSB)
C7	C6	C5	C4	C3	C2	C1	C0

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	RUPCD1.7	**Receive Up Code Definition Bit 7.** First bit of the repeating pattern.
C6	RUPCD1.6	**Receive Up Code Definition Bit 6.** A Don't Care if a 1-bit length is selected.
C5	RUPCD1.5	**Receive Up Code Definition Bit 5.** A Don't Care if a 1 or 2 bit length is selected.
C4	RUPCD1.4	**Receive Up Code Definition Bit 4.** A Don't Care if a 1 to 3 bit length is selected.
C3	RUPCD1.3	**Receive Up Code Definition Bit 3.** A Don't Care if a 1 to 4 bit length is selected.
C2	RUPCD1.2	**Receive Up Code Definition Bit 2.** A Don't Care if a 1 to 5 bit length is selected.
C1	RUPCD1.1	**Receive Up Code Definition Bit 1.** A Don't Care if a 1 to 6 bit length is selected.
C0	RUPCD1.0	**Receive Up Code Definition Bit 0.** A Don't Care if a 1 to 7 bit length is selected.

RUPCD2 (0EH): RECEIVE UP CODE DEFINITION REGISTER 2

(MSB)							(LSB)
C15	C14	C13	C12	C11	C10	C9	C8

SYMBOL	POSITION	NAME AND DESCRIPTION
C15	RUPCD2.7	**Receive Up Code Definition Bit 15**
C14	RUPCD2.6	**Receive Up Code Definition Bit 14**
C13	RUPCD2.5	**Receive Up Code Definition Bit 13**
C12	RUPCD2.4	**Receive Up Code Definition Bit 12**
C11	RUPCD2.3	**Receive Up Code Definition Bit 11**
C10	RUPCD2.2	**Receive Up Code Definition Bit 10**
C9	RUPCD2.1	**Receive Up Code Definition Bit 9**
C8	RUPCD2.0	**Receive Up Code Definition Bit 8**

RDNCD1 (0FH): RECEIVE DOWN CODE DEFINITION REGISTER 1

(MSB)							(LSB)
C7	C6	C5	C4	C3	C2	C1	C0

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	RDNCD1.7	**Receive Down Code Definition Bit 7.** First bit of the repeating pattern.
C6	RDNCD1.6	**Receive Down Code Definition Bit 6.** A Don't Care if a 1-bit length is selected.
C5	RDNCD1.5	**Receive Down Code Definition Bit 5.** A Don't Care if a 1 or 2 bit length is selected.
C4	RDNCD1.4	**Receive Down Code Definition Bit 4.** A Don't Care if a 1 to 3 bit length is selected.
C3	RDNCD1.3	**Receive Down Code Definition Bit 3.** A Don't Care if a 1 to 4 bit length is selected.
C2	RDNCD1.2	**Receive Down Code Definition Bit 2.** A Don't Care if a 1 to 5 bit length is selected.
C1	RDNCD1.1	**Receive Down Code Definition Bit 1.** A Don't Care if a 1 to 6 bit length is selected.
C0	RDNCD1.0	**Receive Down Code Definition Bit 0.** A Don't Care if a 1 to 7 bit length is selected.

RDNCD2 (10H): RECEIVE DOWN CODE DEFINITION REGISTER 2

(MSB)							(LSB)
C15	C14	C13	C12	C11	C10	C9	C8

SYMBOL	POSITION	NAME AND DESCRIPTION
C15	RDNCD2.7	**Receive Down Code Definition Bit 15**
C14	RDNCD2.6	**Receive Down Code Definition Bit 14**
C13	RDNCD2.5	**Receive Down Code Definition Bit 13**
C12	RDNCD2.4	**Receive Down Code Definition Bit 12**
C11	RDNCD2.3	**Receive Down Code Definition Bit 11**
C10	RDNCD2.2	**Receive Down Code Definition Bit 10**
C9	RDNCD2.1	**Receive Down Code Definition Bit 9**
C8	RDNCD2.0	**Receive Down Code Definition Bit 8**

8.2 LOOPBACKS

8.2.1 Remote Loopback (RLB)

When RLB (CCR6.6) is enabled, the DS2148 is placed into remote loopback. In this loopback, data from the clock/data recovery state machine will be looped back to the transmit path passing through the jitter attenuator if it is enabled. The data at the RPOS and RNEG pins will be valid while data presented at TPOS and TNEG will be ignored. See Figure 3-1 for details.

If the Automatic Remote Loop Back Enable (CCR6.5) is set to a one, the DS2148 will automatically go into remote loop back when it detects the loop up code programmed in the Receive Up Code Definition Registers (RUPCD1 and RUPCD2) for a minimum of 5 seconds. When the DS2148 detects the loop down code programmed in the Receive Loop Down Code Definition registers (RDNCD1 and RDNCD2) for a minimum of 5 seconds, the DS2148 will come out of remote loop back. The ARLB can also be disabled by setting ARLBE to a zero.

8.2.2 Local Loopback (LLB)

When LLB (CCR6.7) is set to a one, the DS2148 is placed into Local Loop Back. In this loopback, data on the transmit-side will continue to be transmitted as normal. TCLK and TPOS/TNEG will pass through the jitter attenuator (if enabled) and be output at RCLK and RPOS/RNEG. Incoming data from the line at RTIP and RRING will be ignored. If Transmit Unframed All Ones (CCR3.7) is set to a one while in LLB, TTIP and TRING will transmit all ones while TCLK and TPOS/TNEG will be looped back to RCLK and RPOS/RNEG. See Figure 3-1 for more details.

8.2.3 Analog Loopback (LLB)

Setting ALB (CCR6.4) to a one puts the DS2148 in Analog Loop Back. Signals at TTIP and TRING will be internally connected to RTIP and RRING. The incoming signals at RTIP and RRING will be ignored. The signals at TTIP and TRING will be transmitted as normal. See Figure 3-1 for more details.

8.2.4 Dual Loopback (DLB)

Setting both CCR6.7 and CCR6.6 to a one, LLB and RLB respectively, puts the DS2148 into Dual Loop Back operation. The TCLK and TPOS/TNEG signals will be looped back through the jitter attenuator (if enabled) and output at RCLK and RPOS/RNEG. Clock and data recovered from RTIP and RRING will be looped back to the transmit-side and output at TTIP and TRING. This mode of operation is not available when implementing hardware operation. See Figure 3-1 for more details.

8.3 PRBS GENERATION & DETECTION

Setting TPRBSE (CCR3.4) = 1 enables the DS2148 to transmit a 2^{15}-1 (E1) or a 2^{20}-1 (T1) Pseudo Random Bit Sequence (PRBS) depending on the ETS bit setting in CCR1.7. The receive-side of the DS2148 will always search for these PRBS patterns independent of CCR3.4. The PRBS Bit Error Output (PBEO) will remain high until the receiver has synchronized to one of the two patterns (64 bits received without an error) at which time PBEO will go low and the PRBSD bit in the Status Register (SR) will be set. Once synchronized, any bit errors received will cause a positive going pulse at PBEO, synchronous with RCLK. This output can be used with external circuitry to keep track of bit error rates during the PRBS testing. Setting CCR6.0 (ECRS) = 1 will allow the PRBS errors to be accumulated in the 16-bit counter in registers ECR1 and ECR2. The PRBS synchronizer will remain in sync until it experiences 6 bit errors or more within a 64 bit span. Both PRBS patterns comply with the ITU-T O.151 specifications.

8.4 ERROR COUNTER

Error Count Register 1 (ECR1) is the most significant word and ECR2 is the least significant word of a user selectable 16-bit counter that records incoming errors including BiPolar Violations (BPV), Code Violations (CV), Excessive Zero violations (EXZ) and/or PRBS Errors. See Table 8-3 and Table 8-4 and Figure 3-2 for details.

Table 8-3 **DEFINITION OF RECEIVED ERRORS**

ERROR	E1 OR T1	DEFINITION OF RECEIVED ERRORS
BPV	E1/T1	Two consecutive marks with the same polarity. Will ignore BPVs due to HDB3 and B8ZS zero suppression when CCR2.3 = 0. Typically used with AMI coding (CCR2.3 = 1). ITU-T O.161.
CV	E1	When HDB3 is enabled (CCR2.3 = 0) and the receiver detects two consecutive BPVs with the same polarity. ITU-T O.161.
EXZ	E1	When four or more consecutive zeros are detected.
EXZ	T1	When receiving AMI coded signals (CCR2.3 = 1), detection of 16 or more zeros or a BPV. ANSI T1.403 1999. When receiving B8ZS coded signals (CCR2.3 = 0), detection of 8 or more zeros or a BPV. ANSI T1.403 1999.
PRBS	E1/T1	A bit error in a received PRBS pattern. See section 8.3 for details. ITU-T O.151.

Table 8-4 **FUNCTION OF ECRS BITS AND RNEG PIN**

E1 or T1 (CCR1.7)	ECRS2 (CCR6.2)	ECRS1 (CCR6.1)	ECRS0 (CCR6.0)	RHBE (CCR2.3)	FUNCTION OF ECR COUNTERS/RNEG[1]
0	0	0	0	X	CVs
0	0	0	1	X	BPVs (HDB3 code words not counted)
0	0	1	0	X	CVs + EXZs
0	0	1	1	X	BPVs + EXZs
1	0	X	0	0	BPVs (B8ZS code words not counted)
1	0	X	1	0	BPVs + 8 EXZs
1	0	X	0	1	BPVs
1	0	X	1	1	BPVs + 16 EXZs
X	1	X	X	X	PRBS Errors[2]

NOTES:

1. RNEG outputs error data only when in NRZ mode (CCR1.6 = 1)
2. PRBS errors will always be output at PBEO independent of ECR control bits and NRZ mode and will not be present at RNEG.

8.4.1 Error Counter Update

A transition of the ECUE (CCR1.4) control bit from 0 to 1 will update the ECR registers with the current values and reset the counters. ECUE must be set back to zero and another 0 to 1 transition must occur for subsequent reads/resets of the ECR registers. Note that the DS2148 can report errors at RNEG when in NRZ mode (CCR1.6 = 1) by outputting a pulse for each error occurrence. The counter saturates at 65,535 and will not rollover.

ECR1 (11H): UPPER ERROR COUNT REGISTER 1
ECR2 (12H): LOWER ERROR COUNT REGISTER 2

(MSB)							**(LSB)**	
E15	E14	E13	E12	E11	E10	E9	E8	ECR1
E7	E6	E5	E4	E3	E2	E1	E0	ECR2

SYMBOL	POSITION	NAME AND DESCRIPTION
E15	ECR1.7	**MSB of the 16-bit error count**
E0	ECR2.0	**LSB of the 16-bit error count**

8.5 ERROR INSERTION

When IBPV (CCR3.1) is transitioned from a zero to a one, the device waits for the next occurrence of three consecutive ones to insert a BPV. IBPV must be cleared and set again for another BPV error insertion. See Figure 3-3 for details on the insertion of the BPV into the datasteam.

When IBE (CCR3.0) is transitioned from a zero to a one, the device will insert a logic error. IBE must be cleared and set again for another logic error insertion. See Figure 3-3 for details on the insertion of the logic error into the datasteam.

9. ANALOG INTERFACE

9.1 RECEIVER

The DS2148 contains a digital clock recovery system. The DS2148 couples to the receive E1 or T1 twisted pair (or coaxial cable in 75 ohm E1 applications) via a 1:1 transformer. See Table 9-3 and Table **9-4** for transformer details. Figure 9-1, Figure 9-2, and Figure 9-3 along with Table 9-1 and Table **9-2** show the receive termination requirements. The DS2148 has the option of using internal termination resistors.

The DS2148 is designed to be fully software-selectable for E1 and T1 without the need to change any external resistors for the receive-side. The receive-side will allow the user to configure the DS2148 for 75, 100, or 120 ohm receive termination by setting the RT1 (CCR5.1) and RT0 (CCR5.0) bits. When using the internal termination feature, the Rr resistors should be 60 ohms each. See Figure 9-1 for details. If external termination is required, RT1 and RT0 should be set to 0 and both Rr resistors in Figure 9-1 will need to be 37.5 ohms, 50 ohms, or 60 ohms each depending on the line impedance.

The resultant E1 or T1 clock derived from the 2.048/1.544 PLL (JACLK in Figure 3-1) is internally multiplied by 16 via another internal PLL and fed to the clock recovery system. The clock recovery system uses the clock from the PLL circuit to form a 16 times oversampler which is used to recover the clock and data. This oversampling technique offers outstanding performance to meet jitter tolerance specifications shown in Figure 9-6.

Normally, the clock that is output at the RCLK pin is the recovered clock from the E1 AMI/HDB3 or T1 AMI/B8ZS waveform presented at the RTIP and RRING inputs. When no signal is present at RTIP and RRING, a Receive Carrier Loss (RCL) condition will occur and the RCLK will be derived from the JACLK source. See Figure 3-1. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to an approximate 50% duty cycle. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLK output can exhibit slightly shorter high cycles of the clock. This is due to the highly oversampled digital clock recovery circuitry. See the Receive AC Timing Characteristics in Section 12 for more details.

The receive-side circuitry also contains a clock synthesizer which outputs a user configurable clock (up to 16.384 MHz) synthesized to RCLK at BPCLK (pin 31). See Table 6-3 for details on output clock frequencies at BPCLK. In hardware mode, BPCLK defaults to a 16.384 MHz output.

The DS2148 has a bypass mode for the receive side clock and data. This allows the BPCLK to be derived from RCLK after the jitter attenuator while the clock and data presented at RCLK, RPOS, and RNEG go unaltered. This is intended for applications where the receive side jitter attenuation will be done after the LIU. Setting RJAB (CCR6.3) to a logic 1 will enable the bypass. Be sure that the jitter attenuator is in the receive path (CCR4.3 = 0). See Figure 3-1 for details.

The DS2148 will report the signal strength at RTIP and RRING in 2.5 dB increments via RL3-RL0 located in the Receive Information Register 2. This feature is helpful when trouble shooting line performance problems. See Table 7-2 for details.

Monitor applications in both E1 and T1 require various flat gain settings for the receive-side circuitry. The DS2148 can be programmed to support these applications via the Monitor Mode control bits MM1 and MM0. When the monitor modes are enabled, the receiver will tolerate normal line loss up to –6 dB. See Table 6-4 for details.

9.2 TRANSMITTER

The DS2148 uses a set of laser-trimmed delay lines along with a precision Digital-to-Analog Converter (DAC) to create the waveforms that are transmitted onto the E1 or T1 line. The waveforms created by the DS2148 meet the latest ETSI, ITU, ANSI, and AT&T specifications. The user will select which waveform is to be generated by setting the ETS bit (CCR1.7) for E1 or T1 operation, then programming the L2/L1/L0 bits in Common Control Register 4 for the appropriate application. See Table 9-1 and Table 9-2 for the proper L2/L1/L0 settings.

A 2.048 MHz or 1.544 MHz TTL clock is required at TCLK for transmitting data at TPOS and TNEG. ITU specification G.703 requires an accuracy of +/-50 ppm for both T1 and E1. TR62411 and ANSI specs require an accuracy of +/- 32 ppm for T1 interfaces. The clock can be sourced internally by RCLK or JACLK. See CCR1.2, CCR1.1, CCR1.0, and Figure 3-3 for details. Due to the nature of the design of the transmitter in the DS2148, very little jitter (less than 0.005 UIpp broadband from 10 Hz to 100 kHz) is added to the jitter present on TCLK. Also, the waveforms created are independent of the duty cycle of TCLK. The transmitter in the DS2148 couples to the E1 or T1 transmit twisted pair (or coaxial cable in some E1 applications) via a 1:1.36 or 1:2 step-up transformer depending on power supply and the application. In order for the device to create the proper waveforms, the transformer used must meet the specifications listed in Table 9-3 and Table 9-4.

The DS2148 has automatic short-circuit limiter which limits the source current to 50 mA (rms) into a 1 ohm load. This feature can be disabled by setting the SCLD bit (CCR2.5) = 1. When the current limiter is activated, TCLE (SR.2) will be set even if short circuit limiter is disabled. The TPD bit (CCR4.0) will power-down the transmit line driver and tri-state the TTIP and TRING pins. The DS2148 can also detect when the TTIP or TRING outputs are open circuited. When an open circuit is detected, TOCD (SR.1) will be set.

9.3 JITTER ATTENUATOR

The DS2148 contains an onboard jitter attenuator that can be set to a depth of either 32 or 128 bits via the JABDS bit (CCR4.2). The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay sensitive applications. The characteristics of the attenuation are shown in Figure 9-7. The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit (CCR4.3). Also, the jitter attenuator can be disabled (in effect, removed) by setting the DJA bit (CCR4.1). In order for the jitter attenuator to operate properly, a 2.048 MHz or 1.544 MHz clock must be applied at MCLK. ITU specification G.703 requires an accuracy of +/-50 ppm for both T1 and E1. TR62411 and ANSI specs require an accuracy of +/- 32 ppm for T1 interfaces. There is an onboard PLL for the jitter attenuator, which will convert the 2.048 MHz clock to a 1.544 MHz rate for T1 applications. Setting JAMUX (CCR1.3) to a logic 0 bypasses this PLL. Onboard circuitry adjusts either the recovered clock from the clock/data recovery block or the clock applied at the TCLK pin to create a smooth jitter free clock which is used to clock data out of the jitter attenuator FIFO. It is acceptable to provide a gapped/bursty clock at the TCLK pin if the jitter attenuator is placed on the transmit side. If the incoming jitter exceeds either 120 UIpp (buffer depth is 128 bits) or 28 UIpp (buffer depth is 32 bits), then the DS2148 will divide the internal nominal 32.768 MHz (E1) or 24.704 MHz (T1) clock by either 15 or 17 instead of the normal 16 to keep the buffer from overflowing. When the device divides by either 15 or 17, it also sets the Jitter Attenuator Limit Trip (JALT) bit in the Receive Information Register 1 (RIR1).

9.4 G.703 SYNCHRONIZATION SIGNAL

The DS2148 is capable of receiving a 2.048 MHz square wave synchronization clock as specified in section 10 of ITU G.703. In order to use the DS2148 in this mode, set the Receive Synchronization Clock Enable (CCR5.3) = 1. The DS2148 can also transmit the 2.048 MHz square wave synchronization clock as specified in section 10 of G.703. In order to transmit the 2.048 MHz clock, set the Transmit Synchronization Clock Enable (CCR5.2) = 1.

Table 9-1 **LINE BUILD OUT SELECT FOR E1 IN REGISTER CCR4 (ETS = 0)**

L2	L1	L0	VDD	APPLICATION	N	RETURN LOSS	Rt
0	0	0	5V	75Ω normal	1:1.36	NM	0Ω
0	0	1	5V	120Ω normal	1:1.36	NM	0Ω
1	0	0	5V	75Ω w/ high return loss	1:1.36	21 dB	18Ω
1	0	1	5V	120Ω w/ high return loss	1:1.36	21 dB	27Ω
0	0	0	3.3V	75Ω normal	1:2	NM	0Ω
0	0	1	3.3V	120Ω normal	1:2	NM	0Ω
1	0	0	3.3V	75Ω w/ high return loss	1:2	21 dB	6.2Ω
1	0	1	3.3V	120Ω w/ high return loss	1:2	21 dB	11.6Ω

NOTES:

1. See Figure 9-1, Figure 9-2, and Figure 9-3.

Table 9-2 **LINE BUILD OUT SELECT FOR T1 IN REGISTER CCR4 (ETS = 1)**

L2	L1	L0	VDD	APPLICATION	N	RETURN LOSS	Rt
0	0	0	5V	DSX-1 (0 to 133 feet) / 0 DB CSU	1:1.36	NM	0Ω
0	0	1	5V	DSX-1 (133 to 266 feet)	1:1.36	NM	0Ω
0	1	0	5V	DSX-1 (266 to 399 feet)	1:1.36	NM	0Ω
0	1	1	5V	DSX-1 (399 to 533 feet)	1:1.36	NM	0Ω
1	0	0	5V	DSX-1 (533 to 655 feet)	1:1.36	NM	0Ω
1	0	1	5V	-7.5 dB CSU	1:1.36	NM	0Ω
1	1	0	5V	-15 dB CSU	1:1.36	NM	0Ω
1	1	1	5V	-22.5 dB CSU	1:1.36	NM	0Ω
0	0	0	3.3V	DSX-1 (0 to 133 feet) / 0 DB CSU	1:2	NM	0Ω
0	0	1	3.3V	DSX-1 (133 to 266 feet)	1:2	NM	0Ω
0	1	0	3.3V	DSX-1 (266 to 399 feet)	1:2	NM	0Ω
0	1	1	3.3V	DSX-1 (399 to 533 feet)	1:2	NM	0Ω
1	0	0	3.3V	DSX-1 (533 to 655 feet)	1:2	NM	0Ω
1	0	1	3.3V	-7.5 dB CSU	1:2	NM	0Ω
1	1	0	3.3V	-15 dB CSU	1:2	NM	0Ω
1	1	1	3.3V	-22.5 dB CSU	1:2	NM	0Ω

NOTES:

1. See Figure 9-1, Figure 9-2, and Figure 9-3.

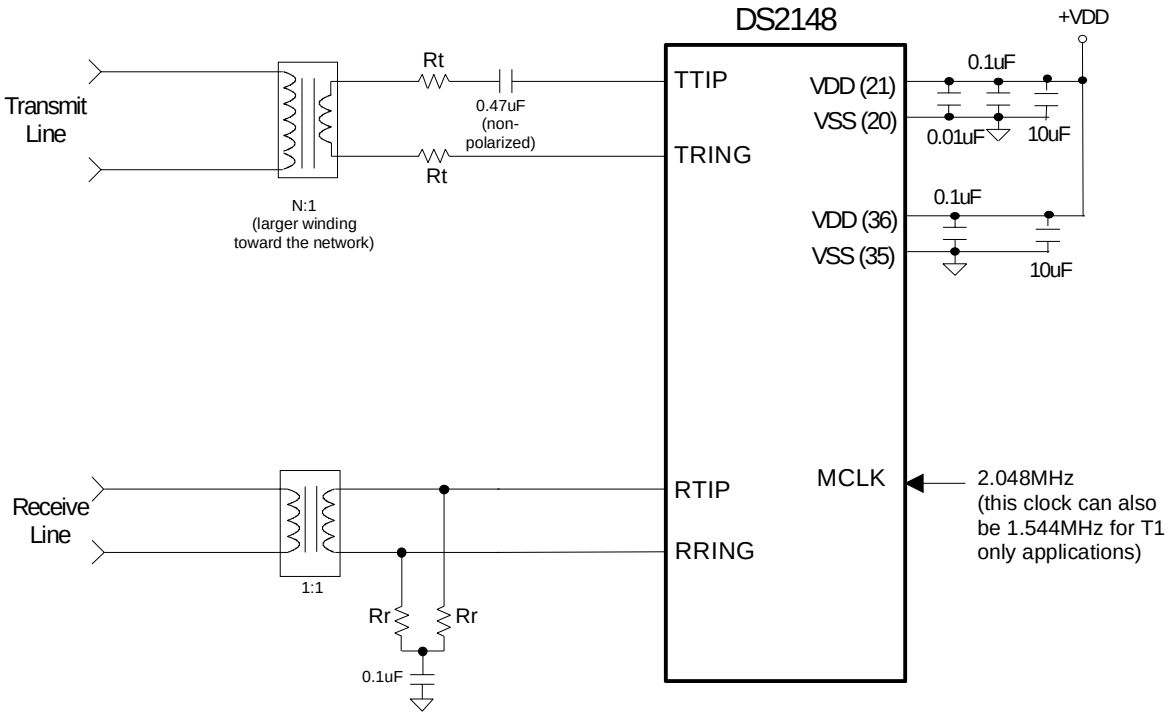
Table 9-3 **TRANSFORMER SPECIFICATIONS FOR 5V OPERATION**

SPECIFICATION	RECOMMENDED VALUE
Turns Ratio 5V Applications	1:1(receive) and 1:1.36(transmit) +/-2%
Primary Inductance	600 µH minimum
Leakage Inductance	1.0 µH maximum
Interwinding Capacitance	40 pF maximum
Transmit Transformer DC Resistance Primary (Device Side) Secondary	 1.2Ω maximum 1.2Ω maximum
Receive Transformer DC Resistance Primary (Device Side) Secondary	 1.2Ω maximum 1.2Ω maximum

Table 9-4 **TRANSFORMER SPECIFICATIONS FOR 3.3V OPERATION**

SPECIFICATION	RECOMMENDED VALUE
Turns Ratio 3.3V Applications	1:1(receive) and 1:2(transmit) +/-2%
Primary Inductance	600 µH minimum
Leakage Inductance	1.0 µH maximum
Intertwining Capacitance	40 pF maximum
Transmit Transformer DC Resistance Primary (Device Side) Secondary	 1.0Ω maximum 2.0Ω maximum
Receive Transformer DC Resistance Primary (Device Side) Secondary	 1.2Ω maximum 1.2Ω maximum

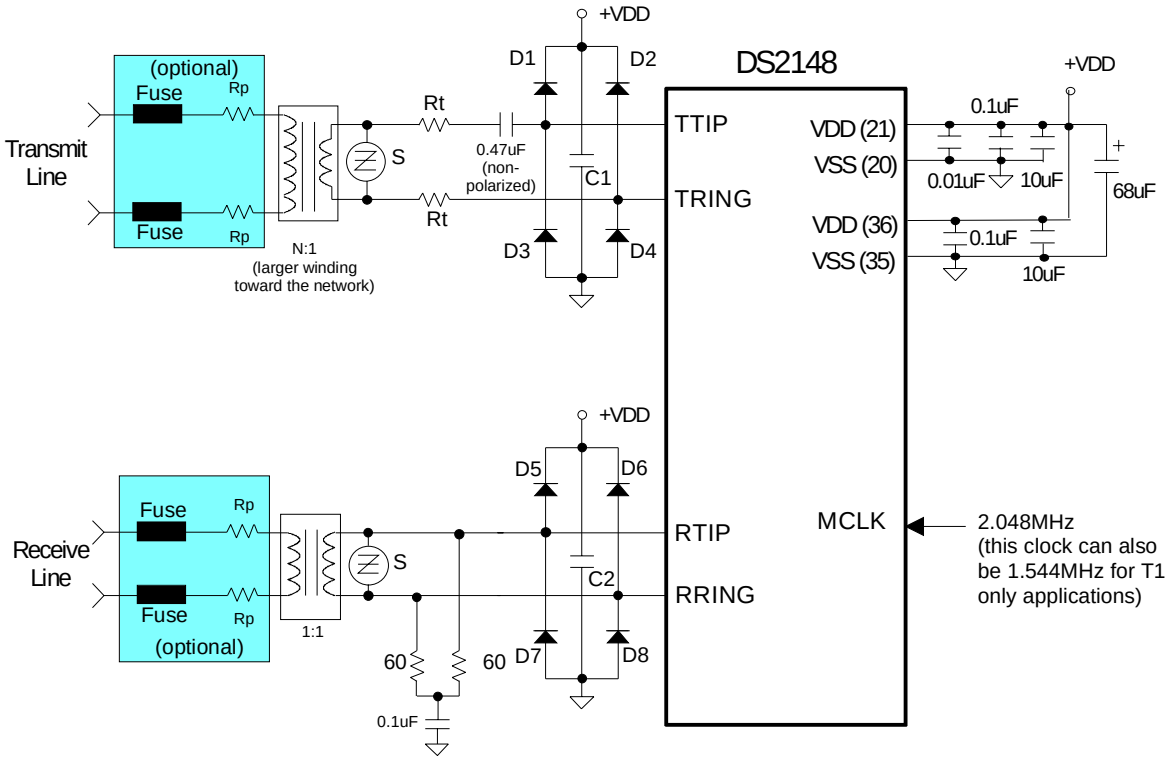
Figure 9-1 **BASIC INTERFACE**



NOTES:

1. All resistor values are +/- 1%.
2. In E1 applications, the Rt resistors are used to increase the transmitter return loss (see Table 9-1). No return loss is required for T1 applications.
3. The Rr resistors should be set to 60Ω each if the internal receive-side termination feature is enabled. When this feature is disabled, Rr = 37.5Ω for 75Ω or 60Ω for 120Ω E1 systems, or 50Ω for 100Ω T1 lines.
4. See Table 9-1 and Table 9-2 for the appropriate transmit transformer turns ratio (N).

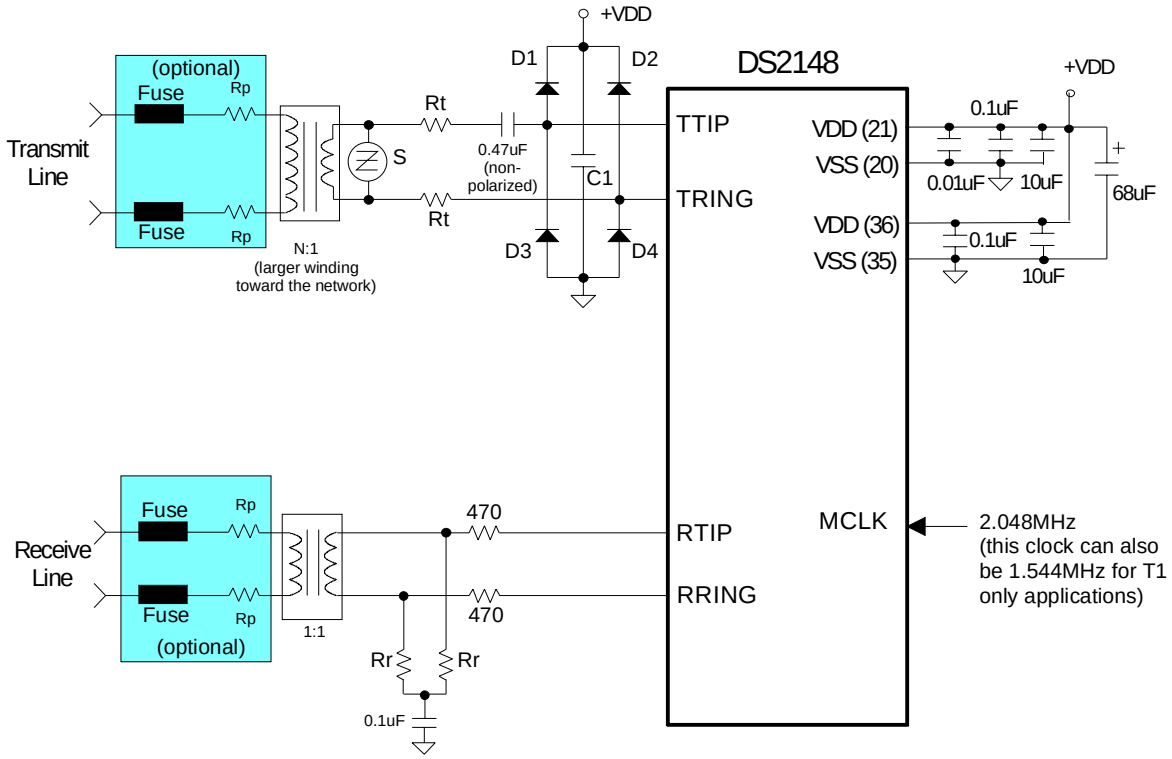
Figure 9-2 **PROTECTED INTERFACE USING INTERNAL RECEIVE TERMINATION**



NOTES:

1. All resistor values are +/- 1%.
2. C1 = C2 = 0.1 uF.
3. S is a 6V transient suppresser.
4. D1 to D8 are Schottky diodes.
5. The fuses are optional to prevent AC power line crosses from compromising the transformers.
6. Rp resistors exist to keep the Fuses from opening during a surge. If they are used, then the 60Ω receive termination resistance must be adjusted to match the line impedance.
7. The Rt resistors are used to increase the transmitter return loss (see Table 9-1). No return loss is required for T1 applications.
8. The transmit transformer turns ratio (N) would be 1:1.36 for 5V operation or 1:2 for 3.3V operation.
9. The 68 µF is used to keep the local power plane potential within tolerance during a surge.

Figure 9-3 **PROTECTED INTERFACE USING EXTERNAL RECEIVE TERMINATION**



NOTES:

1. All resistor values are +/- 1%.
2. C1 = 0.1 uF.
3. S is a 6V transient suppresser.
4. D1 to D4 are Schottky diodes.
5. The fuses are optional to prevent AC power line crosses from compromising the transformers.
6. Rp resistors exist to keep the Fuses from opening during a surge. If they are used, then Rr must be adjusted to match the line impedance.
7. Rr = 37.5Ω for 75Ω or 60Ω for 120Ω E1 systems, or 50Ω for 100Ω T1 lines.
8. The Rt resistors are used to increase the transmitter return loss (see Table 9-1). No return loss is required for T1 applications.
9. The transmit transformer turns ratio (N) would be 1:1.36 for 5V operation or 1:2 for 3.3V operation.
10. The 68µF is used to keep the local power plane potential within tolerance during a surge.

Figure 9-4 **E1 TRANSMIT PULSE TEMPLATE**

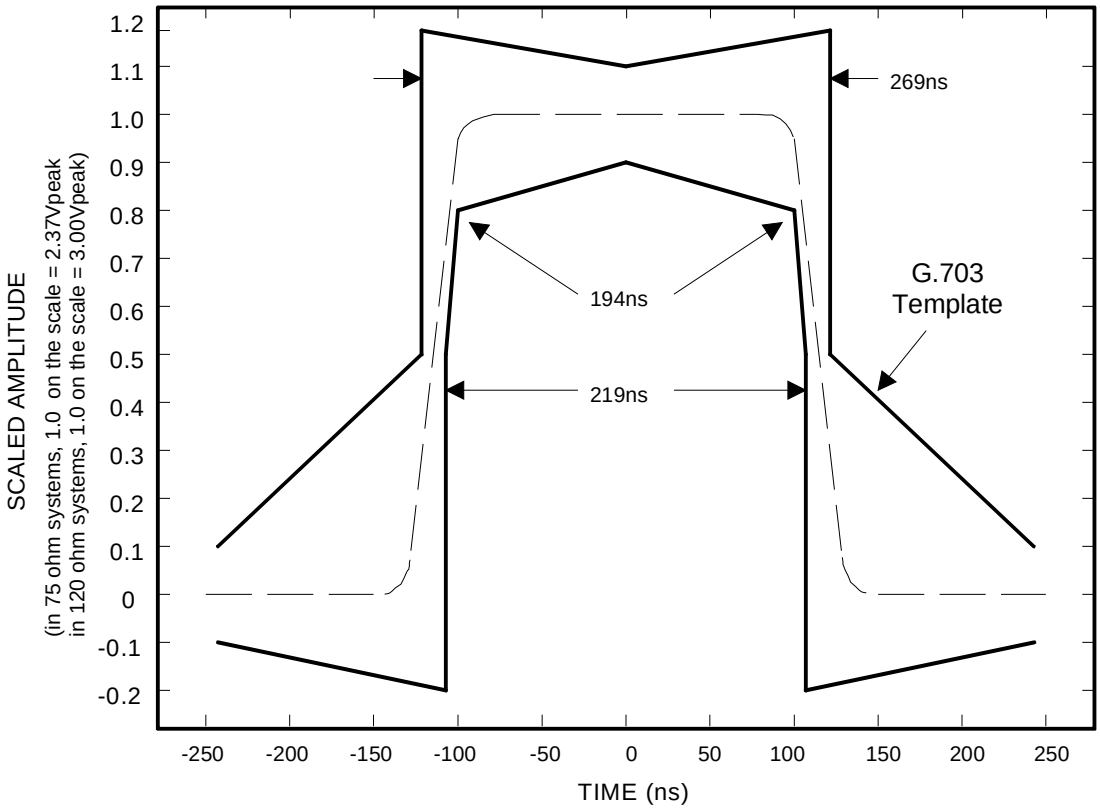


Figure 9-5 **T1 TRANSMIT PULSE TEMPLATE**

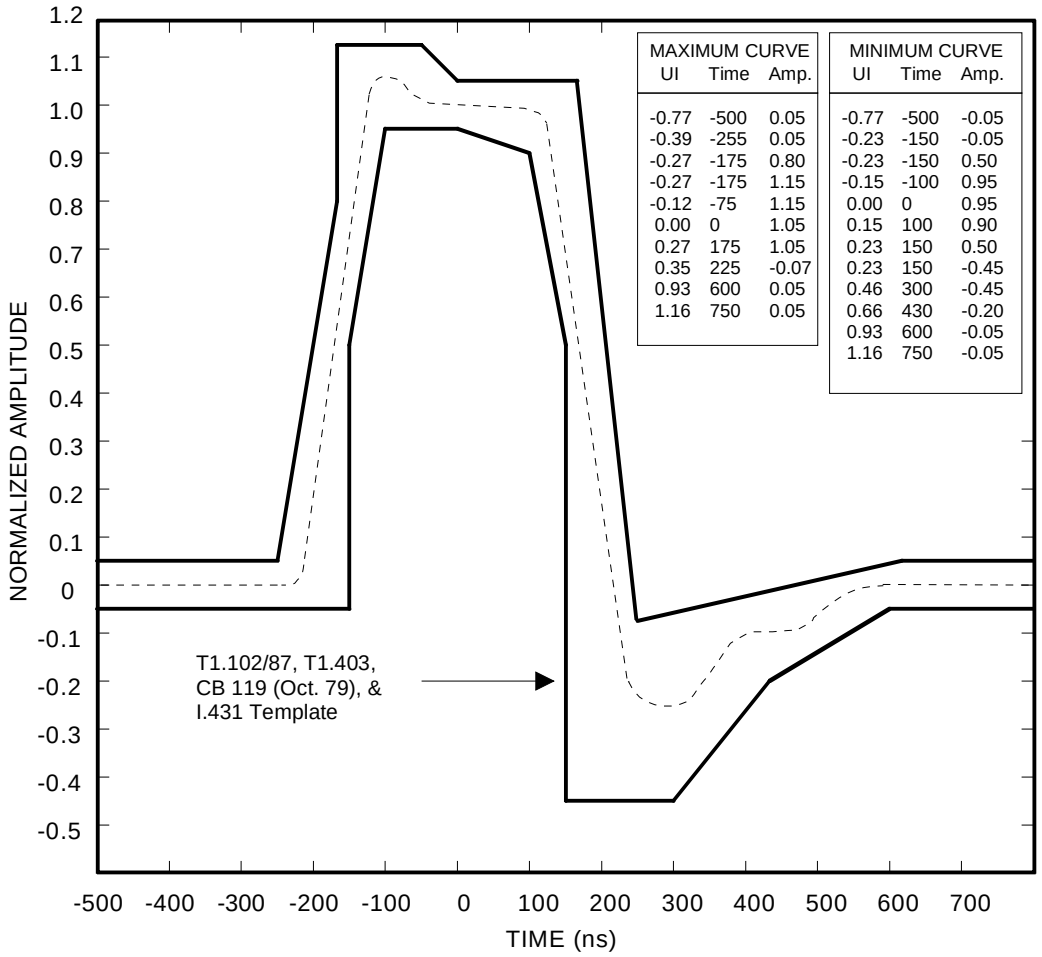


Figure 9-6 **JITTER TOLERANCE**

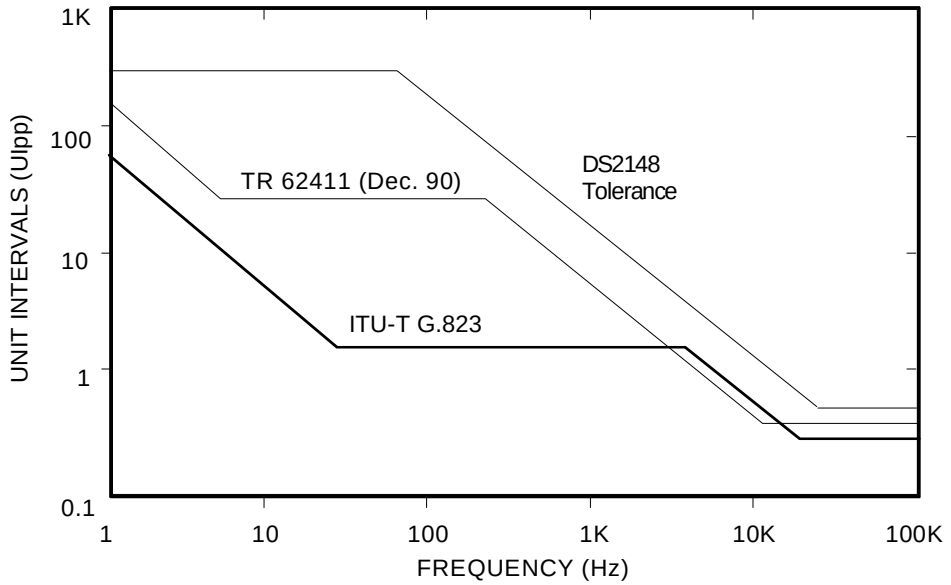
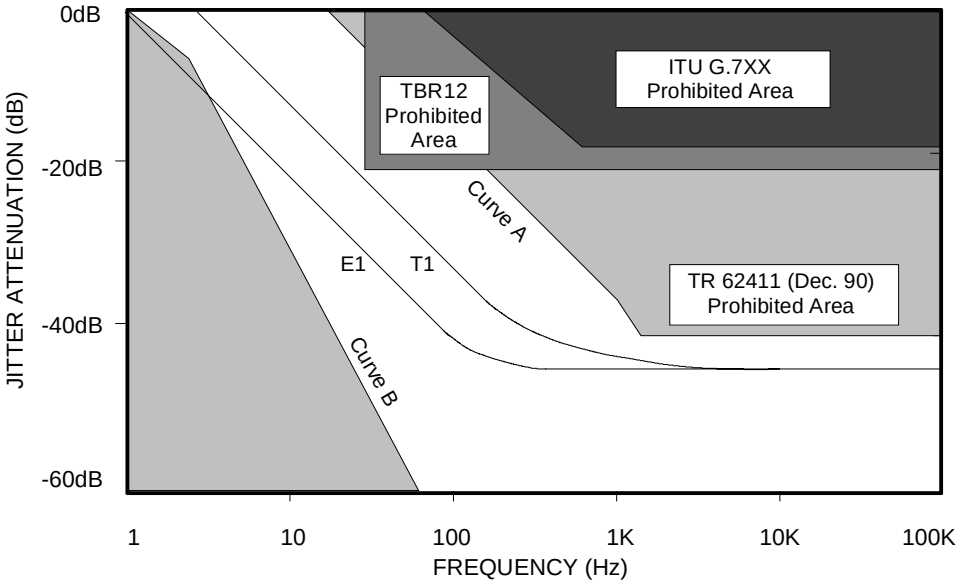


Figure 9-7 **JITTER ATTENUATION**



10. DS21Q48 QUAD LIU

The DS21Q48 is a quad version of the DS2148G utilizing CABGA on carrier packaging technology. The 4 LIUs are controlled via the parallel port mode. Serial and Hardware mode are unavailable in this package.

Table 110-1 **DS21Q48 PIN ASSIGNMENT**

DS21Q48 PIN#	I/O	PARALLEL PORT MODE
J1	I	Connect to VSS
K3	I	Connect to VSS
J2	I	RD*(DS*)
H1	I	WR*(R/W*)
K2	I	ALE(AS)
K1	I/O	A4
L1	I	A3
H11	I	A2
H12	I	A1
G12	I	A0
J10	I/O	D7/AD7
H10	I/O	D6/AD6
G11	I/O	D5/AD5
J9	I/O	D4/AD4
E3	I/O	D3/AD3
D4	I/O	D2/AD2
F3	I/O	D1/AD1
D5	I/O	D0/AD0
G4	I	VSM
K9	I/O	INT*
K7	I	TEST
L9	I	HRST*
J6	I	MCLK
L7	I	BIS0
M8	I	BIS1
M12	I	PBTS
J3	I	CS*1
D3	I	CS*2
D10	I	CS*3
K10	I	CS*4
K5	O	PBEO1
G3	O	PBEO2
E10	O	PBEO3
K8	O	PBEO4
L6	O	RCL/LOTC1
D7	O	RCL/LOTC2
F9	O	RCL/LOTC3

DS21Q48 PIN#	I/O	PARALLEL PORT MODE
J7	O	RCL/LOTC4
A1	I	RTIP1
A4	I	RTIP2
A7	I	RTIP3
A10	I	RTIP4
B2	I	RRING1
B5	I	RRING2
B8	I	RRING3
B11	I	RRING4
H4	O	BPCLK1
D6	O	BPCLK2
F10	O	BPCLK3
L8	O	BPCLK4
A2	O	TTIP1
A5	O	TTIP2
A8	O	TTIP3
A11	O	TTIP4
B3	O	TRING1
B6	O	TRING2
B9	O	TRING3
B12	O	TRING4
K4	O	RPOS1
E1	O	RPOS2
D11	O	RPOS3
K11	O	RPOS4
G2	O	RNEG1
E2	O	RNEG2
F11	O	RNEG3
M10	O	RNEG4
H3	O	RCLK1
F1	O	RCLK2
E11	O	RCLK3
L11	O	RCLK4
G1	I	TPOS1
F2	I	TPOS2
E12	I	TPOS3
M11	I	TPOS4
H2	I	TNEG1
M1	I	TNEG2
D12	I	TNEG3
K12	I	TNEG4
M2	I	TCLK1
L2	I	TCLK2
F12	I	TCLK3
L12	I	TCLK4

DS21Q48 PIN#	I/O	PARALLEL PORT MODE
J5	-	VDD1
D2	-	VDD2
G9	-	VDD3
M9	-	VDD4
L5	-	VDD1
E4	-	VDD2
D8	-	VDD3
J8	-	VDD4
J4	-	VSS1
D1	-	VSS2
E9	-	VSS3
L10	-	VSS4
M4	-	VSS1
F4	-	VSS2
D9	-	VSS3
H9	-	VSS4

Figure 110-1 **BGA 12 x 12 PIN LAYOUT**

	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
A	RTIP 1	TTIP 1	NC	RTIP 2	TTIP 2	NC	RTIP 3	TTIP 3	NC	RTIP 4	TTIP 4	NC
B	NC	RRING 1	TRING 1	NC	RRING 2	TRING 2	NC	RRING 3	TRING 3	NC	RRING 4	TRING 4
C	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
D	VSS 2	VDD 2	CS* 2	D2/ AD2	D0/ AD0	BPCLK 2	RCL/ LOTC2	VDD 3	VSS 3	CS* 3	RPOS 3	TNEG 3
E	RPOS 2	RNEG 2	D3/ AD3	VDD 2	NC	NC	NC	NC	VSS 3	PEBO 3	RCLK 3	TPOS 3
F	RCLK 2	TPOS 2	D1/ AD1	VSS 2	NC	NC	NC	NC	RCL/ LOTC3	BPCLK 3	RNEG 3	TCLK 3
G	TPOS 1	RNEG 1	PEBO 2	VSM	NC	NC	NC	NC	VDD 3	NC	D5/ AD5	A0
H	WR* (R/W*)	TNEG 1	RCLK 1	BPCLK 1	NC	NC	NC	NC	VSS 4	D6/ AD6	A2	A1
J	**See Note 2**	RD* (DS*)	CS* 1	VSS 1	VDD 1	MCLK	RCL/ LOTC4	VDD 4	D4/ AD4	D7/ AD7	NC	NC
K	A4	ALE (AS)	**See Note 2**	RPOS 1	PEBO 1	NC	TEST	PEBO 4	INT*	CS* 4	RPOS 4	TNEG 4
L	A3	TCLK 2	NC	NC	VDD 1	RCL/ LOTC1	BIS0	BPCLK 4	HRST*	VSS 4	RCLK 4	TCLK 4
M	TNEG 2	TCLK 1	NC	VSS 1	NC	NC	NC	BIS1	VDD 4	RNEG 4	TPOS 4	PBTS

NOTES:

1. Shaded areas are signals common to all four devices
2. Connect to VSS.

11. DC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +6.0V
Operating Temperature for DS2148TN	–40°C to +85°C
Storage Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		5.5	V	
Logic 0	V_{IL}	–0.3		+0.8	V	
Supply for 3.3V Operation	V_{DD}	3.135	3.3	3.465	V	1
Supply for 5V Operation	V_{DD}	4.75	5	5.25	V	1

CAPACITANCE (t_A =25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS (-40°C to +85°C; V_{DD} = 3.3V ± 5%; -40°C to +85°C; V_{DD} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{IL}	–1.0		+1.0	µA	3
Output Leakage	I_{LO}			1.0	µA	4
Output Current (2.4V)	I_{OH}	–1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	
Power dissipation @ 3.3V	P_{DD}	-	320	370	mW	2,5

NOTES:

1. Applies to V_{DD}.
2. TCLK = MCLK = 2.048 MHz.
3. $0.0V < V_{IN} < V_{DD}$.
4. Applied to INT* when 3–stated.
5. Power dissipation with TTIP and TRING driving a 30Ω load, for an all 1’s data density.

12. AC CHARACTERISTICS

AC CHARACTERISTICS –MULTIPLEXED PARALLEL PORT

(BIS1 = 0, BIS0 = 0)

[See Figure 12-1, Figure 12-2, Figure 12-3]

(-40°C to +85°C; V_{DD} = 3.3V ± 5%;
-40°C to +85°C; V_{DD} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	200			ns	
Pulse Width, DS low or RD* high	PW_{EL}	100			ns	
Pulse Width, DS high or RD* low	PW_{EH}	100			ns	
Input Rise/Fall times	t_R , t_F			20	ns	
R/W* Hold Time	t_{RWH}	10			ns	
R/W* Set Up time before DS high	t_{RWS}	50			ns	
CS* Set Up time before DS, WR* or RD* active	t_{CS}	20			ns	
CS* Hold time	t_{CH}	0			ns	
Read Data Hold time	t_{DHR}	10		50	ns	
Write Data Hold time	t_{DHW}	0			ns	
Muxed Address valid to AS or ALE fall	t_{ASL}	15			ns	
Muxed Address Hold time	t_{AHL}	10			ns	
Delay time DS, WR* or RD* to AS or ALE rise	t_{ASD}	20			ns	
Pulse Width AS or ALE high	PW_{ASH}	30			ns	
Delay time, AS or ALE to DS, WR* or RD*	t_{ASED}	10			ns	
Output Data Delay time from DS or RD*	t_{DDR}	20		80	ns	
Data Set Up time	t_{DSW}	50			ns	

Figure 12-1 **INTEL BUS READ TIMING (PBTS = 0, BIS1 = 0, BIS0 = 0)**

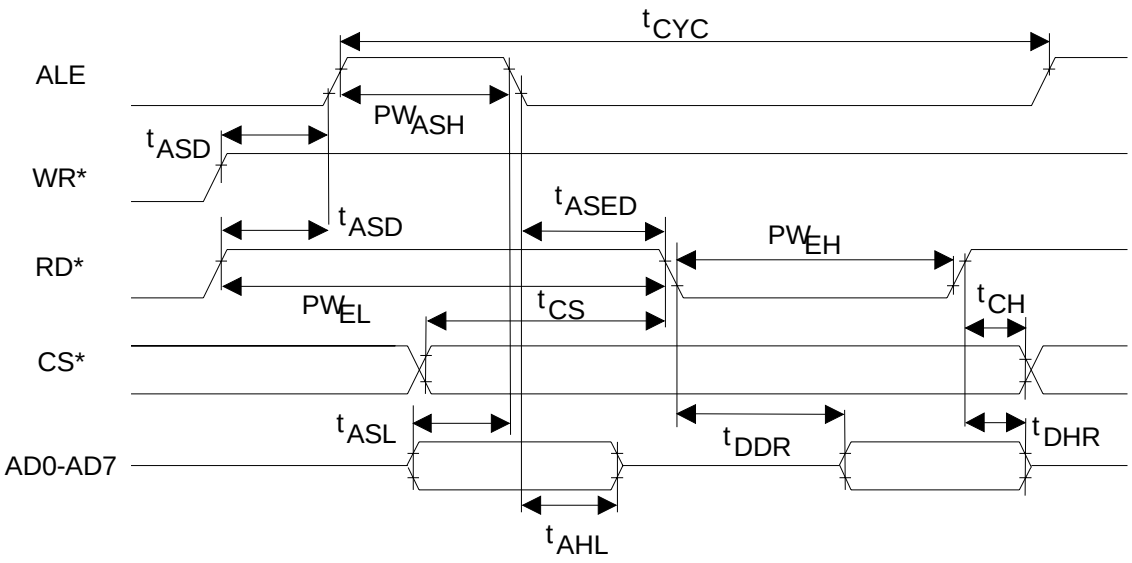


Figure 12-2 **INTEL BUS WRITE TIMING (PBTS = 0, BIS1 = 0, BIS0 = 0)**

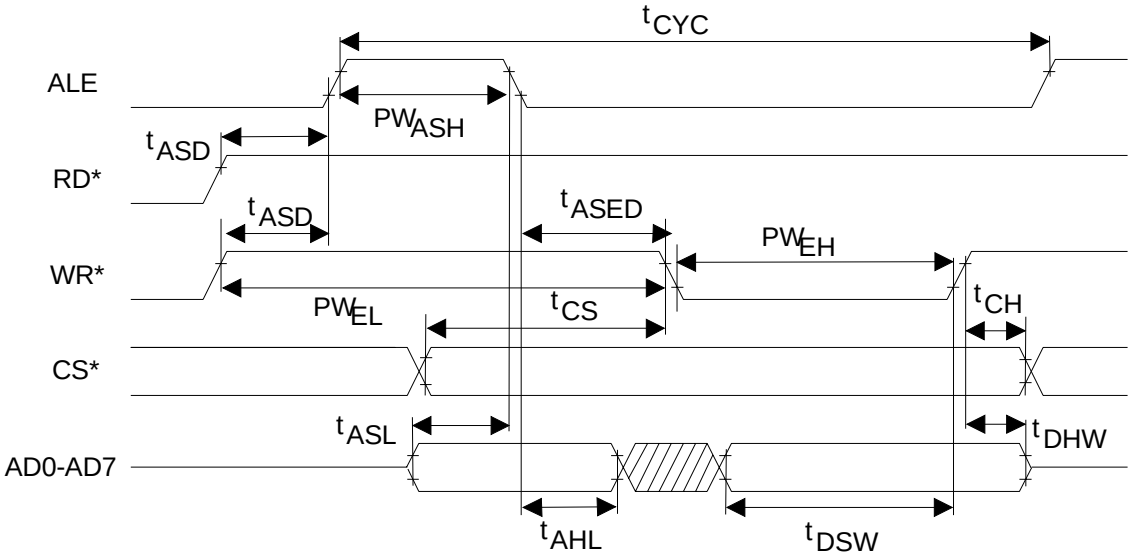
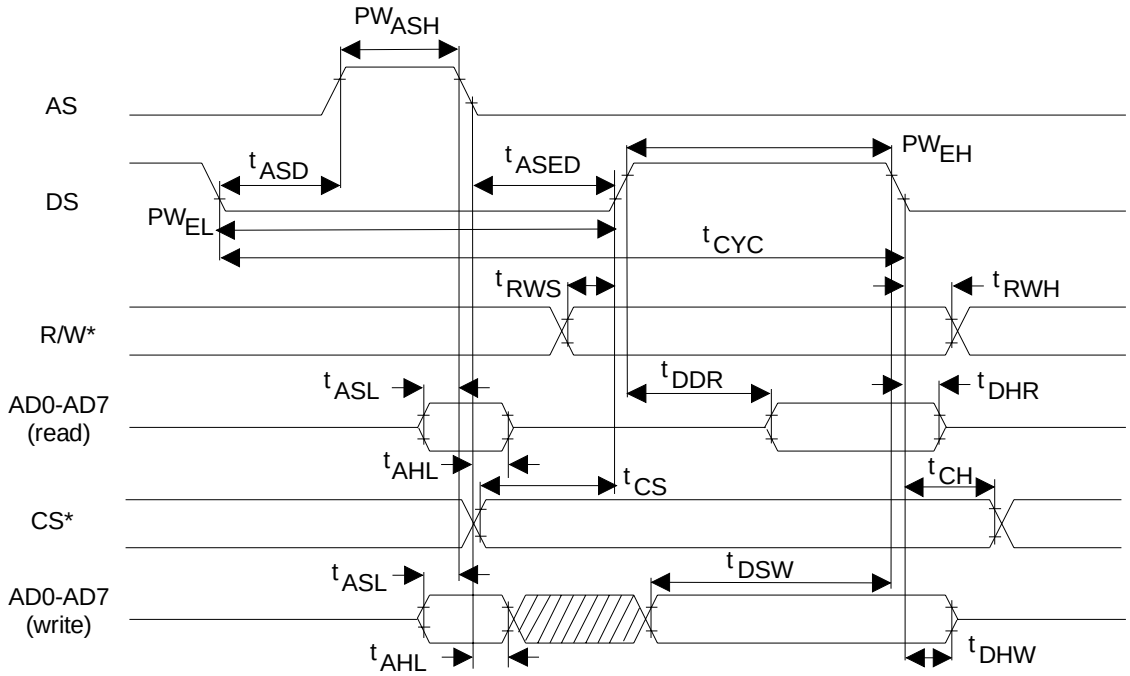


Figure 12-3 **MOTOROLA BUS TIMING (PBTS = 1, BIS1 = 0, BIS0 = 0)**



AC CHARACTERISTICS – NON-MULTIPLEXED PARALLEL PORT

(BIS1 = 0, BIS0 = 1)

[See Figure12-4, Figure 12-5, Figure 12-6, Figure 12-7]

(-40°C to +85°C; V_{DD} = 3.3V ± 5%;
-40°C to +85°C; V_{DD} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Set Up Time for A0 to A4, Valid to CS* Active	t1	0			ns	
Set Up Time for CS* Active to either RD*, WR*, or DS* Active	t2	0			ns	
Delay Time from either RD* or DS* Active to Data Valid	t3			75	ns	
Hold Time from either RD*, WR*, or DS* Inactive to CS* Inactive	t4	0			ns	
Hold Time from CS* Inactive to Data Bus 3–state	t5	5		20	ns	
Wait Time from either WR* or DS* Active to Latch Data	t6	75			ns	
Data Set Up Time to either WR* or DS* Inactive	t7	10			ns	
Data Hold Time from either WR* or DS* Inactive	t8	10			ns	
Address Hold from either WR* or DS* inactive	t9	10			ns	

Figure12-4 **INTEL BUS READ TIMING (PBTS = 0, BIS1 = 0, BIS0 = 1)**

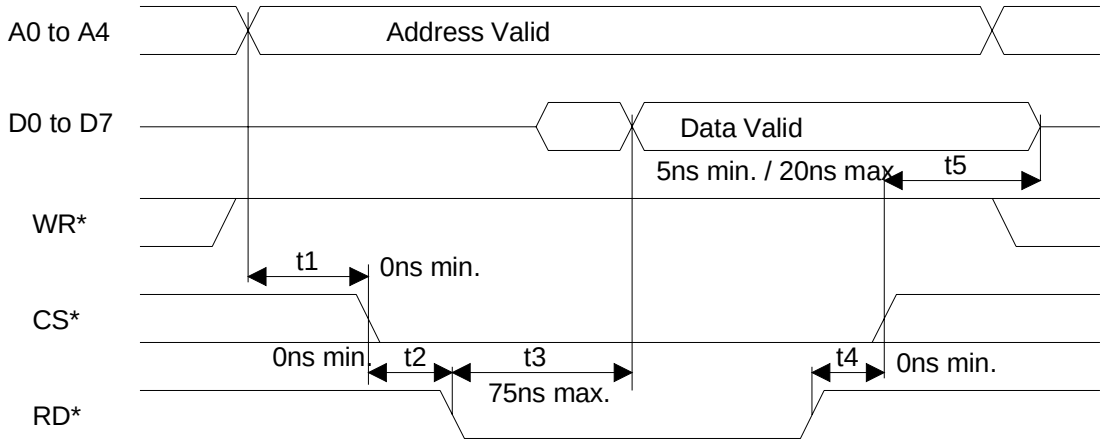


Figure 12-5 **INTEL BUS WRITE TIMING (PBTS = 0, BIS1 = 0, BIS0 = 1)**

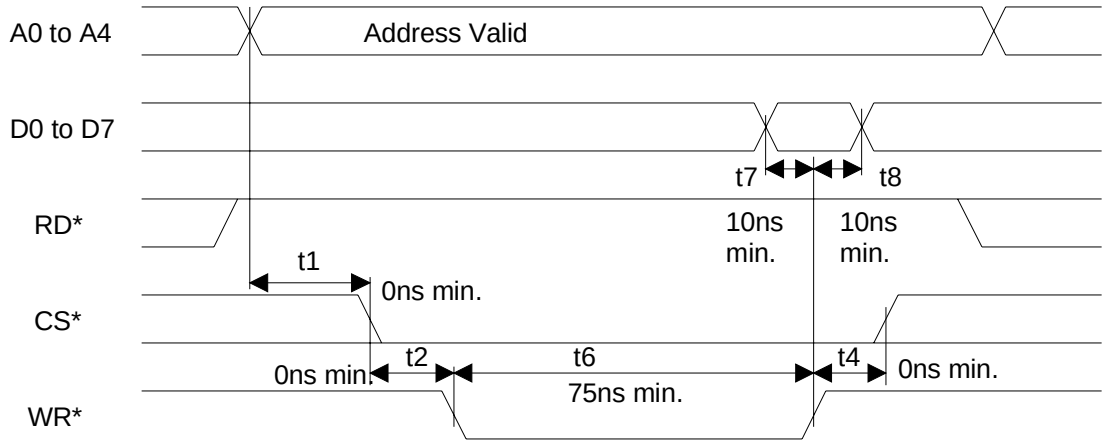


Figure 12-6 **MOTOROLA BUS READ TIMING (PBTS = 1, BIS1 = 0, BIS0 = 1)**

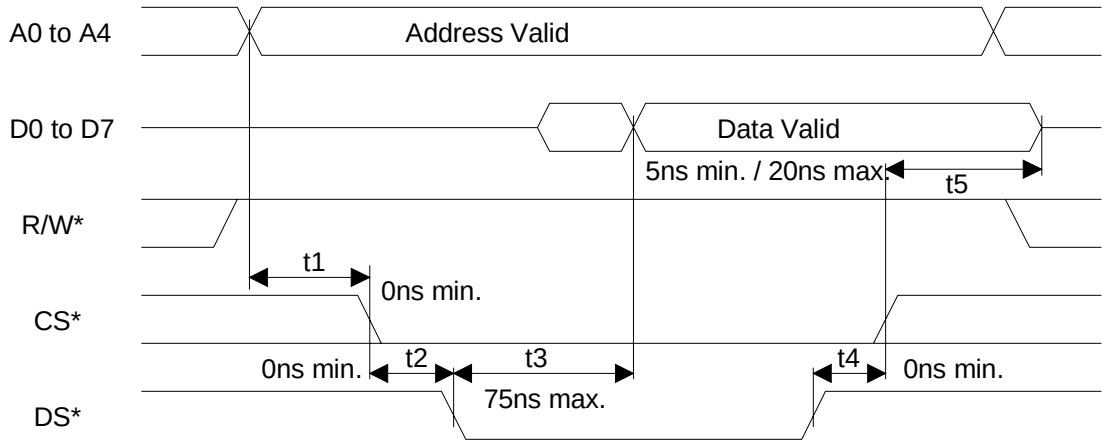
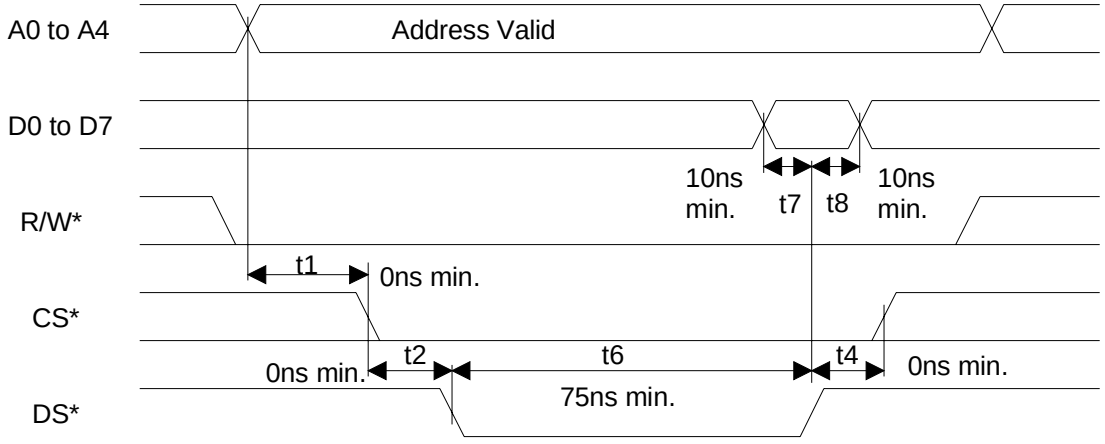


Figure 12-7 **MOTOROLA BUS WRITE TIMING (PBTS = 1, BIS1 = 0, BIS0 = 1)**

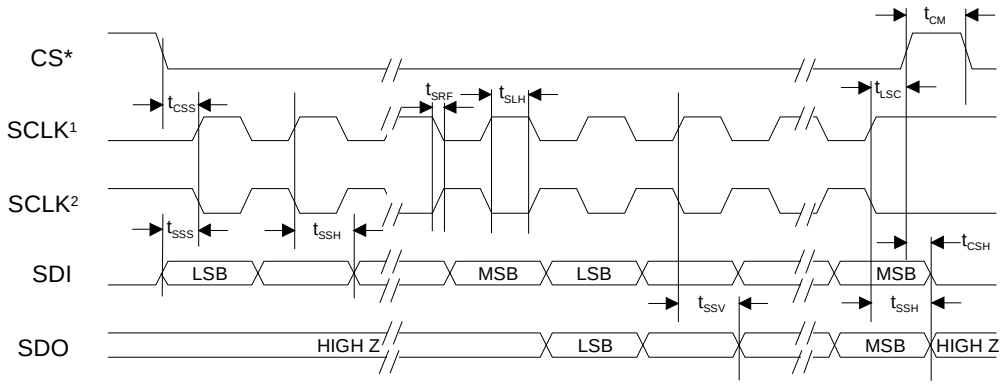


AC CHARACTERISTICS –SERIAL PORT

(BIS1 = 1, BIS0 = 0) (-40°C to +85°C; V_{DD} = 3.3V ± 5%;
[See Figure 12-8] -40°C to +85°C; V_{DD} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Set Up Time CS* to SCLK	t_{CSS}	50			ns	
Set Up Time SDI to SCLK	t_{SSS}	50			ns	
Hold Time SCLK to SDI	t_{SSH}	50			ns	
SCLK High/Low Time	t_{SLH}	200			ns	
SCLK Rise/Fall Time	t_{SRF}			50	ns	
SCLK to CS* Inactive	t_{LSC}	50			ns	
CS* Inactive Time	t_{CM}	250			ns	
SCLK to SDO Valid	t_{SSV}			50	ns	
SCLK to SDO Tri-State	t_{SSH}		100		ns	
CS* Inactive to SDO Tri-State	t_{CSH}		100		ns	

Figure 12-8 **SERIAL BUS TIMING (BIS1 = 1, BIS0 = 0)**



NOTES:

1. OCES =1 & ICES = 0.
2. OCES = 0 & ICES = 1.

AC CHARACTERISTICS – RECEIVE SIDE

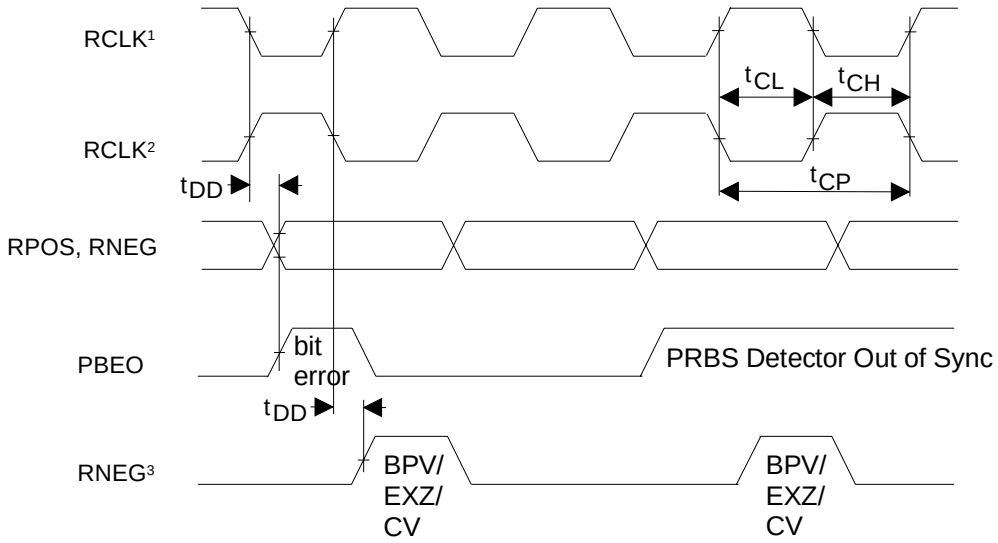
[See Figure 12-9] (-40°C to +85°C; VDD = 3.3V ± 5%; -40°C to +85°C; VDD = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{CP}		488 648		ns ns	1 2
RCLK Pulse Width	t_{CH} t_{CL}	200 200			ns ns	3 3
RCLK Pulse Width	t_{CH} t_{CL}	150 150			ns ns	4 4
Delay RCLK to RPOS, RNEG, PBEO, RBPV Valid	t_{DD}			50	ns	

NOTES:

1. E1 Mode.
2. T1 or J1 Mode.
3. Jitter attenuator enabled in the receive path.
4. Jitter attenuator disabled or enabled in the transmit path.

Figure 12-9 **RECEIVE SIDE TIMING**



NOTES:

1. RCES = 1 (CCR2.0) or CES = 1.
2. RCES = 0 (CCR2.0) or CES = 0.
3. RNEG is in NRZ mode (CCR1.6 = 1).

AC CHARACTERISTICS – TRANSMIT SIDE

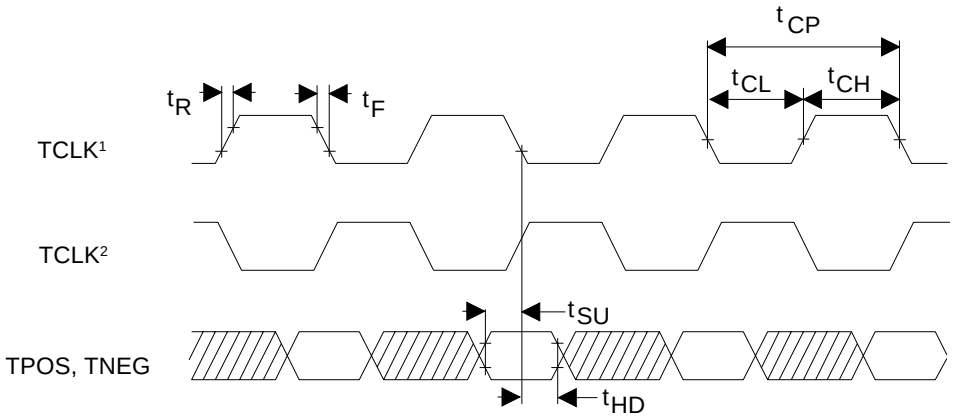
[See Figure 12-10] (-40°C to +85°C; V_{DD} = 3.3V ± 5%; -40°C to +85°C; V_{DD} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_{CP}		488 648		ns ns	1 2
TCLK Pulse Width	t_{CH} t_{CL}	75 75			ns ns	
TPOS/TNEG Set Up to TCLK Falling or Rising	t_{SU}	20			ns	
TPOS/TNEG Hold from TCLK Falling or Rising	t_{HD}	20			ns	
TCLK Rise and Fall Times	t_R , t_F			25	ns	

NOTES:

1. E1 Mode.
2. T1 or J1 Mode.

Figure 12-10 **TRANSMIT SIDE TIMING**



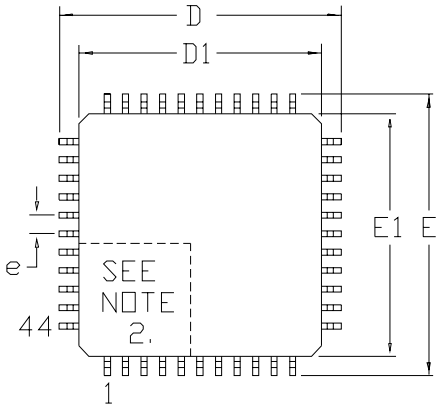
Notes:

1. TCES = 0 (CCR2.1) or CES = 0.
2. TCES = 1 (CCR2.1) or CES = 1.

13. MECHANICAL DIMENSIONS

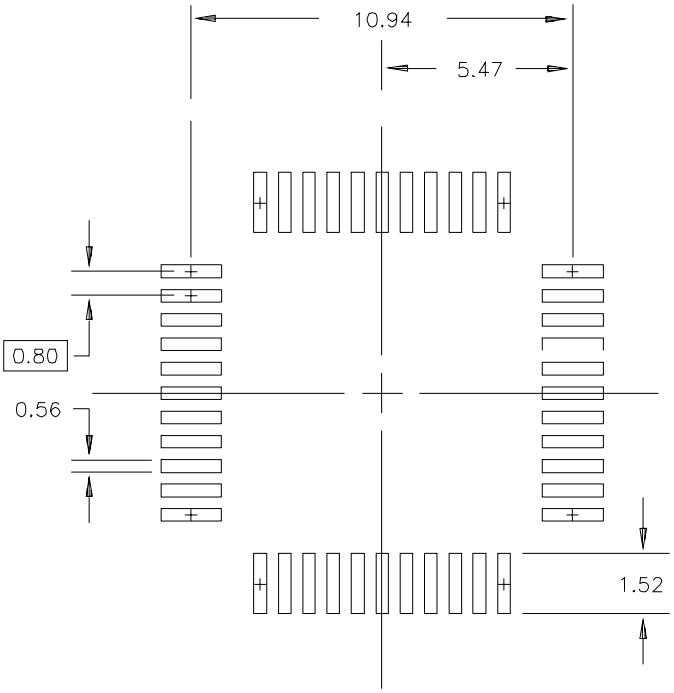
NOTES:

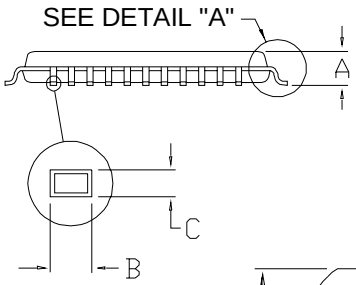
1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; AT MAXIMUM MATERIAL CONDITION. PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.
4. CONTROLLING DIMENSIONS: MILLIMETERS.



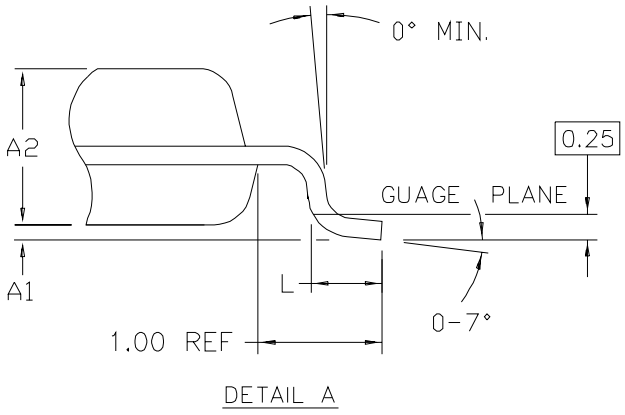
SUGGESTED PAD LAYOUT

44 PIN TQFP, 10*10*1.0

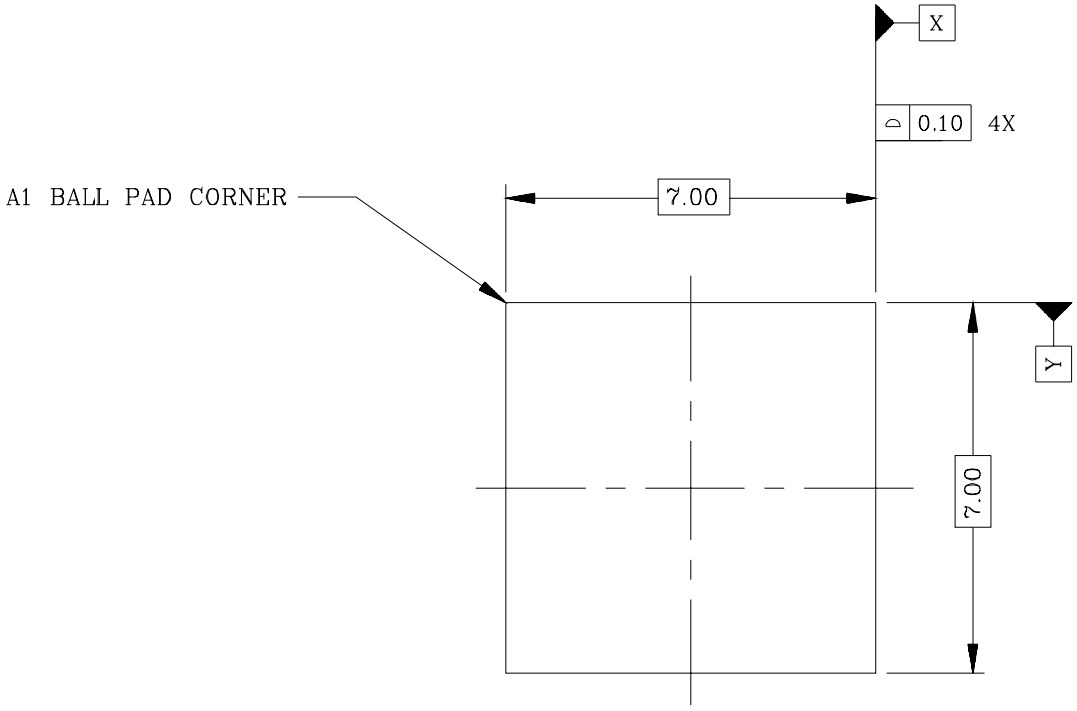


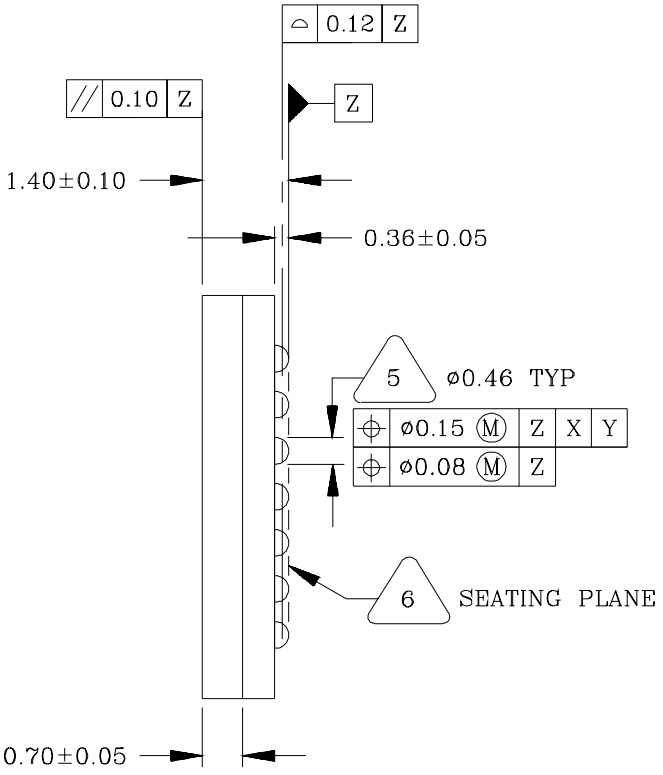


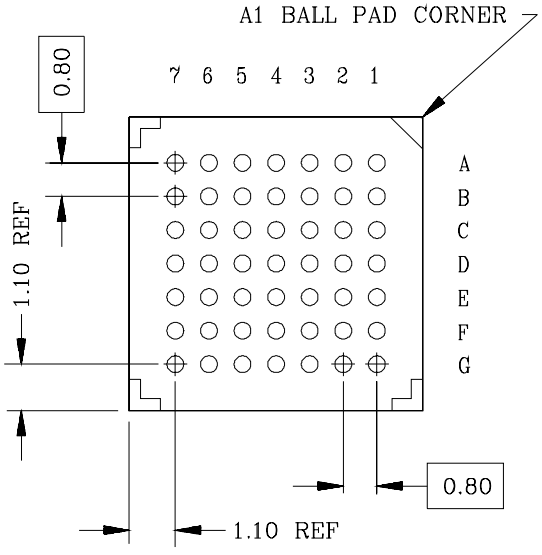
DIM	MIN	MAX
A	–	1.20
A1	0.05	0.15
A2	0.95	1.05
D	11.80	12.20
D1	10.00 BSC	
E	11.80	12.20
E1	10.00 BSC	
L	0.45	0.75
e	0.80 BSC	
B	0.30	0.45
C	0.09	0.20



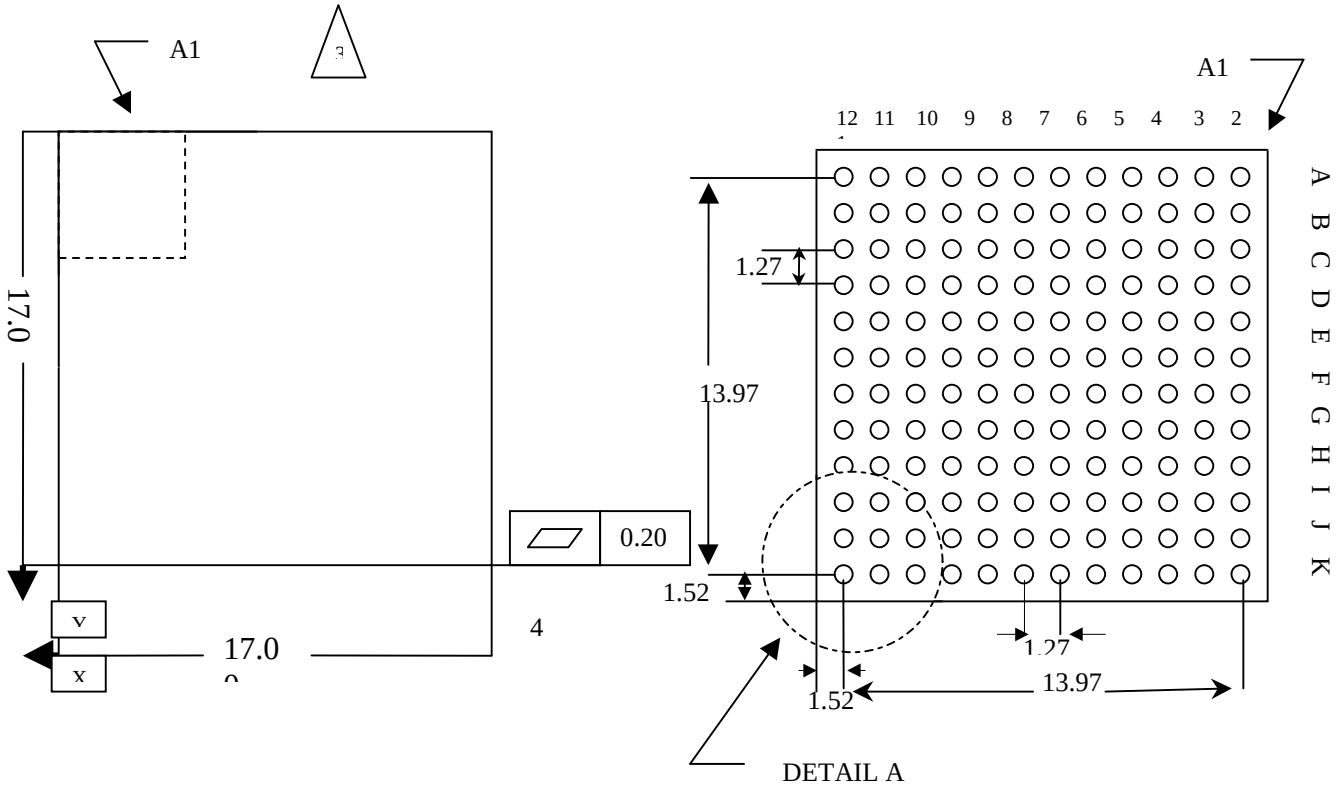
DIMENSIONS ARE IN MILLIMETERS


X
0.10 4X
A1 BALL PAD CORNER
7.00
Y
7.00

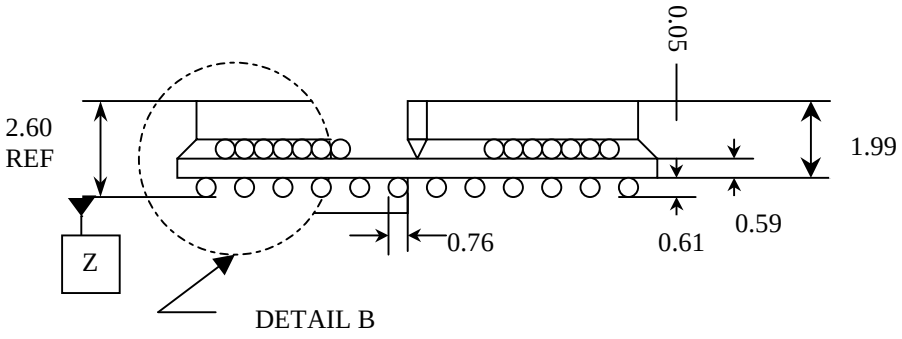

0.12 Z
0.10 Z
Z
1.40±0.10
0.36±0.05
5
ø0.46 TYP
ø0.15 M Z X Y
ø0.08 M Z
6
SEATING PLANE
0.70±0.05


A1 BALL PAD CORNER
0.80
7 6 5 4 3 2 1
A
B
C
D
E
F
G
1.10 REF
0.80
1.10 REF

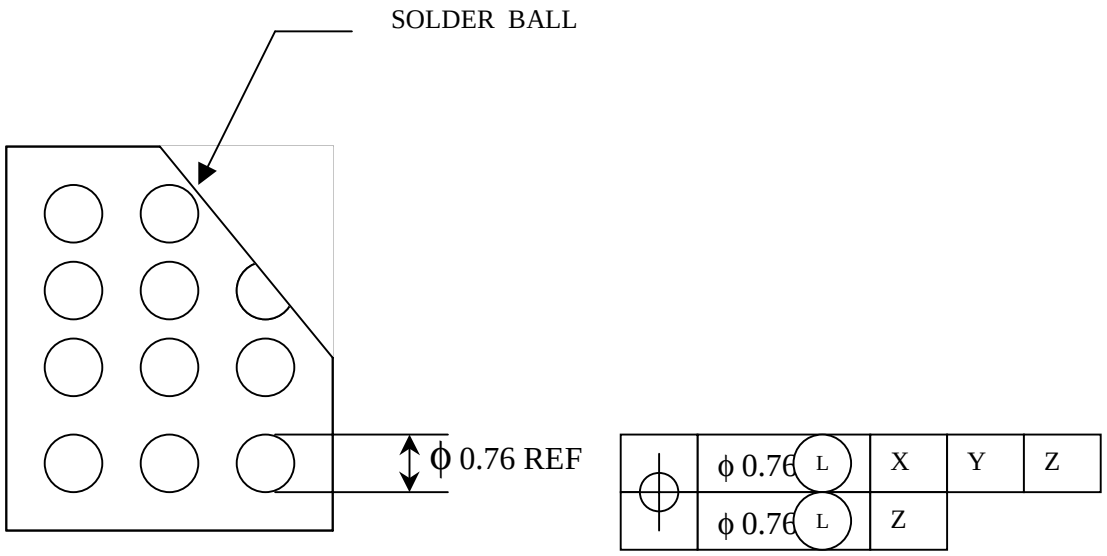
13.1 MECHANICAL DIMENSIONS –QUAD VERSION



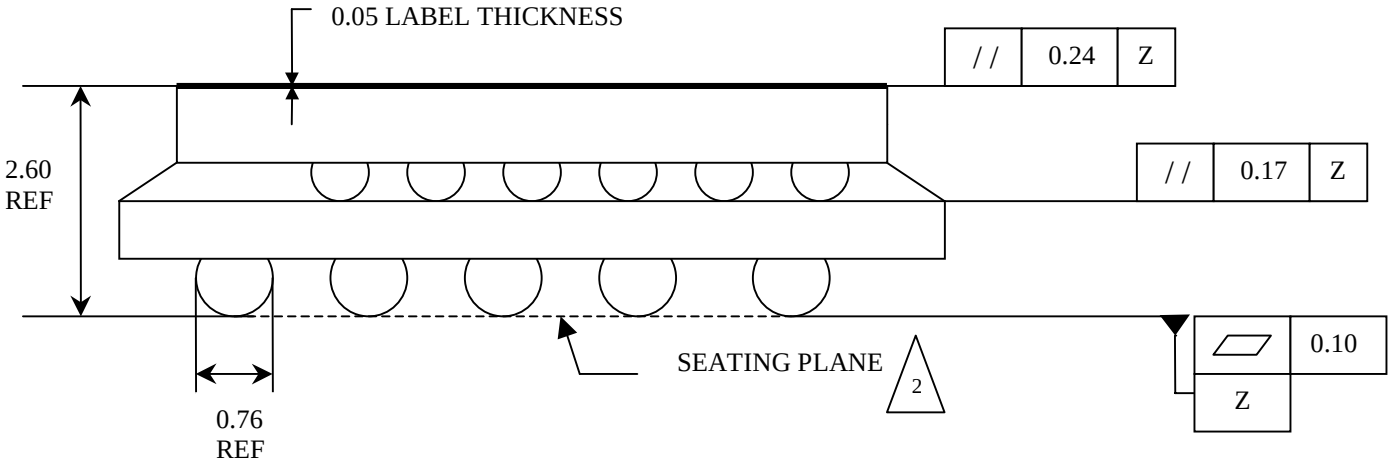
TOP VIEW (DIE SIDE) **BOTTOM VIEW (BALL SIDE)**



SIDE VIEW



DETAIL A



DETAIL B