

# DATA SHEET

## **74ALVCH16373**

**2.5V/3.3V 16-bit D-type transparent latch  
(3-State)**

Product specification  
Supersedes data of 1998 Jun 29  
IC24 Data Handbook

1999 Sep 20

## 16-bit D-type transparent latch (3-State)

74ALVCH16373

## FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold
- Output drive capability 50Ω transmission lines @ 85°C
- Current drive  $\pm 24$  mA at 3.0 V

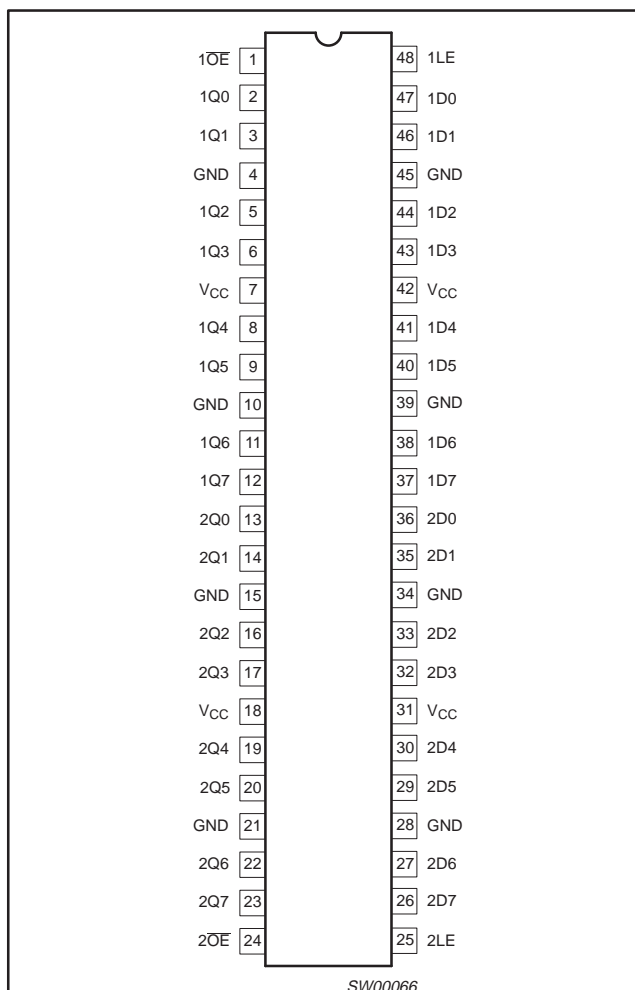
## DESCRIPTION

The 74ALVCH16373 is a 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. Incorporates bus hold data inputs which eliminate the need for external pull-up or pull-down resistors to hold unused inputs. One latch enable (LE) input and one output enable ( $\overline{OE}$ ) are provided per 8-bit section.

The 74ALVCH16373 consists of 2 sections of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When  $\overline{OE}$  is LOW, the contents of the eight latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches.

## PIN CONFIGURATION



## QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5\text{ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT	
$t_{PHL}/t_{PLH}$	Propagation delay Dn to Qn	$V_{CC} = 2.5\text{V}$ , $C_L = 30\text{pF}$	2.1	ns	
		$V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pF}$	2.1		
	Propagation delay LE to Qn	$V_{CC} = 2.5\text{V}$ , $C_L = 30\text{pF}$	2.2		
		$V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pF}$	2.2		
$C_I$	Input capacitance		5.0	pF	
$C_{PD}$	Power dissipation capacitance per latch	$V_I = \text{GND to } V_{CC}^1$	Outputs enabled	16	pF
			Outputs disabled	10	

## NOTE:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74ALVCH16373 DL	ACH16373 DL	SOT370-1
48-Pin Plastic TSSOP Type II	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74ALVCH16373 DGG	ACH16373 DGG	SOT362-1

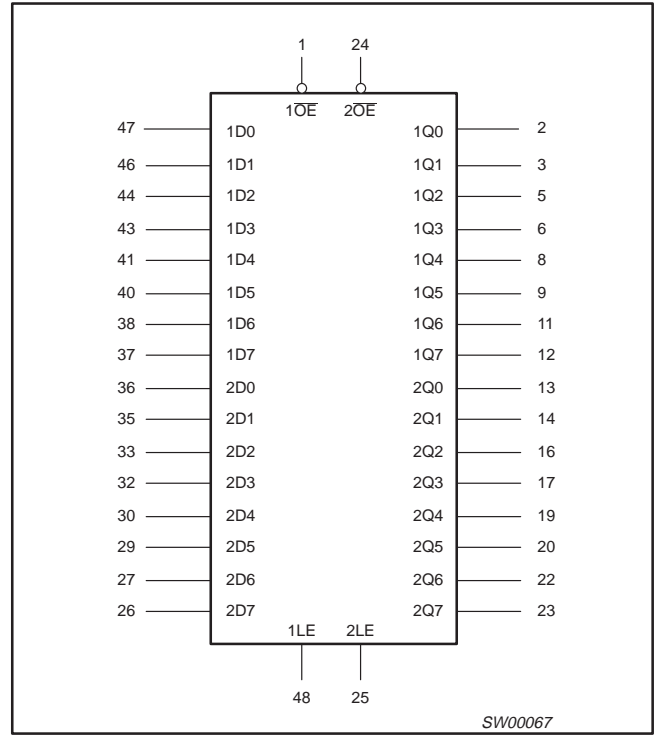
# 16-bit D-type transparent latch (3-State)

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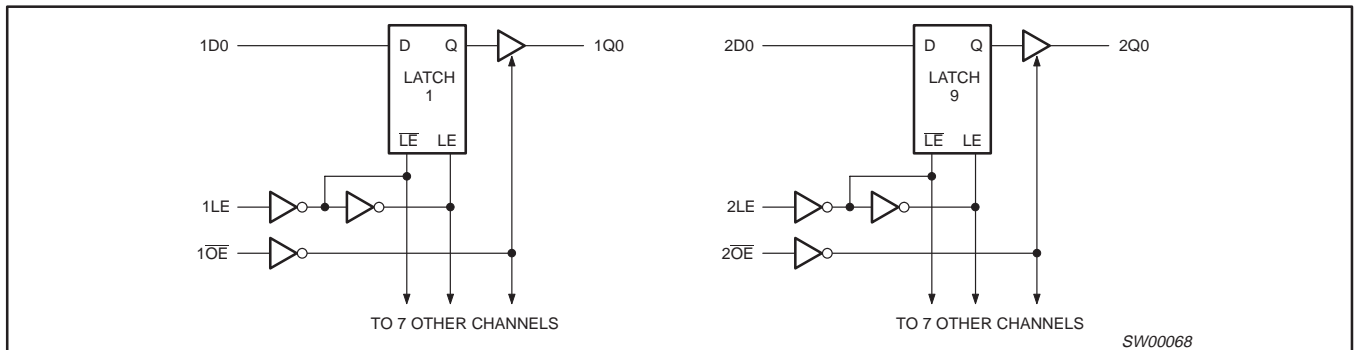
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1OE	Output enable input (active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V <sub>CC</sub>	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	Data inputs/outputs
24	2OE	Output enable input (active LOW)
25	2LE	Latch enable input (active HIGH)
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data inputs
48	1LE	Latch enable input (active HIGH)

## LOGIC SYMBOL



## LOGIC DIAGRAM



## FUNCTION TABLE (per section of eight bits)

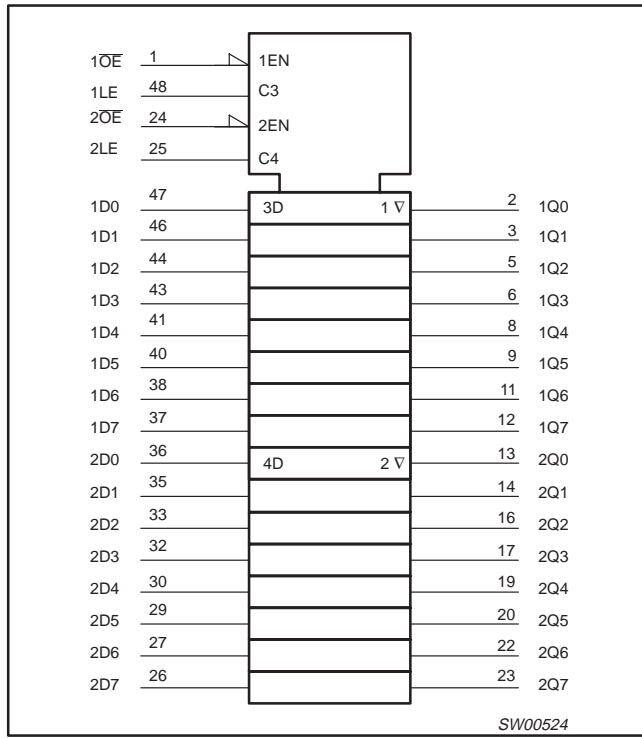
OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	nOE	nLE	nDn		
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register (hold mode)	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition  
 X = don't care  
 Z = high impedance OFF-state

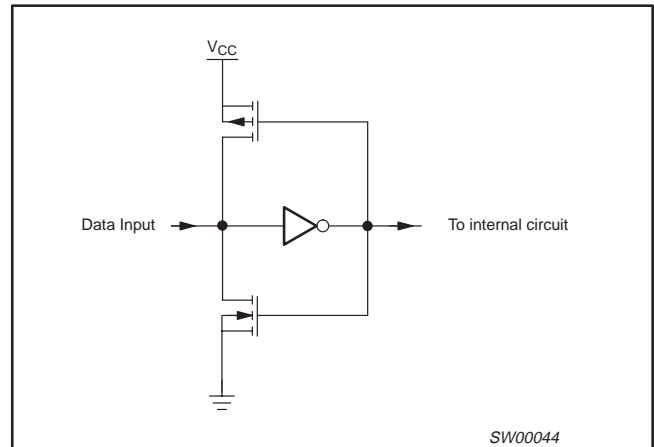
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## LOGIC SYMBOL (IEEE/IEC)



## BUS HOLD CIRCUIT



## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V <sub>CC</sub>	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V <sub>I</sub>	DC Input voltage range	For data input pins	0	V <sub>CC</sub>	V
		For control pins	0	5.5	
V <sub>O</sub>	DC output voltage range		0	V <sub>CC</sub>	V
T <sub>amb</sub>	Operating free-air temperature range		-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input rise and fall times	V <sub>CC</sub> = 2.3 to 3.0V	0	20	ns/V
		V <sub>CC</sub> = 3.0 to 3.6V	0	10	

## 16-bit D-type transparent latch (3-State)

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**ABSOLUTE MAXIMUM RATINGS**

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +4.6	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	For control pins <sup>2</sup>	-0.5 to +4.6	V
		For data inputs <sup>2</sup>	-0.5 to $V_{CC} + 0.5$	
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	$\pm 50$	mA
$V_O$	DC output voltage	Note 2	-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	$\pm 50$	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		$\pm 100$	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package	For temperature range: -40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	850	mW
	-plastic medium-shrink (SSOP) -plastic thin-medium-shrink (TSSOP)		600	

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
$V_{IH}$	HIGH level Input voltage	$V_{CC} = 1.2V$	$V_{CC}$			V
		$V_{CC} = 1.8V$	$0.7 \cdot V_{CC}$	0.9		
		$V_{CC} = 2.3$ to $2.7V$	1.7	1.2		
		$V_{CC} = 2.7$ to $3.6V$	2.0	1.5		
$V_{IL}$	LOW level Input voltage	$V_{CC} = 1.2V$			GND	V
		$V_{CC} = 1.8V$		0.9	$0.2 \cdot V_{CC}$	
		$V_{CC} = 2.3$ to $2.7V$		1.2	0.7	
		$V_{CC} = 2.7$ to $3.6V$		1.5	0.8	
$V_{OH}$	HIGH level output voltage	$V_{CC} = 1.8$ to $3.6V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -100\mu A$	$V_{CC} - 0.2$	$V_{CC}$		V
		$V_{CC} = 1.8V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -6mA$	$V_{CC} - 0.4$	$V_{CC} - 0.10$		
		$V_{CC} = 2.3V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -6mA$	$V_{CC} - 0.3$	$V_{CC} - 0.08$		
		$V_{CC} = 2.3V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -12mA$	$V_{CC} - 0.5$	$V_{CC} - 0.17$		
		$V_{CC} = 2.3V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -18mA$	$V_{CC} - 0.6$	$V_{CC} - 0.26$		
		$V_{CC} = 2.7V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -12mA$	$V_{CC} - 0.5$	$V_{CC} - 0.14$		
		$V_{CC} = 3.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -24mA$	$V_{CC} - 1.0$	$V_{CC} - 0.28$		

## 16-bit D-type transparent latch (3-State)

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**DC ELECTRICAL CHARACTERISTICS (Continued)**

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 1.8 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA		GND	0.20	V
		V <sub>CC</sub> = 1.8V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA		0.09	0.30	
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA		0.07	0.20	
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.15	0.40	
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.23	0.60	
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.14	0.40	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA		0.27	0.55	
I <sub>I</sub>	Input leakage current per control pin	V <sub>CC</sub> = 1.8 to 3.6V; V <sub>I</sub> = 5.5V or GND		0.1	5	μA
	Input leakage current per data pin	V <sub>CC</sub> = 1.8 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND		0.1	5	
I <sub>IHZ</sub> /I <sub>ILZ</sub>	Input current for common I/O pins	V <sub>CC</sub> = 1.8 to 2.7V; V <sub>I</sub> = V <sub>CC</sub> or GND		0.1	10	μA
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND		0.1	15	
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 2.7 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND		0.1	10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 1.8 to 2.7V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.2	40	μA
		V <sub>CC</sub> = 2.7 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.2	40	
ΔI <sub>CC</sub>	Additional quiescent supply current given per control pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		150	750	μA
	Additional quiescent supply current given per data I/O pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		150	750	
I <sub>BHL</sub> <sup>2</sup>	Bus hold LOW sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 0.7V	45	–		μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V	75	150		
I <sub>BHH</sub> <sup>2</sup>	Bus hold HIGH sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 1.7V	–45			μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V	–75	–175		
I <sub>BHLO</sub> <sup>2</sup>	Bus hold LOW overdrive current	V <sub>CC</sub> = 2.7V	300			μA
		V <sub>CC</sub> = 3.6V	450			
I <sub>BHHO</sub> <sup>2</sup>	Bus hold HIGH overdrive current	V <sub>CC</sub> = 2.7V	–300			μA
		V <sub>CC</sub> = 3.6V	–450			

**NOTES:**

1. All typical values are at T<sub>amb</sub> = 25°C.
2. Valid for data inputs of bus hold parts.

## 16-bit D-type transparent latch (3-State)

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**AC CHARACTERISTICS FOR  $V_{CC} = 2.3V$  TO  $2.7V$  RANGE AND  $V_{CC} < 2.3V$** GND = 0V;  $t_r = t_f \leq 2.0ns$ ;  $C_L = 30pF$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			$V_{CC} = 2.3$ to $2.7V$			$V_{CC} = 1.8V$			$V_{CC} = 1.2V$	
			MIN	TYP <sup>1, 2</sup>	MAX	MIN	TYP <sup>1</sup>	MAX	TYP	
$t_{PHL}/t_{PLH}$	Propagation delay nDn to nYn	1, 5	1.0	2.1	3.9	1.5	3.2	5.7	8.8	ns
$t_{PHL}/t_{PLH}$	Propagation delay nLE to nYn	2, 5	1.0	2.2	3.9	1.5	3.4	5.9	7.4	ns
$t_{PZH}/t_{PZL}$	3-State output enable time nOE to nYn	4, 5	1.0	2.6	5.2	1.5	4.0	7.3	8.9	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time nOE to nYn	4, 5	1.0	2.2	4.1	1.5	3.2	5.6	8.9	ns
$t_W$	nLE pulse width HIGH	2	3.0	1.0	–	3.5	1.0	–	–	ns
$t_{SU}$	Set-up time nDn to nLE	3	1.0	–0.1	–	1.0	–0.1	–	–	ns
$t_h$	Hold time nDn to nLE	3	1.5	0.2	–	1.2	0.1	–	–	ns

**NOTES:**

- All typical values are measured at  $T_{amb} = 25^\circ C$ .
- Typical value is measured at  $V_{CC} = 2.5V$ .

**AC CHARACTERISTICS FOR  $V_{CC} = 3.0V$  TO  $3.6V$  RANGE AND  $V_{CC} = 2.7V$** GND = 0V;  $t_r = t_f \leq 2.5ns$ ;  $C_L = 50pF$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$			
			MIN	TYP <sup>1, 2</sup>	MAX	MIN	TYP <sup>1</sup>	MAX	
$t_{PHL}/t_{PLH}$	Propagation delay nDn to nYn	1, 5	1.0	2.1	3.3	1.0	2.3	3.7	ns
$t_{PHL}/t_{PLH}$	Propagation delay nLE to nYn	2, 5	1.0	2.2	3.2	1.0	2.2	3.5	ns
$t_{PZH}/t_{PZL}$	3-State output enable time nOE to nYn	4, 5	1.0	2.3	4.2	1.0	2.9	4.9	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time nOE to nYn	4, 5	1.0	2.8	4.1	1.0	3.1	4.7	ns
$t_W$	nLE pulse width HIGH	2	2.5	1.0	–	3.0	1.0	–	ns
$t_{SU}$	Set-up time nDn to nLE	3	1.0	0.0	–	1.0	–0.1	–	ns
$t_h$	Hold time nDn to nLE	3	1.2	0.2	–	1.5	0.4	–	ns

**NOTES:**

- All typical values are measured at  $T_{amb} = 25^\circ C$ .
- Typical value is measured at  $V_{CC} = 3.3V$ .

# 16-bit D-type transparent latch (3-State)

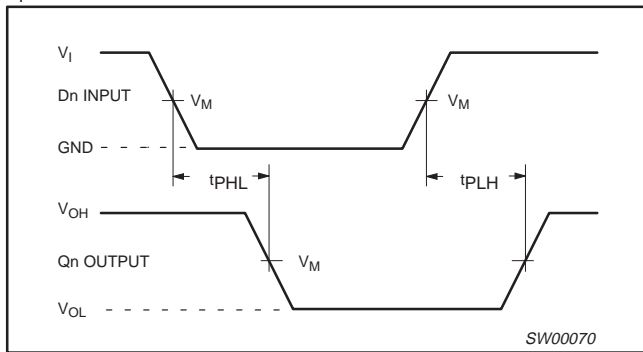
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## AC WAVEFORMS FOR $V_{CC} = 2.3V$ TO $2.7V$ AND $V_{CC} < 2.3V$ RANGE

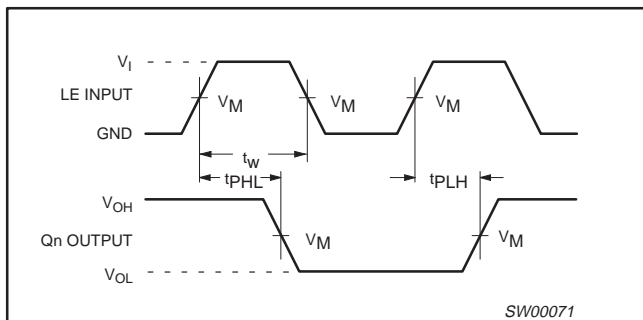
$V_M = 0.5 V_{CC}$   
 $V_X = V_{OL} + 0.15V$   
 $V_Y = V_{OH} - 0.15V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_I = V_{CC}$

## AC WAVEFORMS FOR $V_{CC} = 3.0V$ TO $3.6V$ AND $V_{CC} = 2.7V$ RANGE

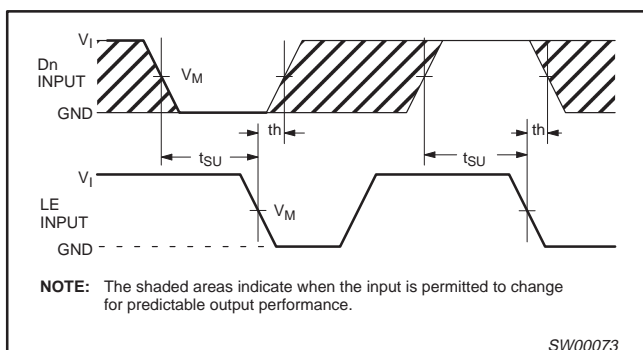
$V_M = 1.5 V$   
 $V_X = V_{OL} + 0.3V$   
 $V_Y = V_{OH} - 0.3V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_I = 2.7V$



Waveform 1. Input (Dn) to output (Qn) propagation delays

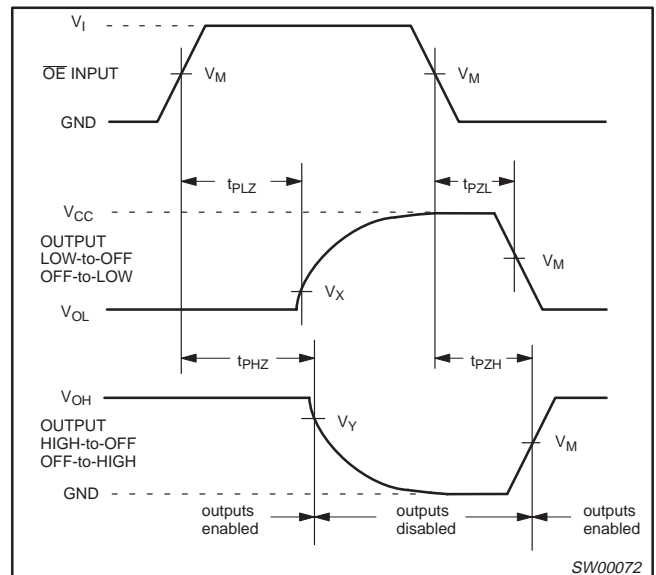


Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays



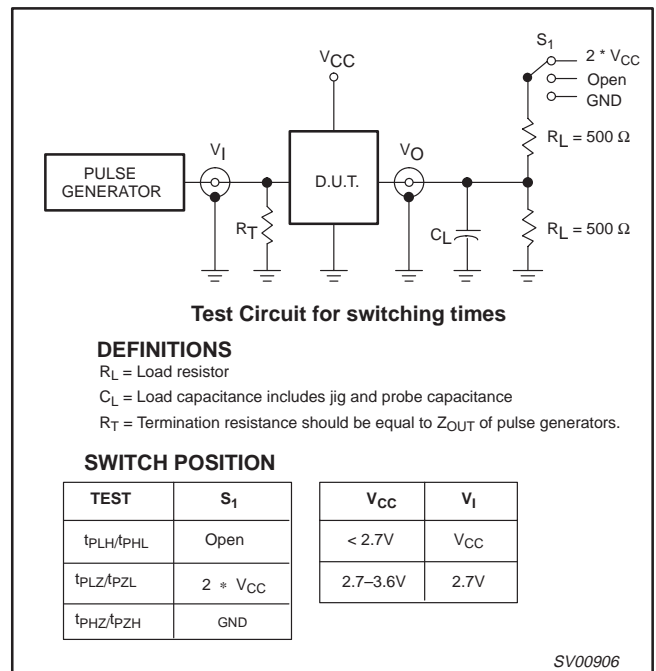
**NOTE:** The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3. Data set-up and hold times for the Dn input to the LE input



Waveform 4. 3-State enable and disable times

## TEST CIRCUIT



Test Circuit for switching times

### DEFINITIONS

$R_L$  = Load resistor  
 $C_L$  = Load capacitance includes jig and probe capacitance  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

### SWITCH POSITION

TEST	S <sub>1</sub>	V <sub>CC</sub>	V <sub>I</sub>
t <sub>PLH</sub> /t <sub>PHL</sub>	Open	< 2.7V	V <sub>CC</sub>
t <sub>PLZ</sub> /t <sub>PZL</sub>	2 * V <sub>CC</sub>	2.7-3.6V	2.7V
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND		

SV00906

Waveform 5. Load circuitry for switching times

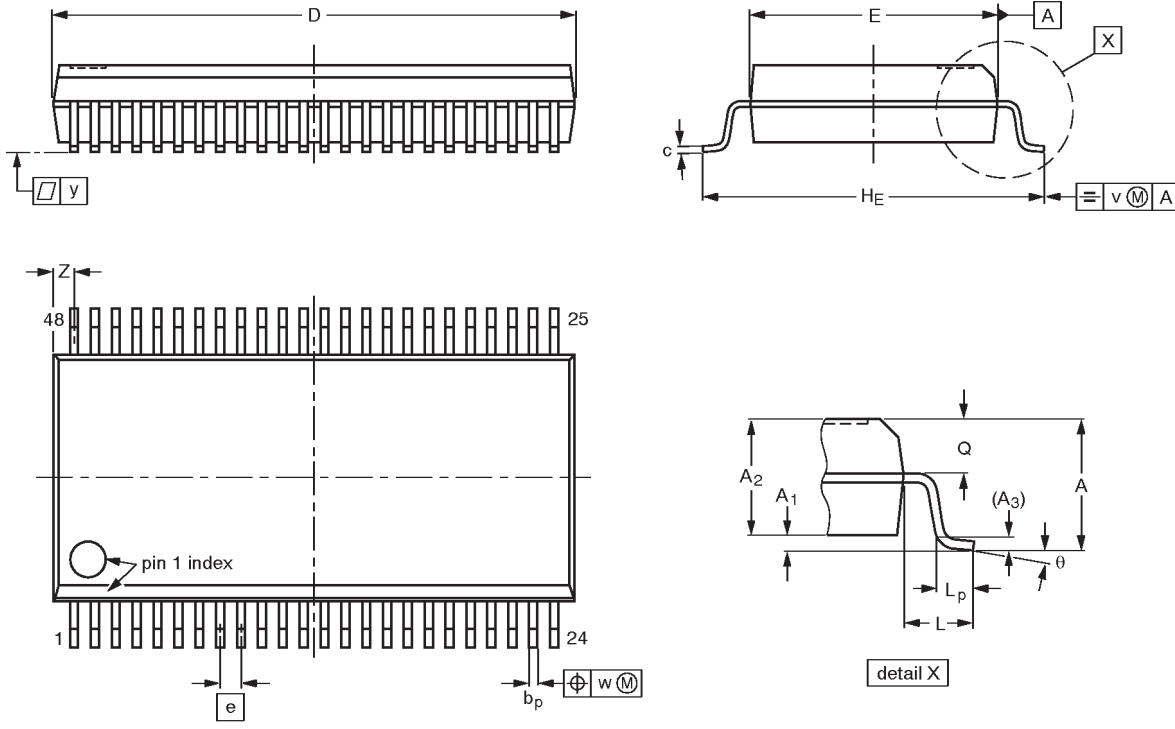


2.5V/3.3V 16-bit D-type transparent latch (3-State)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	$\theta$
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

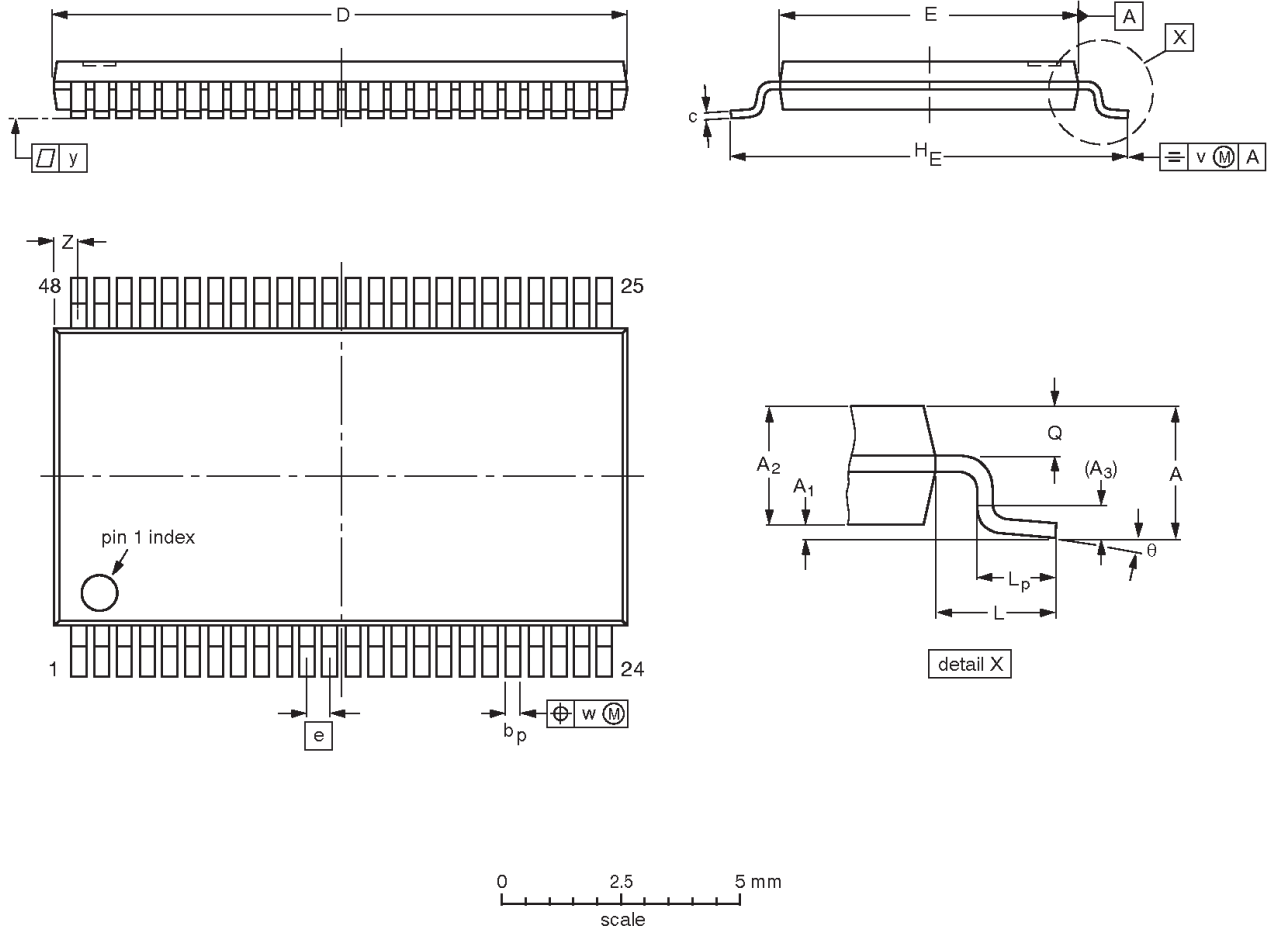
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				93-11-02- 95-02-04

2.5V/3.3V 16-bit D-type transparent latch (3-State)

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153ED				93-02-03 95-02-10

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2.5V/3.3V 16-bit D-type transparent latch (3-State)

74ALVCH16373

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**NOTES**

## 2.5V/3.3V 16-bit D-type transparent latch (3-State)

74ALVCH16373

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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