
2SK2802

Silicon N Channel MOS FET
Low Frequency Power Switching

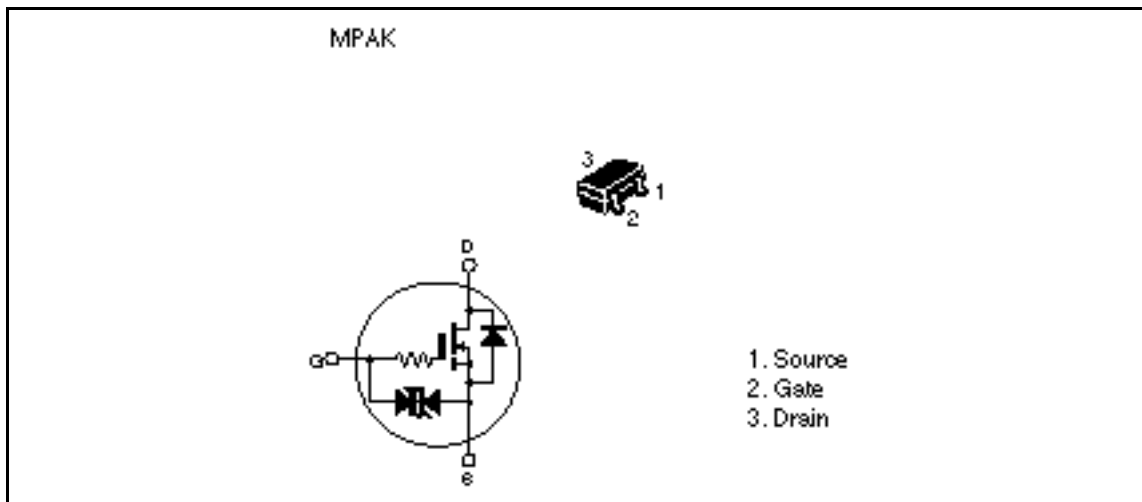
HITACHI

ADE-208-537
1st. Edition

Features

- Low on-resistance
 $R_{DS(on)} = 0.2 \text{ typ. (} V_{GS} = 4 \text{ V, } I_D = 100 \text{ mA)}$
- 2.5V gate drive devices.
- Small package (MPAK)

Outline



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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±10	V
Drain current	I_D	0.5	A
Drain peak current	$I_{D(pulse)}^{*1}$	1.0	A
Channel dissipation	P_{ch}^{*2}	150	mW
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

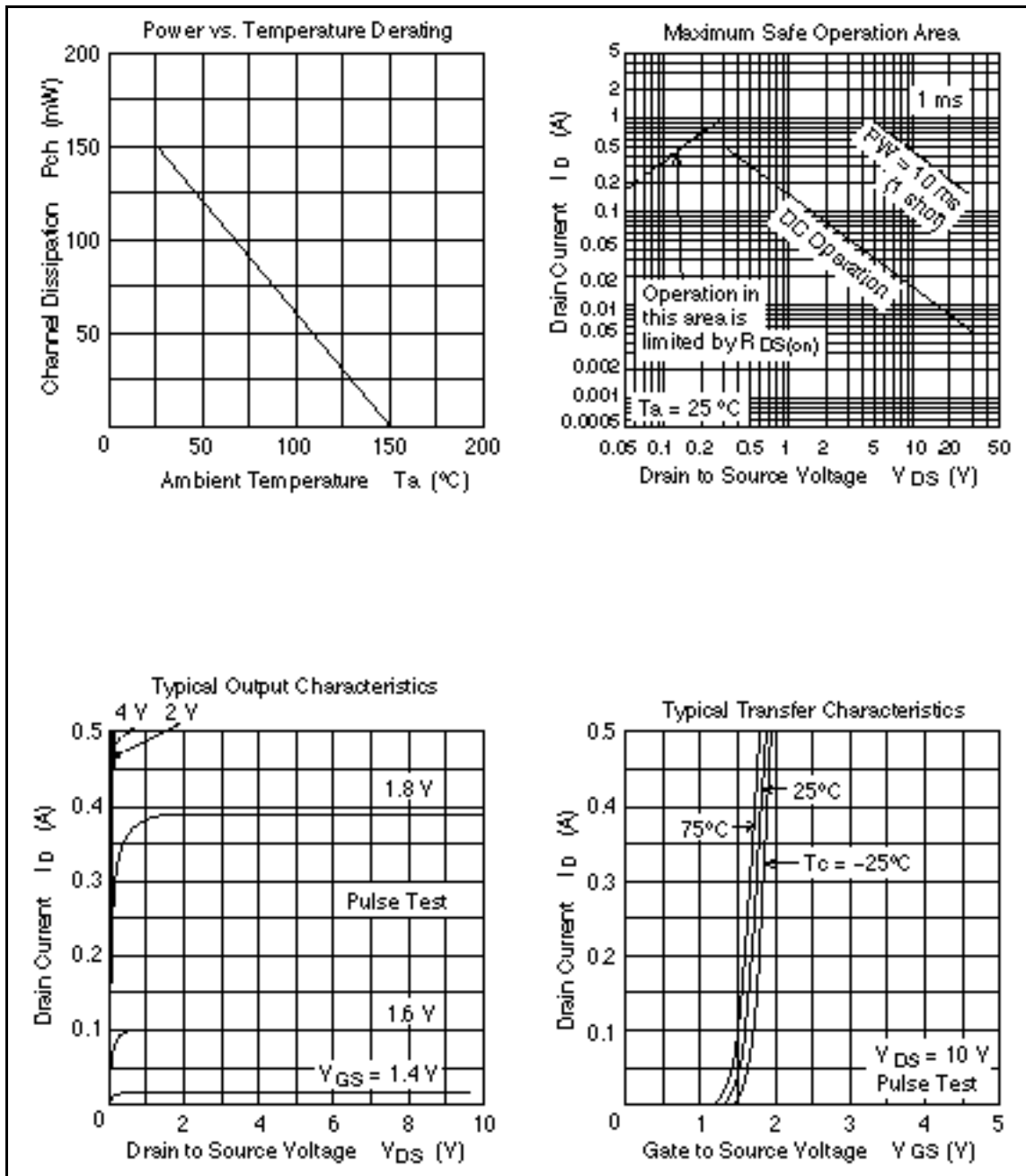
Notes: 1. PW 10µs, duty cycle 1 %
2. Value at Ta = 25 °C

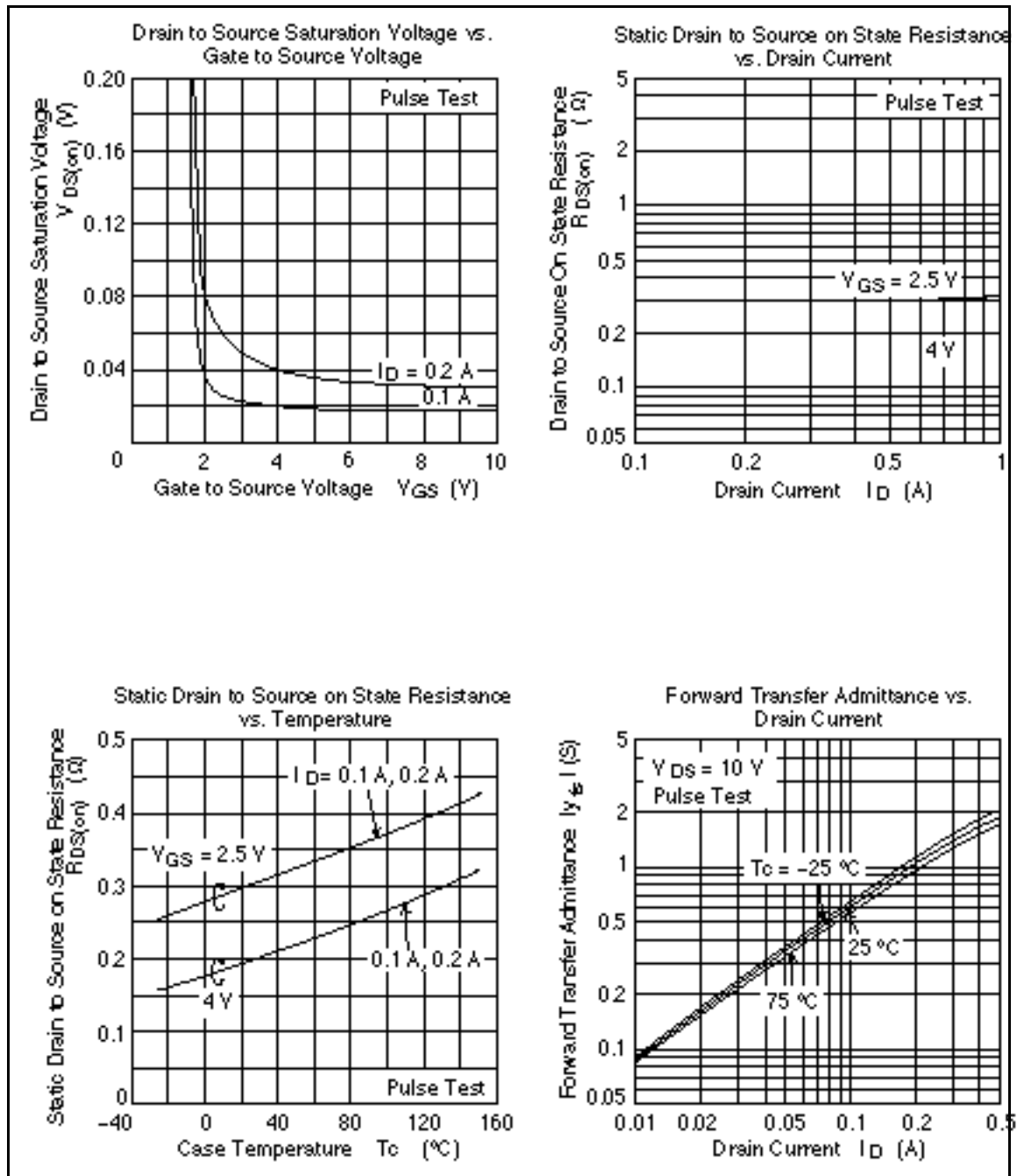
Electrical Characteristics (Ta = 25°C)

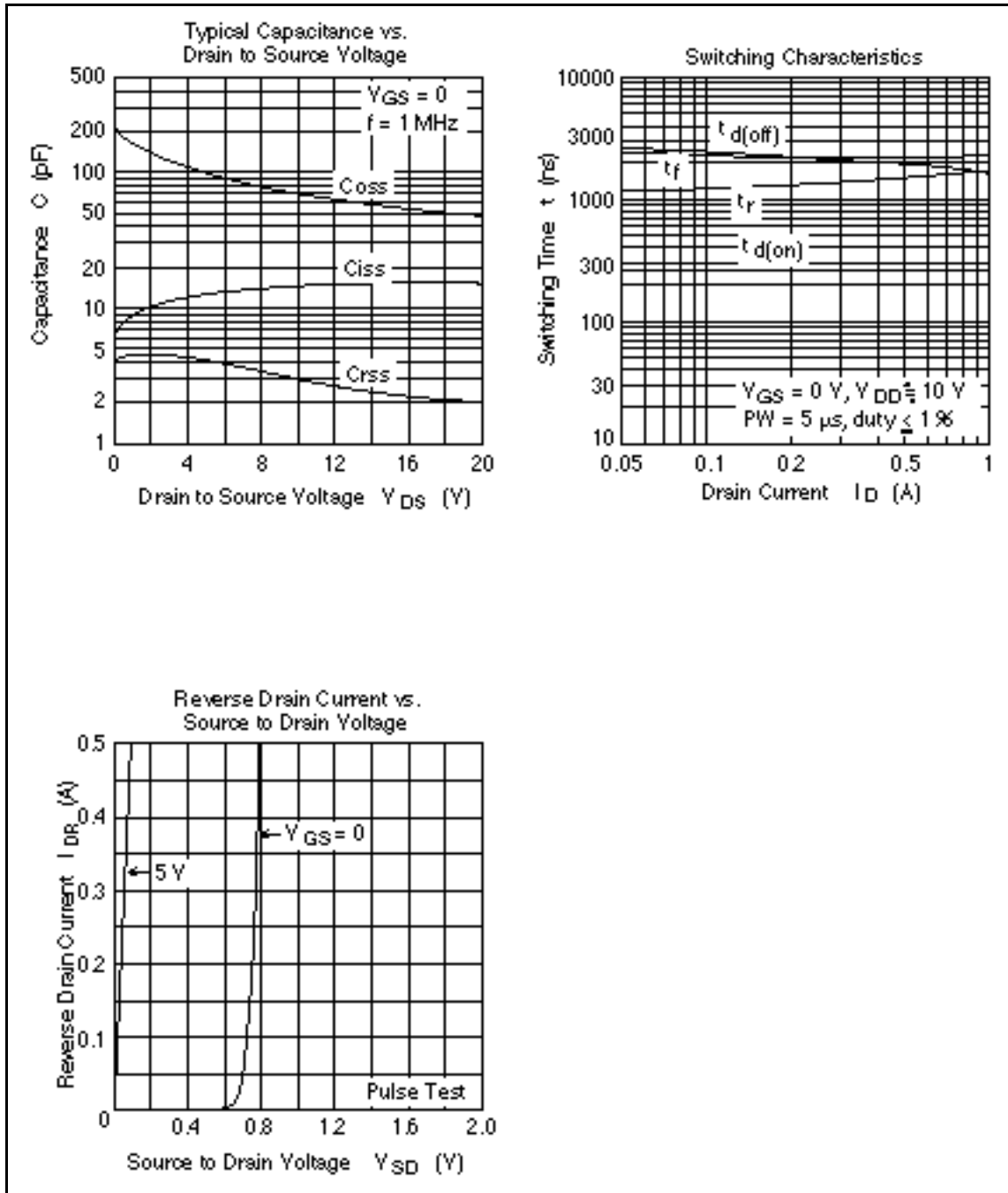
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10\mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	$I_G = \pm 100\mu A, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1.0	µA	$V_{DS} = 30 V, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	µA	$V_{GS} = \pm 6.5 V, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	$I_D = 10\mu A, V_{DS} = 5 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.2	0.28		$I_D = 100 mA$ $V_{GS} = 4V^{*1}$
	$R_{DS(on)}$	—	0.3	0.5		$I_D = 40 mA$ $V_{GS} = 2.5V^{*1}$
Forward transfer admittance	$ y_{fs} $	0.7	1.2	—	S	$I_D = 250 mA$ $V_{DS} = 10V^{*1}$
Input capacitance	C_{iss}	—	14.0	—	pF	$V_{DS} = 10 V$
Output capacitance	C_{oss}	—	68	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	3.0	—	pF	$f = 1 MHz$
Turn-on delay time	$t_{d(on)}$	—	0.27	—	µs	$V_{GS} = 4 V, I_D = 250 mA$
Rise time	t_r	—	1.5	—	µs	$R_L = 40$
Turn-off delay time	$t_{d(off)}$	—	2.2	—	µs	
Fall time	t_f	—	2.15	—	µs	

Notes: 1. Pulse test
2. Marking is "ZV—"

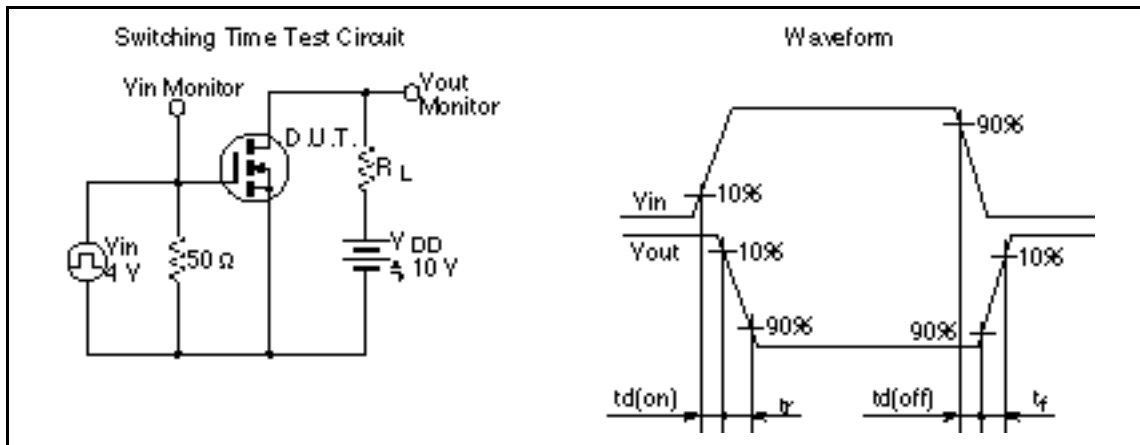
Main Characteristics





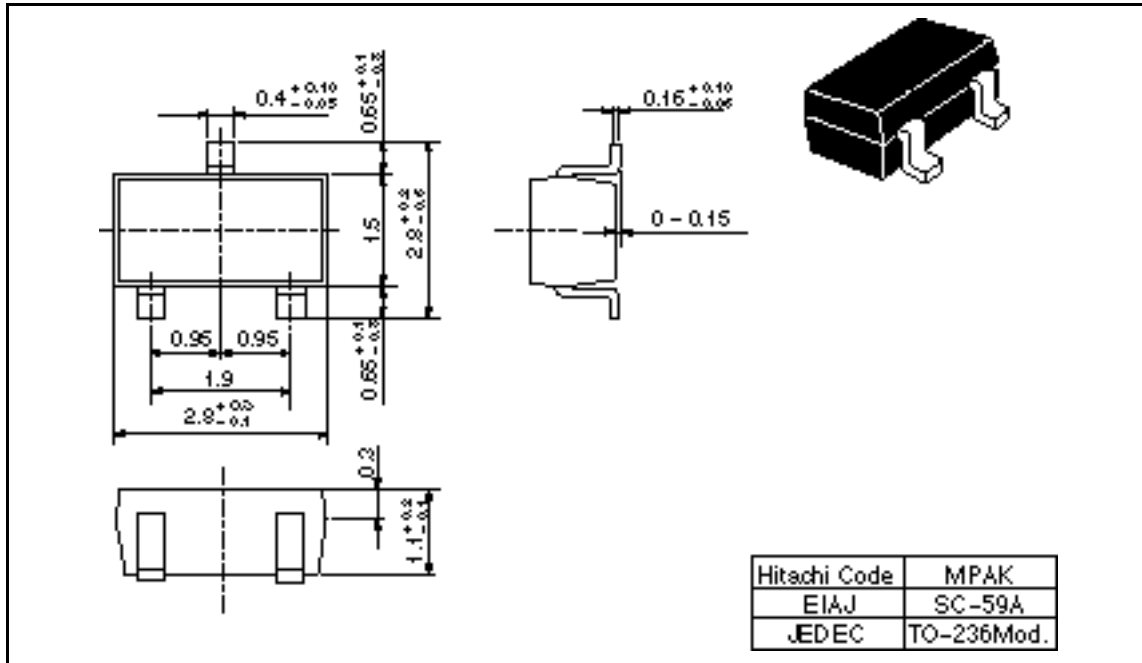


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Package Dimensions

Unit: mm



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