Universal Semiconductor

USH5008
HIGH VOLTAGE 8-CHANNEL ANALOG SWITCH

FEATURES

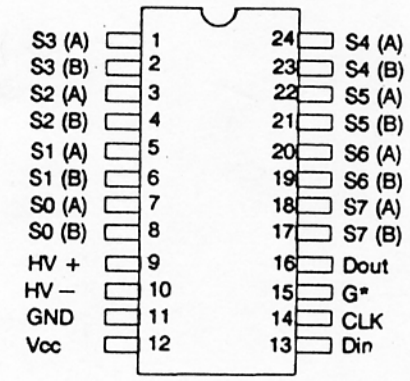
- 180V Analog Signal Switching
- DC to 10MHZ Analog Signal Frequency
- On Resistance 30 ohms
- Turn on / Turn off 2us
- RF Isolation 45 db at 10MHZ
- Push-Pull Driver
- Internal Level Shifters
- Silicon-Gate CMOS Logic
- Low Power Dissipation

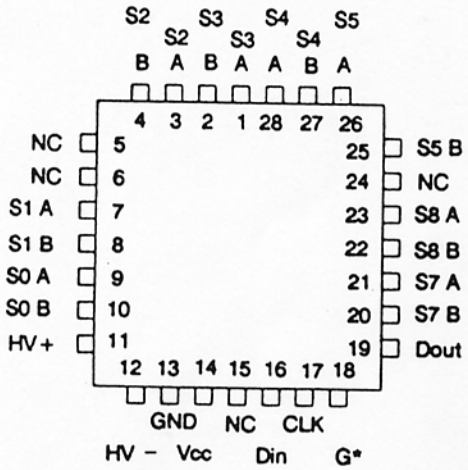
DESCRIPTION

The USH5008 is a High Voltage Integrated Circuit (HIVIC) designed for switching high voltage analog signals. This HIVIC can be used in ultrasound imaging systems and in other applications that require flexible high voltage switching controlled by internal CMOS logic signals.

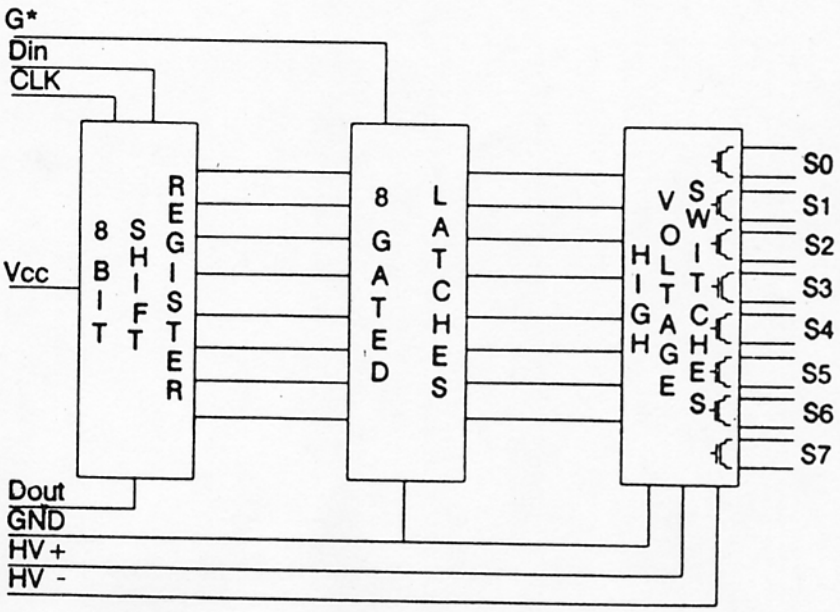
The USH5008 combines high voltage bi-directional DMOS switches with low power CMOS logic to provide efficient control of high voltage analog signals. This HIVIC incorporates high voltage level shifters to interface the high voltage switches to the CMOS logic. The level shifters and push-pull drivers ensure high speed operation with minimal power dissipation.

PIN CONFIGURATION





BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

LEVEL	PARAMETER	SYMBOL	RATING	UNITS
HIGH VOLTAGE	Positive Supply Voltage	HV+	+ 110	V
	Negative Supply Voltage	HV-	-110	V
	Analog Signal Voltage	V_A	- 110 to +90	V
	Analog Signal Current**	I_A	1.5	A
CMOS CONTROL	DC Supply Voltage	V_{CC}	5 to 16	VDC
	DC Supply Current	I_{CC}	20	mA
	DC Input Voltage	V_{IN}	-0.5 to VCC + 0.5	VDC
PACKAGED DEVICE	Operating Temperature	T_{OP}	-55 to +125	°C
	Storage Temperature	T_{ST}	-55 to +150	°C
	Power Dissipation			
	Ceramic Package	P_D	2	W
	Plastic Package	P_D	800	mW

** 2% Duty Cycle; f = 10 MHZ

DC ELECTRICAL CHARACTERISTICS

T_A = 25° C, V_{CC} = 15V, HV + = + 100V, HV- = -100 V (See note 1)

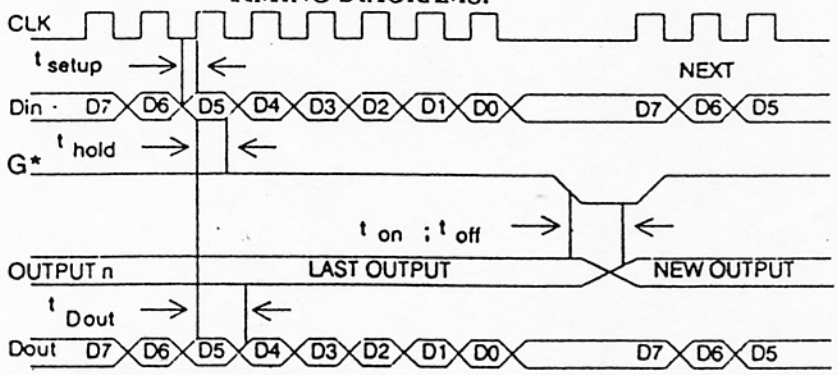
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Analog Voltage Range	V_A	HV + = + 100V	-100	+80	V
On Resistance of Switch	R_{ON}	V_{IN} = 0V; I_{IN} = 10 mA	15	35	Ohms
Change in R_{ON}	ΔR_{ON}	-50V < V_{IN} < + 50 V	_	20	%
Switch Leakage Current	I_L	-80V < V_{IN} < +80V	_	500	mA
Max Switch DC Current***	I_{MAX}	-80V < V_{IN} < + 80V	_	300	mA
Quiescent Current Vcc	I_{CC}	_	_	1.5	mA
Quiescent Current HV + / -	I_{HV+} ; I_{HV-}	_	_	10	uA
Logic High Input Voltage	V_{IH}	V_{CC} = 15 V	12	V_{CC} + 0.5 V	V
Logic Low Input Voltage	V_{IL}	V_{CC} = 15V	-0.5	1.4	V
Logic High Input Current	I_{IH}	V_{IN} = 15 V	_	1	uA
Logic Low Input Current	I_{IL}	V_{IN} = 0V	_	-1	uA
Logic High Output Voltage	V_{OH}	V_{CC} = 15V;' IOUT = 1.8mA	14	_	V
Logic Low Output Voltage	V_{OI}	V_{CC} = 15V; I_{OUT} = -1.8mA	_	0.7	V
Output Current DOUT pin	I_{OUT}	_	-10	+8	mA

NOTE 1 : The recommended method for Power Supply turn-on is as follows:
1. GND ; 2. Vcc + 15V ; 3. HV - -100V ; 4. HV + +100V
***Current is per switch. Not to exceed the maximum power dissipation of package.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Turn-On Time	TON	G* to Output or CLK to Output	–	5	us
Turn-Off Time	TOFF	G* to Output or CLK to Output	–	5	us
Min Setup Time	TSETUP	CLK on DIN	30	–	ns
Min Hold Time	THOLD	DIN to CLK	30	–	ns
Min Pulse Width, G*	TG WIDTH	G* : low	50	–	ns
Clock Pulse Width	TCLK WIDTH	–	50	–	ns
Chan'l SW Capacitance	CS (OFF)	Switch in Off Cond.; F = 1MHZ	–	20	pf
Off Isolation**	–	ZL = 50 ohms	50	–	db
Chan'l to Chan'l Isolation**	–	f = 10MHZ	45	–	db
Max SW Pulse Current	IA	1% duty cycle f = 10KHZ	–	1.5	A
Max Clock Frequency	FCLK	–	–	10	MHZ

** Plastic DIP Package

TIMING DIAGRAMS:



DESCRIPTION OF OPERATION

The USH5008 is a High Voltage Integrated Circuit (HIVIC) that contains eight independent high voltage bi-directional switches and the CMOS logic necessary to interface them to a CMOS environment. This HIVIC is designed to switch 180V analog signals into capacitive loads, and it is designed to conduct current pulses of 1A.

The switches (S0-7) are controlled by the serial data on DIN, the shift register clock input (CLK), and the data transfer enable (G*). (See Tables 1 and 2, and timing diagrams). Serial data on line DIN is clocked into the eight-staged static shift registers.

The data in the shift register is transferred to the latches by enable G*. When G* is low, the shift register data flows through the latch and controls the state of the switch.

TABLE 1 PIN DESCRIPTIONS

PIN	DESCRIPTION
D_{IN}	Serial Data Input to Shift Register
CLK	Serial Shift Clock
G*	Parallel Transfer Enable from Shift Register to Latches
D_{out}	Serial Data Out of Eighth Stage of Shift Register
S0-7 (A,B)	Eight Pairs of High Voltage Lines for Analog Signal Switching
HV+	Positive High Voltage Supply for the Level Shift Circuits
HV–	Negative High Voltage Supply for the Level Shift Circuits
V_{CC}	+15V Logic Supply Pin
GND	Ground Reference Pin for both the Logic Supply and the High Voltage Supply

NOTES:

1) The eight switches operate independently.
2) Serial data is clocked in on the L / H transition of CLK.
3) The switches go to a state retaining their present condition at the rising edge of G*. When G* is low, the shift register data flows through the latch.
4) DOUT is high when switch 7 is ON.
5) Shift register clocking has no effect on the switch states if G* is high.

TABLE 2 TRUTH TABLE

D1	D2	D3	D4	D5	D6	D7	G*	S0	S1	S2	S3	S4	S5	S6	S7
							L	OFF							
H							L	ON							
L							L		OFF						
H							L		ON						
	L						L			OFF					
	H						L			ON					
		L					L				OFF				
		H					L				ON				
			L				L					OFF			
			H				L					ON			
				L			L						OFF		
				H			L						ON		
					L		L							OFF	
					H		L							ON	
						L	L								OFF
						H	L								ON
X	X	X	X	X	X	X	H	HOLD PREVIOUS STATE							

ORDERING INFORMATION

PRODUCT NO.	PACKAGE	TEMP RANGE
USH5008-AI-P24	24 Pin Plastic Dip	0 to 70 °C
USH5008-AI-K28	28 Pin PLCC	0 to 70 °C
USH5008-AI-C24	24 PIN Cerdip	-25 to + 85 °C
USH5008-AM-C24	24 Pin Cerdip	-55 to + 125 °C
USH5008-AI-L28	28 Pin Ceramic Chip Carrier	-25 to +85 °C
USH5008-AM-L28	28 Pin Ceramic Chip Carrier	-55 to + 125°C

MIL-STD-883C Processing Available