

September 2001

DESCRIPTION

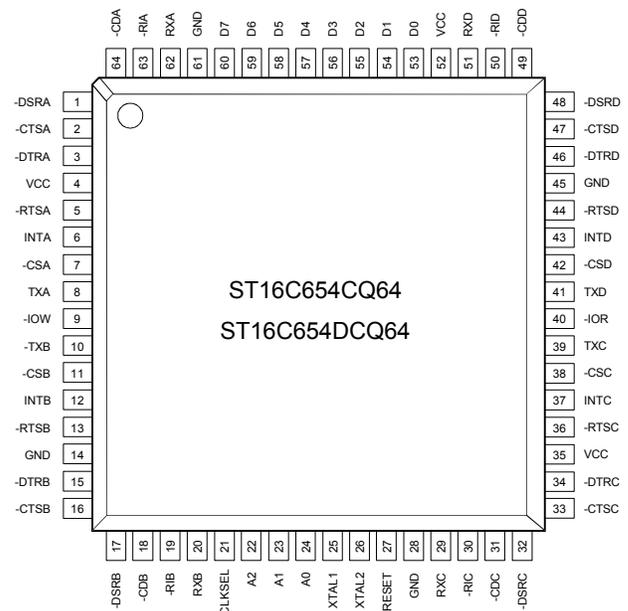
The ST16C654 *1 is a universal asynchronous receiver and transmitter (UART) with a dual foot print interface compatible with the ST16C554 and ST68C554. The 654 is an enhanced UART with 64 byte FIFO's, automatic hardware/software flow control, and data rates up to 1.5Mbps. Onboard status registers provide the user with error indications and operational status, modem interface control. System interrupts may be tailored to meet user requirements. An internal loop-back capability allows onboard diagnostics. The 654 is available in 64 pin TQFP, 68 pin PLCC, and 100 pin QFP packages. The 64 pin package offers the 16 interface mode which is compatible with the industry standard ST16C554. The 68 and 100 pin packages offer an additional 68 mode which allows easy integration with Motorola, and other popular microprocessors. The ST16C654CQ64 (64 pin) offers three state interrupt control while the ST16C654DCQ64 provides constant active interrupt outputs. The 64 pin devices do not offer TXRDY/RXRDY outputs. The 100 pin packages offer faster channel status access by providing separate outputs for TXRDY and RXRDY, offer separate Infrared TX outputs and a separate clock for channel C (CHCCLK) that can be used as a musical instrument clock input. The 654 combines the package interface modes of the 16C454/554 and 68C454/554 series on a single integrated chip.

Note *1: Covered by US Patents #5,649,122 and 5,949,787

FEATURES

- Each channel can be controlled independently.
- Compatibility with the Industry Standard ST16C454/554, ST68C454/554, TL16C554/754
- 1.5 Mbps transmit/receive operation (24MHz)
- 64 byte transmit FIFO
- 64 byte receive FIFO with error flags
- Four selectable Transmit/Receive FIFO interrupt trigger levels
- Automatic software/hardware flow control
- Programmable Xon/Xoff characters
- Software selectable Baud Rate Generator pre-scaleable clock rates of 1X, 4X.
- Standard modem interface or infrared IrDA encoder/decoder interface
- Independent clock input for channel C on 100 pin packages
- 100 pin package offers internal register FIFO status monitoring and separate IrDA TX outputs
- Sleep mode (200µA stand-by)

64 Pin TQFP Package



ORDERING INFORMATION

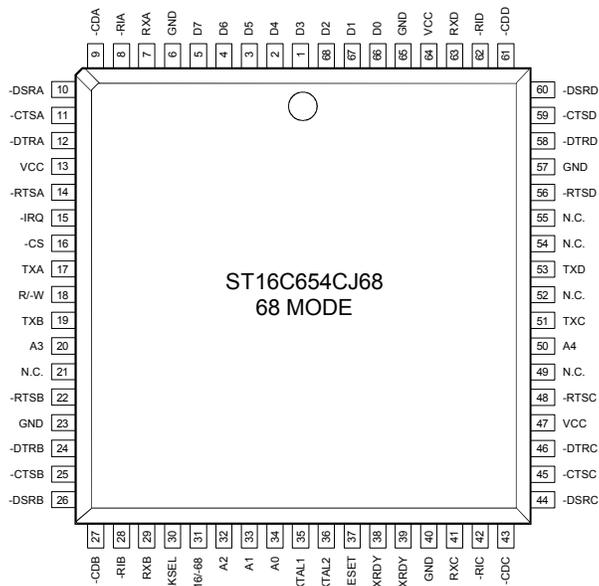
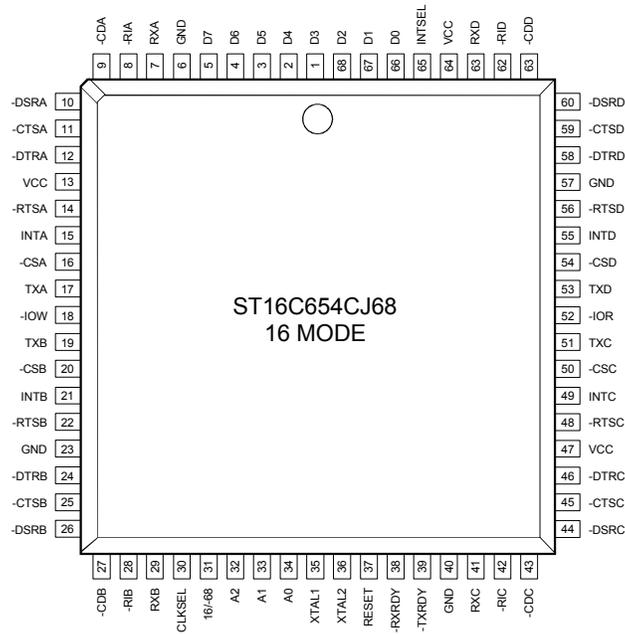
Part number	Pins	Package	Operating temperature	Part number	Pins	Package	Operating temperature
ST16C654CJ68	68	PLCC	0° C to + 70° C	ST16C654IJ68	68	PLCC	-40° C to + 85° C
ST16C654CQ64	64	TQFP	0° C to + 70° C	ST16C654IQ64	64	TQFP	-40° C to + 85° C
ST16C654DCQ64	64	TQFP	0° C to + 70° C	ST16C654DIQ64	64	TQFP	-40° C to + 85° C
ST16C654CQ100	100	QFP	0° C to + 70° C	ST16C654IQ100	100	QFP	-40° C to + 85° C

ST16C654/654D



Figure 1, Package Descriptions

68 Pin PLCC Package



100 Pin QFP Package

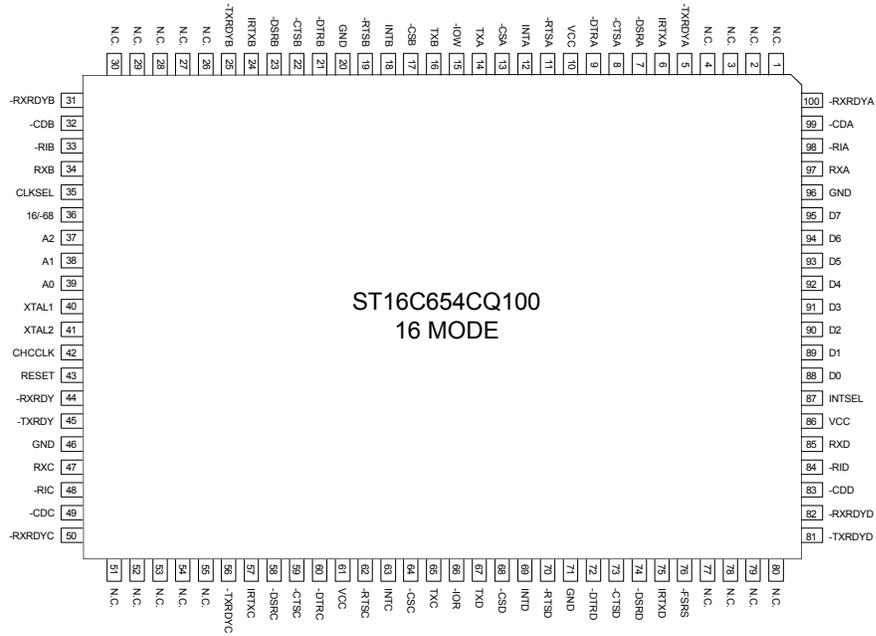


Figure 2, Block Diagram 16 Mode (16/-68 Pin = VCC)

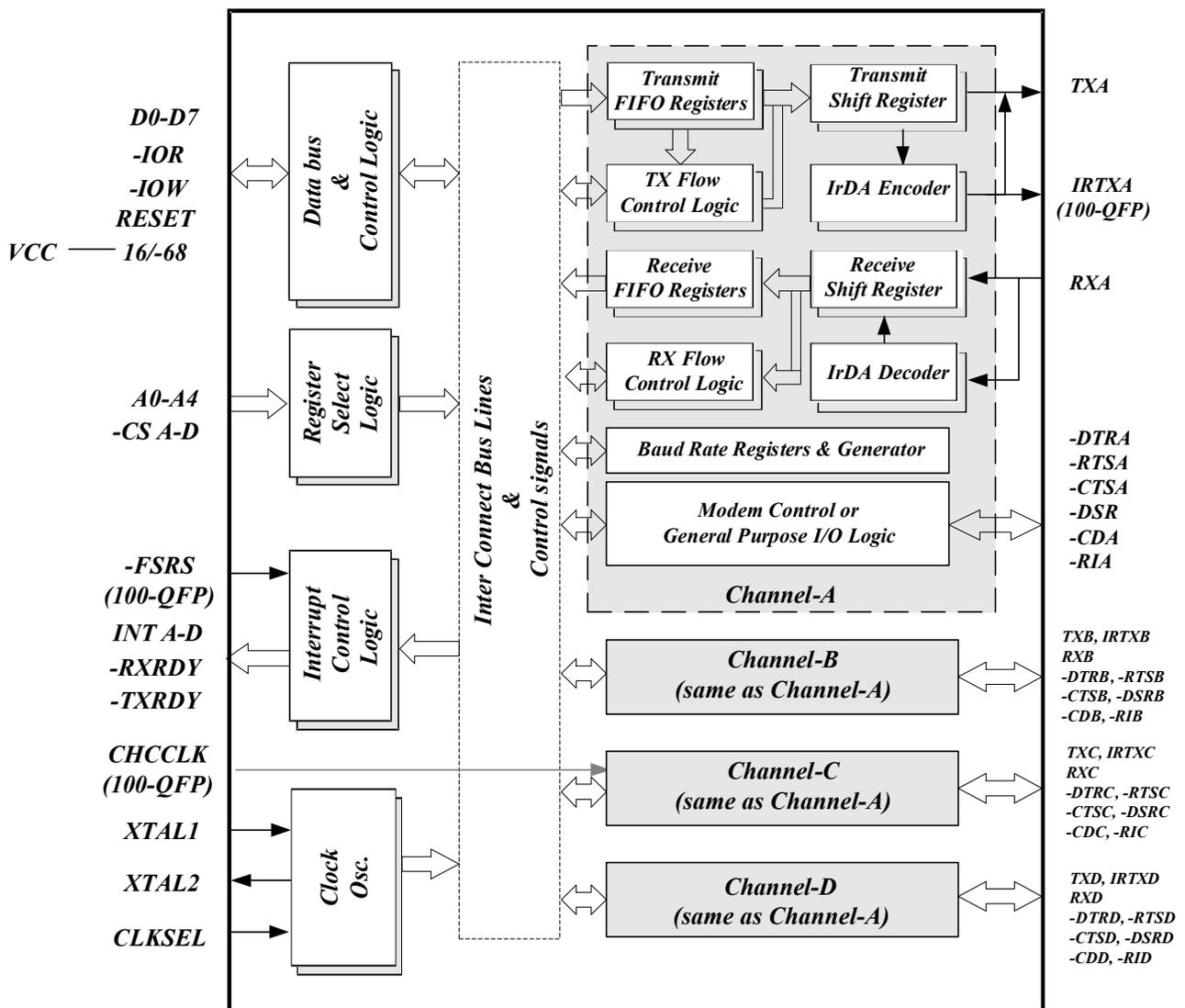
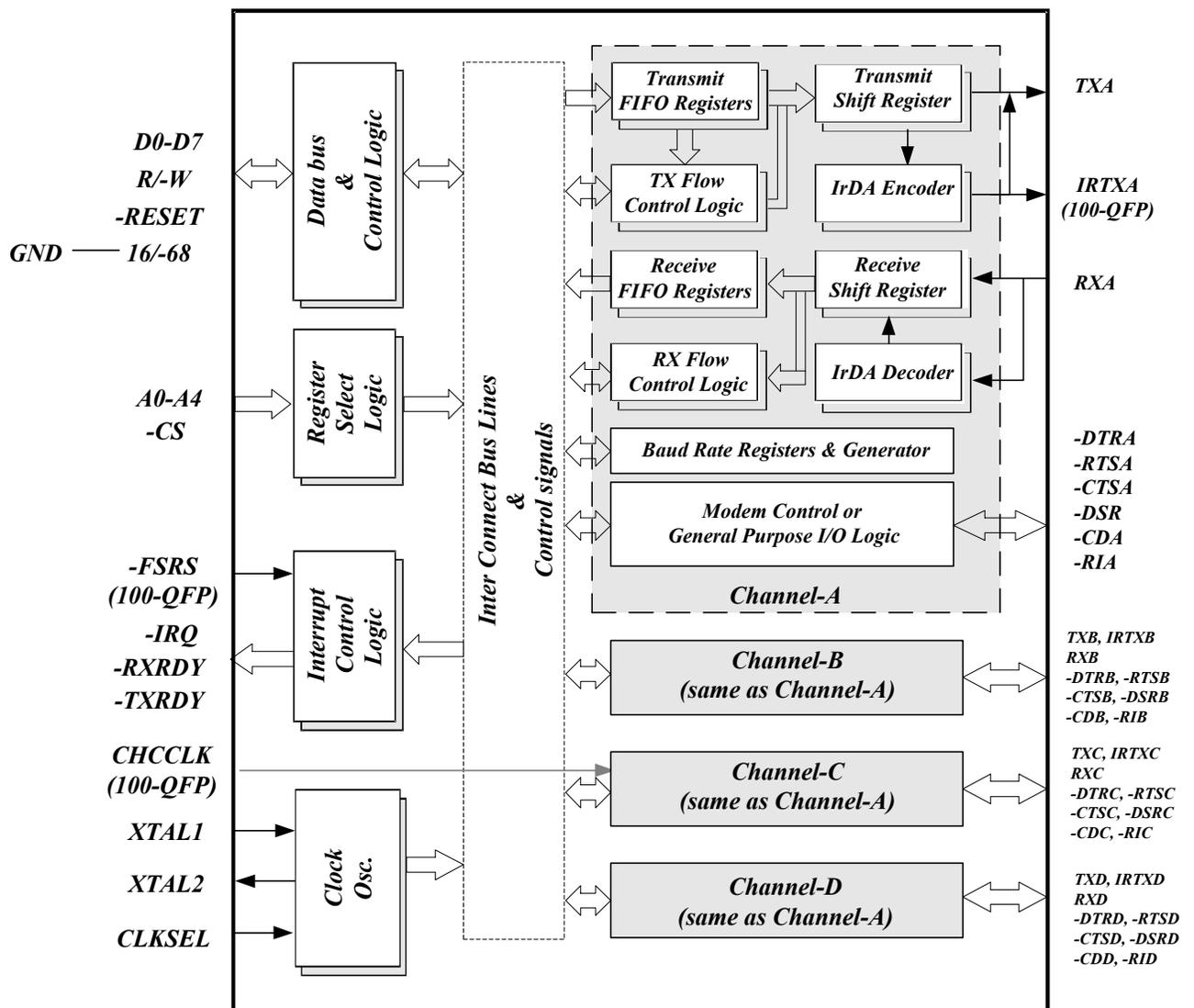


Figure 3, Block Diagram 68 Mode (16/-68 Pin = GND)



SYMBOL DESCRIPTION

Symbol	Pin			Signal type	Pin Description
	68	100	64		
16/-68	31	36	-	I	16/68 Interface Type Select (input with internal pull-up). - This input provides the 16 (Intel) or 68 (Motorola) bus interface type select. The functions of -IOR, -IOW, INT A-D, and -CS A-D are re-assigned with the logical state of this pin. When this pin is a logic 1, the 16 mode interface 16C554 is selected. When this pin is a logic 0, the 68 mode interface (68C554) is selected. When this pin is a logic 0, -IOW is re-assigned to R/-W, RESET is re-assigned to -RESET, -IOR is not used, and INT A-D(s) are connected in a WIRE-OR™ configuration. The WIRE-OR outputs are connected internally to the open drain IRQ signal output. This pin is not available on 64 pin packages which operate in the 16 mode only.
A0	34	39	24	I	Address-0 Select Bit. Internal registers address selection in 16 and 68 modes.
A1	33	38	23	I	Address-1 Select Bit. Internal registers address selection in 16 and 68 modes.
A2	32	37	22	I	Address-2 Select Bit. - Internal registers address selection in 16 and 68 modes.
CLKSEL	30	35	21	I	Clock Select. - The pre-scaleable clock to the Baud Rate Generator is selected by this pin upon power-up. The div-by-1 clock is selected when CLKSEL is a logic 1 (connected to VCC) or the div-by-4 is selected when CLKSEL is a logic 0 (connected to GND). MCR bit-7 can override the state of this pin following reset or initialization (see MCR bit-7).
-FSRS	-	76	-	I	FIFO Status Register Select (active low) - This feature is available on 100 pin QFP packages only. The contents of the FIFORDY Register is read when this pin is a logic 0. However it should be noted, D0-D3 will contain the inverted logic states of TXRDY A-D, and D4-D7 the logic states (un-inverted) of RXRDY A-D. See Table 6.
D0-D2 D3-D7	66-68 1-5	88-90 91-95	53-55 56-60	I/O	Data Bus (Bi-directional) - These pins are the eight bit, three state data bus for transferring information to or from the

SYMBOL DESCRIPTION

Symbol	Pin			Signal type	Pin Description
	68	100	64		
GND	6,23	96,20	14,28	Pwr	controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream. Signal and power ground.
GND	40,57	46,71	45,61		
IRTX A-B	-	6,24	-	O	Infrared Transmit Data Output (IrDA) - This function is associated with 100 pin packages only. These pins provide separate infrared IrDA TX outputs for UART channel's (A-D). The serial infrared IRTX data is transmitted via these pins with added start, stop and parity bits. The IRTX signal will be a logic 0 during reset, idle (no data), or when the transmitter is disabled. MCR bit-6 selects the standard modem or infrared interface.
IRTX C-D	-	57,75	-		
CHCCLK	-	42	-	I	Channel C Clock Input- This input provides the clock for UART channel C. An external 16X baud clock or the crystal oscillator's output, XTAL2, must be connected to this pin for normal operation. This input may also be used with MIDI (Music Instrument Digital Interface) applications when an external MIDI clock is provided.
INTSEL	65	87	-	I	Interrupt Select. (active high, with internal pull-down) - This function is associated with the 16 mode only. When the 16 mode is selected, this pin can be used in conjunction with MCR bit-3 to enable or disable the three state interrupts, INT A-D or override MCR bit-3 and force continuous interrupts. Interrupt outputs are enabled continuously by making this pin a logic 1. Making this pin a logic 0 allows MCR bit-3 to control the three state interrupt output: enable outputs when MCR bit-3 is set to a logic 1 and tri-state outputs when MCR bit-3 is set to a logic 0. Due to pin limitations on 64 pin packages, this pin is not available. To cover this limitation, two 64 pin TQFP package versions are offered. The ST16C654DCQ64 operates in the continuous interrupt enable mode by bonding this pin to VCC internally. The ST16C654CQ64 operates with MCR bit-3 control by bonding this pin to GND. This pin should be left open or tied to GND in the 68 mode.

SYMBOL DESCRIPTION

Symbol	Pin			Signal type	Pin Description
	68	100	64		
-RXRDY	38	44	-	O	Receive Ready (active low) - This function is associated with 68 and 100 pin packages only. -RXRDY contains the wire "OR-ed" status of all four receive channel FIFO's, RXRDY A-D. A logic 0 indicates receive data ready status, i.e. the RHR is full or the FIFO has one or more RX characters available for unloading. This pin goes to a logic 1 when the FIFO/RHR is full or when there are no more characters available in either the FIFO or RHR. The 100 pin package provides both the combined wire "or'ed" output and individual channel RXRDY-A-D outputs. RXRDY A-D is discussed in a following paragraph.
-TXRDY	39	45	-	O	Transmit Ready (active low) - This function is associated with 68 and 100 pin packages only. -TXRDY contains the wire "OR-ed" status of all four transmit channel FIFO's, TXRDY A-D. A logic 0 indicates a buffer ready status, i.e., at least one location is empty and available in one of the TX channels (A-D). This pin goes to a logic 1 when all four channels have no more empty locations in the TX FIFO or THR. The 100 pin chip-sets provide both the combined wire "or'ed" output and individual channel TXRDY-A-D outputs. TXRDY A-D is discussed in a following paragraph.
VCC VCC	13 47,64	10 61,86	4, 35,52	I	Power supply inputs.
XTAL1	35	40	25	I	Crystal or External Clock Input - Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit (see figure 8). Alternatively, an external clock can be connected to this pin to provide custom data rates (see Baud Rate Generator Programming and optional MIDCLK).
XTAL2	36	41	26	O	Output of the Crystal Oscillator or Buffered Clock - (See also XTAL1). Crystal oscillator output or buffered clock output.
-CD A-B -CD C-D	9,27 43,61	99,32 49,83	64,18 31,49	I	Carrier Detect (active low) - These inputs are associated with

SYMBOL DESCRIPTION

Symbol	Pin			Signal type	Pin Description
	68	100	64		
-CTS A-B -CTS C-D	11,25 45,59	8,22 59,73	2,16 33,47	I	individual UART channels A through D. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel. If not connected to a modem, these inputs can be used as general purpose inputs. Clear to Send (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on the -CTS pin indicates the modem or data set is ready to accept transmit data from the 654. Status can be tested by reading MSR bit-4. This pin only affects the transmit and receive operations when Auto CTS function is enabled via the Enhanced Feature Register (EFR) bit-7, for hardware flow control operation. If not connected to a modem, these inputs can be used as general purpose inputs.
-DSR A-B -DSR C-D	10,26 44,60	7,23 58,74	1,17 32,48	I	Data Set Ready (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation. If not connected to a modem, these inputs can be used as general purpose inputs.
-DTR A-B -DTR C-D	12,24 46,58	9,21 60,72	3,15 34,46	O	Data Terminal Ready (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates that the 654 is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR bit-0 will set the -DTR output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR bit-0, or after a reset. This pin has no effect on the UART's transmit or receive operation. If not connected to a modem, these outputs can be used as general purpose outputs.
-RI A-B -RI C-D	8,28 42,62	98,33 48,84	63,19 30,50	I	Ring Indicator (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on this pin

SYMBOL DESCRIPTION

Symbol	Pin			Signal type	Pin Description
	68	100	64		
-RTSA-B -RTSC-D	14,22 48,56	11,19 62,70	5,13 36,44	O	indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt. If not connected to a modem, these inputs can be used as general purpose inputs. Request to Send (active low) - These outputs are associated with individual UART channels, A through D. A logic 0 on the -RTS pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register (MCR bit-1) will set this pin to a logic 0 indicating data is available. After a reset this pin will be set to a logic 1. This pin only affects the transmit and receive operations when Auto RTS function is enabled via the Enhanced Feature Register (EFR) bit-6, for hardware flow control operation. If not connected to a modem, these outputs can be used as general purpose outputs.
RX/IRRX A-B RX/IRRX C-D	7,29 41,63	97,34 47,85	62,20 29,51	I	Receive Data Input RX/IRRX A-D. - These inputs are associated with individual serial channel data to the ST16C654. Two user selectable interface options are available. The first option supports the standard modem interface. The second option provides an Infrared decoder interface, see figures 2/3. When using the standard modem interface, the RX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. The inactive state (no data) for the Infrared decoder interface is a logic 0. MCR bit-6 selects the standard modem or infrared interface. During the local loop-back mode, the RX input pin is disabled and TX data is internally connected to the UART RX Input, internally.
TX/IRTX A-B TX/IRTX C-D	17,19 51,53	14,16 65,67	8,10 39,41	O	Transmit Data - These outputs are associated with individual serial transmit channel data from the 654. Two user selectable interface options are available. The first user option supports a standard modem interface. The second option provides an Infrared encoder interface, see figures 2 and 3. When using the standard modem interface, the TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. The inactive state (no data) for the Infrared encoder/ decoder interface is a Logic 0. MCR bit-6

SYMBOL DESCRIPTION

Symbol	Pin			Signal type	Pin Description
	68	100	64		
RESET/ -RESET	37	43	27	I	selects the standard modem or infrared interface. During the local loop-back mode, the TX input pin is disabled and TX data is internally connected to the UART RX Input. Reset. - In the 16 mode a logic 1 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See ST16C654 External Reset Conditions for initialization details.) When 16/68 is a logic 0 (68 mode), this pin functions similarly but, as an inverted reset interface signal, -RESET.
-CS A-B -CS C-D	16,20 50,54	13,17 64,68	7,11 38,42	I	Chip Select A, B, C, D (active low) - This function is associated with the 16 mode only, and for individual channels, "A" through "D." When in 16 Mode, these pins enable data transfers between the user CPU and the ST16C654 for the channel(s) addressed. Individual UART sections (A, B, C, D) are addressed by providing a logic 0 on the respective -CS A-D pin. When the 68 mode is selected, the functions of these pins are reassigned. 68 mode functions are described under the their respective name/pin headings.
INT A-B INT C-D	15,21 49,55	12,18 63,69	6,12 37,43	O	Interrupt A, B, C, D (active high) - This function is associated with the 16 mode only. These pins provide individual channel interrupts, INT A-D. INT A-D are enabled when MCR bit-3 is set to a logic 1, interrupts are enabled in the interrupt enable register (IER), and when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected. When the 68 mode is selected, the functions of these pins are reassigned. 68 mode functions are described under the their respective name/pin headings.
-IOR	52	66	40	I	Input/Output Read. (active low Strobe) - This function is associated with the 16 mode only. A logic 0 transition on this pin will load the contents of an Internal register defined by address bits A0-A2 onto the ST16C654 data bus (D0-D7) for access by an external CPU. This pin is disabled in the 68

SYMBOL DESCRIPTION

Symbol	Pin			Signal type	Pin Description
	68	100	64		
-IOW	18	15	9	I	mode. Input/Output Write. (active low strobe) - This function is associated with the 16 mode only. A logic 0 transition on this pin will transfer the contents of the data bus (D0-D7) from the external CPU to an internal register that is defined by address bits A0, A1 and A2. When the 68 mode is selected, this pin functions as R/-W, see definition under R/-W.
A3-A4	20,50	17,64	-	I	Address 3-4 Select Bits. - When the 68 mode is selected, these pins are used to address or select individual UART's (providing -CS is a logic 0). In the 16 mode, these pins are reassigned as chip selects, see -CSB and -CSC. These pins are not available on 64 pin packages which operate in the 16 mode only.
-CS	16	13	-	I	Chip Select. (active low) - In the 68 mode, this pin functions as a multiple channel chip enable. In this case, all four UART's (A-D) are enabled when the -CS pin is a logic 0. An individual UART channel is selected by the data contents of address bits A3-A4. When the 16 mode is selected (68/100 pin devices), this pin functions as -CSA, see definition under -CS A-B. This pin is not available on 64 pin packages which operate in the 16 mode only.
-IRQ	15	12	-	O	Interrupt Request or Interrupt "A" (open-drain output) - This function is associated with the 68 mode only. In the 68 mode, interrupts from UART channels A-D are WIRE-OR'ed" internally to function as a single IRQ interrupt. This pin transitions to a logic 0 (if enabled by the interrupt enable register) whenever a UART channel(s) requires service. Individual channel interrupt status can be determined by addressing each channel through its associated internal register, using -CS and A3-A4. In the 68 mode an external pull-up resistor must be connected between this pin and VCC. The function of this pin changes to INTA when operating in the 16 mode, see definition under INTA.
R/-W	18	15	-	I	Read/Write Strobe (active low) - This function is associated with the 68 mode only. This pin provides the combined

SYMBOL DESCRIPTION

Symbol	Pin			Signal type	Pin Description
	68	100	64		
-RXRDY A-B -RXRDY C-D	- -	100,31 50,82	-	O	<p>functions for Read or Write strobes. A logic 1 to 0 transition transfers the contents of the CPU data bus (D0-D7) to the register selected by -CS and A0-A4. Similarly a logic 0 to 1 transition places the contents of a 654 register selected by -CS and A0-A4 on the data bus, D0-D7, for transfer to an external CPU.</p> <p>(EMSR register bit-3 = 0) Receive Ready A-D (active low) - This function is associated with 100 pin packages only. This function provides the RX FIFO/RHR status for individual receive channels (A-D). A logic 0 indicates there is receive data to read/unload, i.e., receive ready status with one or more RX characters available in the FIFO/RHR. This pin is a logic 1 when the FIFO/RHR is empty or when the programmed trigger level has not been reached.</p>
-TXRDY A-B -TXRDY C-D	- -	5,25 56,81	-	O	<p>(EMSR register bit-2 = 0) This function is associated with 100 pin packages only. These outputs provide the TX FIFO/THR status for individual transmit channels (A-D). This pin goes to a logic 0 when the FIFO is empty (non-DMA mode) or when the FIFO falls below the trigger level (DMA mode).</p>

GENERAL DESCRIPTION

The 654 provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The ST16C654 represents such an integration with greatly enhanced features. The 654 is fabricated with an advanced CMOS process to achieve low drain power and high speed requirements.

The 654 is an upward solution that provides 64 bytes of transmit and receive FIFO memory, instead of 16 bytes provided in the 16/68C554, or none in the 16/68C454. The 654 is designed to work with high speed modems and shared network environments, that require fast data processing time. Increased performance is realized in the 654 by the larger transmit and receive FIFO's. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C554 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 64 byte FIFO in the 654, the data buffer will not require unloading/loading for 6.1 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the 4 selectable levels of FIFO trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The 654 combines the package interface modes of the 16C454/554 and 68/C454/554 series on a single integrated chip. The 16 mode interface is designed to operate with the Intel type of microprocessor bus while the 68 mode is intended to operate with Motorola, and other popular microprocessors. Following a reset, the 654 is down-ward compatible with the ST16C454/ST68C454 or the ST68C454/ST68C554 dependent on the state of the interface mode selection pin, 16/-68.

The 654 is capable of operation to 1.5Mbps with a 24 MHz crystal or external clock input. With a crystal of 14.7464 MHz and through a software option, the user can select data rates up to 460.8Kbps or 921.6Kbps.

The rich feature set of the 654 is available through internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable TX and RX baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features. MCR bit-5 provides a facility for turning off (Xon) software flow control with any incoming (RX) character. In the 16 mode INTSEL and MCR bit-3 can be configured to provide a software controlled or continuous interrupt capability. Due to pin limitations for the 64 pin 654 this feature is offered by two different QFP packages. The ST16C654DCQ64 operates in the continuous interrupt enable mode by bonding INTSEL to VCC internally. The ST16C654CQ64 operates in conjunction with MCR bit-3 by bonding INTSEL to GND internally.

The 68 and 100 pin ST16C654 packages offer a clock select pin to allow system/board designers to preset the default baud rate table. The CLKSEL pin selects the div-by-1 or div-by-4 pre-scaleable baud rate generator table during initialization, but can be overridden following initialization by MCR bit-7.

The 100 pin packages offer several enhanced features. These features include a separate clock input for channel C (typically MIDI applications), an internal FIFO monitor register, and separate IrDA TX outputs. The MIDI (Musical Instrument Digital Interface) can be connected to the XTAL2 pin for normal operation or to external MIDI oscillator for MIDI applications. A separate register is provided for monitoring the real-time status of the FIFO signals -TXRDY and -RXRDY for each

of the four UART channels (A-D). This reduces polling time involved in accessing individual channels. The 100 pin QFP package also offers, four separate IrDA (Infrared Data Association Standard) outputs for Infrared applications. These outputs are provided in addition to the standard asynchronous modem data outputs.

FUNCTIONAL DESCRIPTIONS

Interface Options

Two user interface modes are selectable for the 654 device (68 and 100 pin packages). These interface modes are designated as the “16 mode” and the “68 mode.” This nomenclature corresponds to the early 16C454/554 and 68C454/554 package interfaces respectively.

The 16 Mode Interface

The 16 mode configures the package interface pins for connection as a standard 16 series (Intel) device and operates similar to the standard CPU interface available on the 16C454/554. In the 16 mode (pin 16/-68 logic 1) each UART is selected with individual chip select (CSx) pins as shown in Table 1 below.

Table 1, SERIAL PORT CHANNEL SELECTION GUIDE, 16 MODE INTERFACE

-CSA	-CSB	-CSC	-CSD	UART CHANNEL
1	1	1	1	None
0	1	1	1	A
1	0	1	1	B
1	1	0	1	C
1	1	1	0	D

The 68 Mode Interface

The 68 mode configures the package interface pins for connection with Motorola, and other popular microprocessor bus types. The interface operates similar to the 68C454/554. In this mode the 654 decodes two additional addresses, A3-A4 to select one of the four UART ports. The A3-A4 address decode function is used only when in the 68 mode (16/-68 logic 0), and is shown in Table 2 below.

Table 2, SERIAL PORT CHANNEL SELECTION GUIDE, 68 MODE INTERFACE

-CS	A4	A3	UART CHANNEL
1	N/A	N/A	None
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D

Internal Registers

The 654 provides 15 (64/68 pin packages) or 16 (100 pin packages) internal registers for monitoring and control. These registers are shown in Table 3 below. Twelve registers are similar to those already available in the standard 16C554. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user assessable scratchpad register (SPR). Beyond the general 16C554 features and capabilities, the 654 offers an enhanced feature register set (EFR, Xon/Xoff 1-2) that provides on board hardware/software flow control. Register functions are more fully described in the following paragraphs.

Table 3, INTERNAL REGISTER DECODE

A2	A1	A0	READ MODE	WRITE MODE
General Register Set (THR/RHR, IER/ISR, MCR/MSR, LCR/LSR, SPR):				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	-----
1	1	0	Modem Status Register	-----
1	1	1	Scratchpad Register	Scratchpad Register
Baud Rate Register Set (DLL/DLM): Note *2				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
Enhanced Register Set (EFR, Xon/off 1-2): Note *3				
0	1	0	Enhanced Feature Register	Enhanced Feature Register
1	0	0	Xon-1 Word	Xon-1 Word
1	0	1	Xon-2 Word	Xon-2 Word
1	1	0	Xoff-1 Word	Xoff-1 Word
1	1	1	Xoff-2 Word	Xoff-2 Word
FIFO Ready Register: Note *4				
X	X	X	RXRDY (A-D), TXRDY (A-D)	-----

Note *2: These registers are accessible only when LCR bit-7 is set to a logic 1, and LCR is not 0xBF.

Note *3: Enhanced Feature Register, Xon 1,2 and Xoff 1,2 are accessible only when the LCR is set to 0xBF.

Note *4: FIFO Ready Register is available through the -FSRS interface pin only.

FIFO Operation

The 64 byte transmit and receive data FIFO's are enabled by the FIFO Control Register (FCR) bit-0. With 16C554 devices, the user can set the receive trigger level but not the transmit trigger level. The 654 provides independent trigger levels for both receiver and transmitter. To remain compatible with ST16C554, the transmit interrupt trigger level is set to 8 following a reset. It should be noted that the user can set the transmit trigger levels by writing to the FCR register, but activation will not take place until EFR bit-4 is set to a logic 1. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached. (see Timeout Interrupt for a description of this timing).

Hardware Flow Control

When automatic hardware flow control is enabled, the 654 monitors the -CTS pin for a remote buffer overflow indication and controls the -RTS pin for local buffer overflows. Automatic hardware flow control is selected by setting bits 6 (RTS) and 7 (CTS) of the EFR register to a logic 1. If -CTS transitions from a logic 0 to a logic 1 indicating a flow control request, ISR bit-5 will be set to a logic 1 (if enabled via IER bit 6-7), and the 654 will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the -CTS input returns to a logic 0, indicating more data may be sent.

With the Auto RTS function enabled, an interrupt is generated when the receive FIFO reaches the programmed trigger level. The -RTS pin will not be forced to a logic 1 (RTS Off), until the receive FIFO reaches the next trigger level. The -RTS pin will return to a logic 0 after the data buffer (FIFO) is unloaded to the next trigger level below the programmed trigger. However, under the above described conditions the 654 will continue to accept data until the receive FIFO is full. The table below shows these FIFO levels.

Software Flow Control

When software flow control is enabled, the 654 compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) match the programmed values, the 654 will halt transmission as soon as the current character(s) has completed transmission. When a match occurs, the receive Xoff (if enabled via Xoff IER bit-5) flags will be set and the interrupt output pin (if receive Xoff interrupt is enabled) will be activated. Following a suspension due to a match of the Xoff characters values, the 654 will monitor the receive data stream for a match to the Xon-1,2 character value(s). If a match is found, the 654 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to 0x00. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters and suspend/resume transmissions. When two 8-bit Xon/Xoff characters are selected, the 654 compares two consecutive receive characters with two

Table 4, FLOW CONTROL MECHANISM

Selected Trigger Level (characters)	INT Pin Activation (characters)	-RTS Logic "1" (characters)	-RTS Logic "0" (characters)	Send XOFF Character (characters)	Send XON Character (characters)
8	8	16	0	8	0
16	16	56	8	16	8
56	56	60	16	56	16
60	60	60	56	60	56

software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the 654 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The 654 sends the Xoff-1,2 characters as soon as received data passes the programmed trigger level. To clear this condition, the 654 will transmit the programmed Xon-1,2 characters as soon as receive data drops below the next lower programmed trigger level (see Table 4).

Xon Any Feature

The 654 offers a special Xon mode via MCR bit-5. The initialized default setting of MCR bit-5 is a logic 0. In this state Xoff and Xon will operate as defined above. Setting MCR bit-5 to a logic 1 sets a special operational mode for the Xon function. In this case Xoff operates normally however, transmission will resume with the next character received, i.e., a match is declared simply by the receipt of an incoming receive character.

Special Feature Software Flow Control

A special feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When 8 bit character is detected, it will be placed on the user accessible data stack along with normal incoming RX data. This condition is selected in conjunction with EFR bits 0-3. Note that software flow control should be turned off when using this special mode by setting EFR bit 0-3 to a logic 0.

The 654 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows each X-Register with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special

character comparison. Bit-0 in the X-registers corresponds with the LSB bit for the receive character.

Flow Control Interrupts

Three special interrupts have been added to monitor the hardware and software flow control. The interrupts are enabled by IER bits 5-7. Care must be taken when handling these interrupts. Following a reset the transmitter interrupt is enabled, the 654 will issue an interrupt to indicate that transmit holding register is empty. This interrupt must be serviced prior to continuing operations. The LSR register provides the current singular highest priority interrupt only. Note that CTS and RTS interrupts have lowest interrupt priority. A condition can exist where a higher priority interrupt may mask the lower priority CTS/RTS interrupt(s). Only after servicing the higher pending interrupt will the lower priority CTS/RTS interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

Timeout Interrupts

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time Out have the same interrupt priority (when enabled by IER bit-3). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case the 654 FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should recheck LSR bit-0 for additional characters. A Receive Time Out will not occur if the receive FIFO is empty. The time out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read. The actual time out value is T (Time out length in bits) = $4 \times P$ (Programmed word length) + 12. To convert the time out value to a character value, the user has to consider the complete word length, including data information length, start bit, parity bit, and the size of stop bit, i.e., 1X, 1.5X, or 2X bit times.

Example -A: If the user programs a word length of 7, with no parity and one stop bit, the time out will be:
 $T = 4 \times 7$ (programmed word length) + 12 = 40 bit times.
The character time will be equal to $40 / 9 = 4.4$ characters, or as shown in the fully worked out example:

$T = [(\text{programmed word length} = 7) + (\text{stop bit} = 1) + (\text{start bit} = 1) = 9] \cdot 40$ (bit times divided by 9) = 4.4 characters.

Example -B: If the user programs the word length = 7, with parity and one stop bit, the time out will be:
 $T = 4 \times 7$ (programmed word length) + 12 = 40 bit times.
 Character time = $40 / 10$ [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1)] = 4 characters.

Three State Interrupts

In the 16 mode for 68/100 pin packages, the system/board designer can optionally provide software controlled three state interrupt operation. This is accomplished by INTSEL and MCR bit-3. When INTSEL interface pin is left open or made a logic 0, MCR bit-3 controls the three state interrupt outputs, INT A-D. When INTSEL is a logic 1, MCR bit-3 has no effect on the INT A-D outputs and the package operates with interrupt outputs enabled continuously.

Programmable Baud Rate Generator

The 654 supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example a 33.6Kbps modem that employs data compression may require a 115.2Kbps input data rate. A 128.0Kbps ISDN modem that supports data compression may need an input data rate of 460.8Kbps. The 654 can support a standard data rate of 921.6Kbps.

The programmable Baud Rate Generator is capable of accepting an input clock up to 24 MHz, as required for supporting a 1.5Mbps data rate. The 654 can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant/ 22-33 pF load) is connected externally between the XTAL1 and XTAL2 pins (see figure 4). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates.

The generator divides the input 16X clock by any divisor

from 1 to $2^{16} - 1$. The 654 divides the basic crystal or external clock by 16. Further division of this 16X clock provides two table rates to support low and high data rate applications using the same system design. After a hardware reset and during initialization, the 654 sets the default baud rate table according to the state of the CLKSEL. pin. A logic 1 on CLKSEL will set the div-by-1 clock default whereas, logic 0 will set the div-by-4 clock default table. Following the default clock rate selection during initialization, the rate tables can be changed by the internal register, MCR bit-7. Setting MCR bit-7 to a logic 1 when CLKSEL is a logic 1 provides an additional divide by 4 whereas, setting MCR bit-7 to a logic 0 only divides by 1. (See Table 5 and Figure 5). Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 5 below, shows the two selectable baud rate tables available when using a 7.3728 MHz crystal.

DMA Operation

Figure 4, Crystal oscillator connection

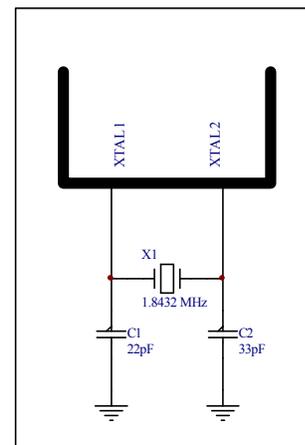
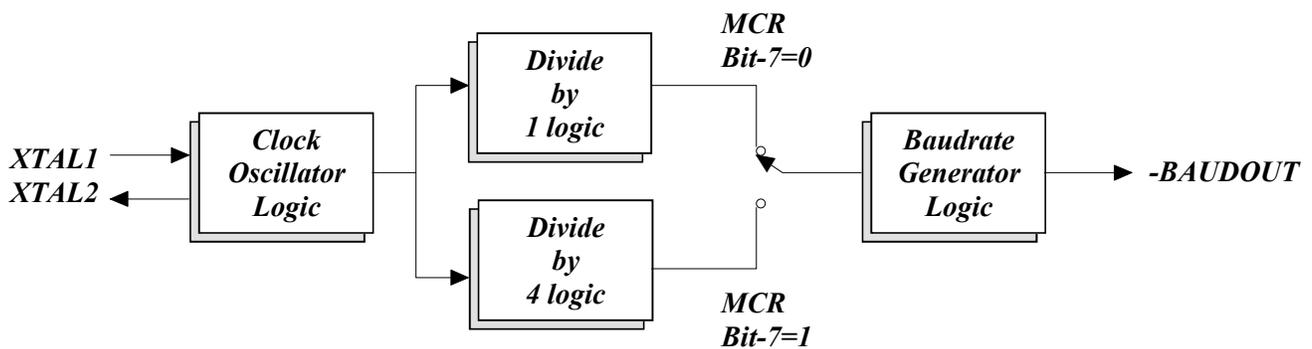


Table 5, BAUD RATE GENERATOR PROGRAMMING TABLE (7.3728 MHz CLOCK):

Output Baud Rate MCR BIT-7=1	Output Baud Rate MCR Bit-7=0	User 16 x Clock Divisor (Decimal)	User 16 x Clock Divisor (HEX)	DLM Program Value (HEX)	DLL Program Value (HEX)
50	200	2304	900	09	00
300	1200	384	180	01	80
600	2400	192	C0	00	C0
1200	4800	96	60	00	60
2400	9600	48	30	00	30
4800	19.2K	24	18	00	18
9600	38.4k	12	0C	00	0C
19.2k	76.8k	6	06	00	06
38.4k	153.6k	3	03	00	03
57.6k	230.4k	2	02	00	02
115.2k	460.8k	1	01	00	01

Figure 5, Baud Rate Generator Circuitry



The ST16C654 FIFO trigger level provides additional flexibility to the user for block mode operation. The user can optionally operate the transmit and receive FIFO's in the DMA mode (FCR bit-3). The DMA mode affects the state of the -RXRDY and -TXRDY output pins. The following tables show this:

-RXRDY pin:	
Non-DMA mode	DMA mode
1 = FIFO empty	0 to 1 transition when FIFO empties
0 = at least 1 byte in FIFO	1 to 0 transition when FIFO reaches trigger level, or timeout occurs

-TXRDY pin:	
Non-DMA mode	DMA mode
1 = at least 1 byte in FIFO	1 = FIFO is full
0 = FIFO empty	0 = FIFO has at least 1 empty location

Sleep Mode

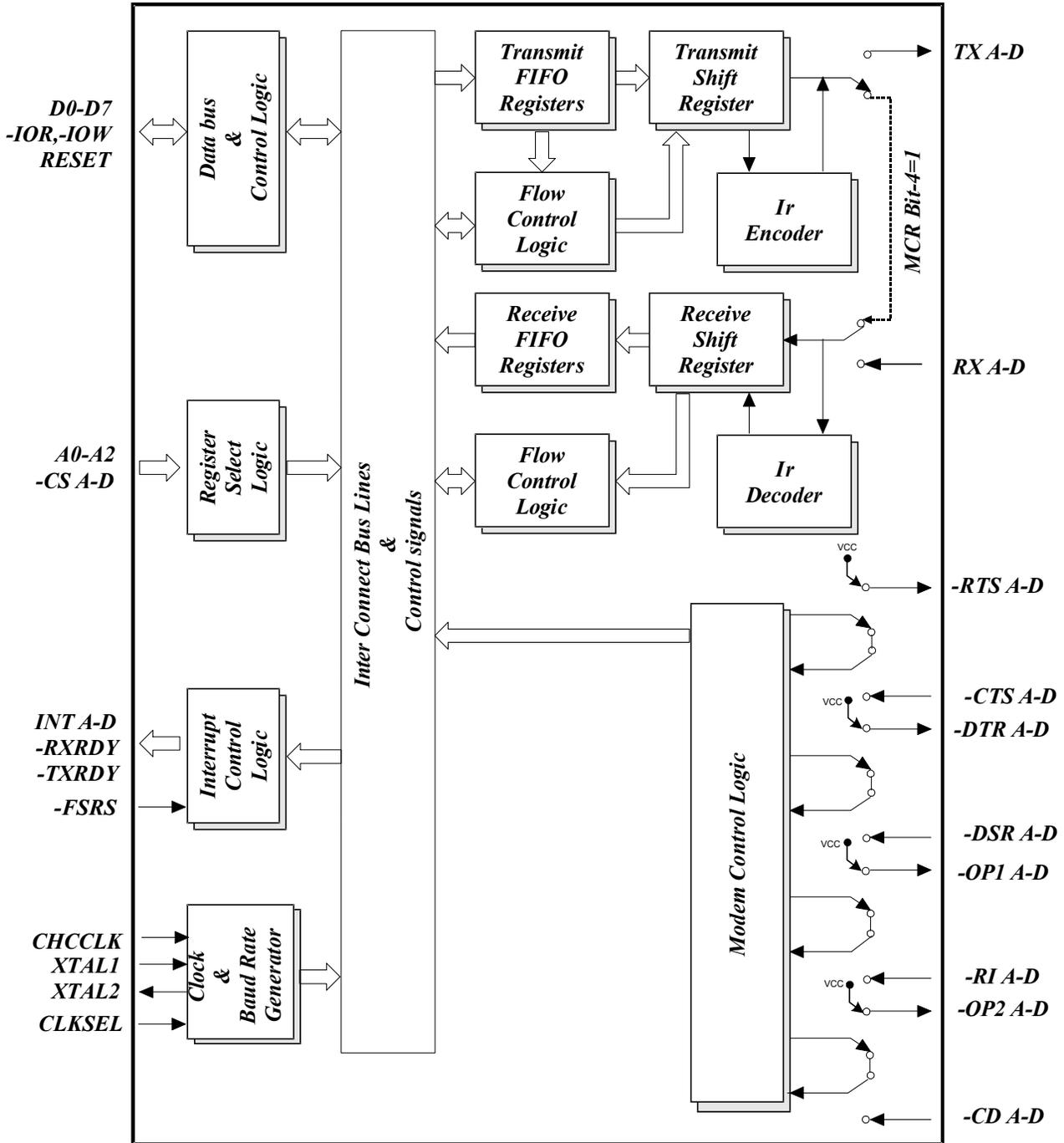
The 654 is designed to operate with low power consumption. A special sleep mode is included to further reduce power consumption when the chip is not being used. With EFR bit-4 and IER bit-4 enabled (set to a logic 1), the 654 enters the sleep mode but resumes normal operation when a start bit is detected, a change of state on any of the modem input pins RX, -RI, -CTS, -DSR, -CD, or transmit data is provided by the user. If the sleep mode is enabled and the 654 is awakened by one of the conditions described above, it will return to the sleep mode automatically after the last character is transmitted or read by the user. In any case, the sleep mode will not be entered while an interrupt(s) is pending. Each 654 channel will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0. All the four channels must be programmed for sleep mode to stop the oscillator circuitry and thus achieve the least power consumption.

Loop-back Mode

The internal loop-back capability allows onboard diagnostics. In the loop-back mode the normal modem interface pins are disconnected and reconfigured for loop-back internally. MCR register bits 0-3 are used for controlling loop-back diagnostic testing. In the loop-back mode OP1 and OP2 in the MCR register (bits 3/2) control the modem -RI and -CD inputs respectively. MCR signals -DTR and -RTS (bits 0-1) are used to control the modem -CTS and -DSR inputs respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (See Figure 8). The -CTS, -DSR, -CD, and -RI are disconnected from their normal modem control inputs pins, and instead are connected internally to -RTS, -DTR, -OP2 and -OP1. Loop-back test data is entered into the transmit holding register via the user data bus interface, D0-D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loop-back connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface, D0-D7. The user optionally compares the received data to the initial transmitted data for verifying error free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. The interrupts are still controlled by the IER.

Figure 6, INTERNAL LOOP-BACK MODE DIAGRAM, CHANNEL A-D



REGISTER FUNCTIONAL DESCRIPTIONS

The following table delineates the assigned bit functions for the fifteen 654 internal registers. The assigned bit functions are more fully defined in the following paragraphs.

Table 6, ST16C654 INTERNAL REGISTERS

A2 A1 A0	Register [Default] Note *9	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
General Register Set (Note *5)										
0 0 0	RHR[XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0	
0 0 0	THR[XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0	
0 0 1	IER[00]	CTS interrupt	RTS interrupt	Xoff interrupt	Sleep mode	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register	
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	TX trigger (MSB)	TX trigger (LSB)	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable	
0 1 0	ISR[01]	FIFO's enabled	FIFO's enabled	INT priority bit-4	INT priority bit-3	INT priority bit-2	INT priority bit-1	INT priority bit-0	INT status	
0 1 1	LCR[00]	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0	
1 0 0	MCR[00]	Clock select	R enable	Xon Any	loop back	-OP2/INTx enable	-OP1	-RTS	-DTR	
1 0 1	LSR[60]	FIFO data error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready	
1 1 0	MSR[X0]	CD	Rl	DSR	CTS	delta -CD	delta -Rl	delta -DSR	delta -CTS	
1 1 1	SPR[FF]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0	
Special Register set: (Note *6)										
0 0 0	DLL[XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0	
0 0 1	DLM[XX]	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8	

A2 A1 A0	Register [Note *9]	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
Enhanced Register Set: (Note *7)									
0 1 0	EFR[00]	Auto CTS	Auto RTS	Special Char. select	Enable IER Bits 4-7, ISR, FCR Bits 4-5, MCR Bits 5-7	Cont-3 Tx,Rx Control	Cont-2 Tx,Rx Control	Cont-1 Tx,Rx Control	Cont-0 Tx,Rx Control
1 0 0	Xon-1[00]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
1 0 1	Xon-2[00]	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8
1 1 0	Xoff-1[00]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
1 1 1	Xoff-2[00]	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8
FIFO Ready Register: (Note *8)									
X X X	FIFORdy	RXRDY D	RXRDY C	RXRDY B	RXRDY A	TXRDY D	TXRDY C	TXRDY B	TXRDY A

Note *5: The RHR, THR and IER registers are accessible only when LCR bit-7 = 0.

Note *6: The Special register set is accessible only when LCR bit-7 is set to "1" and LCR is not equal to 0xBF.

Note *7: Enhanced Feature Register, Xon 1,2 and Xoff 1,2 are accessible only when LCR is set to 0xBF.

Note *8: FIFORdy register is available only in 100 pin QFP packages and is selected by -FSRS pin.

Note *9: The value between the square brackets represents the register's initialized value in hexadecimal.

Transmit (THR) and Receive (RHR) Holding Registers

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7-D0) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the transmit holding register empty flag is set (logic 0 = at least one byte in FIFO/THR, logic 1 = FIFO/THR empty).

The serial receive section also contains an 8-bit Receive Holding Register, RHR. Receive data is removed from the 654 and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at 16x clock rate. After 7 1/2 clocks the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INT A-D output pins in the 16 mode, or on WIRE-OR IRQ output pin, in the 68 mode.

IER Vs Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = a logic 1) and receive interrupts (IER BIT-0 = logic 1) are enabled, the receive interrupts and register status will reflect the following:

A) The receive data available interrupts are issued to the external CPU when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B) FIFO status will also be reflected in the user accessible ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

IER Vs Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1; resetting IER bits 0-3 enables the 654 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A) LSR BIT-0 will be a logic 1 as long as there is at least one byte in the receive FIFO.

B) LSR BIT 1-4 will provide the type of errors encountered, if any.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both the transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate any FIFO data errors.

IER BIT-0:

This interrupt will be issued when the FIFO has reached the programmed trigger level or is cleared when the FIFO drops below the trigger level in the FIFO mode of operation.

Logic 0 = Disable the receiver ready interrupt. (normal default condition)

Logic 1 = Enable the receiver ready interrupt.

IER BIT-1:

This interrupt will be issued whenever the THR is empty (if FIFO is not enabled) or when the FIFO drops below the trigger level (if FIFO is enabled) and is associated with bit-1 in the LSR register.

Logic 0 = Disable the transmitter empty interrupt. (normal default condition)
Logic 1 = Enable the transmitter empty interrupt.

IER BIT-2:

This interrupt will be issued whenever a receive data error condition exists as reflected in LSR bits 1-4.
Logic 0 = Disable the receiver line status interrupt. (normal default condition)
Logic 1 = Enable the receiver line status interrupt.

IER BIT-3:

Logic 0 = Disable the modem status register interrupt. (normal default condition)
Logic 1 = Enable the modem status register interrupt.

IER BIT -4:

Logic 0 = Disable sleep mode. (normal default condition)
Logic 1 = Enable sleep mode. See Sleep Mode section for details.

IER BIT-5:

Logic 0 = Disable the software flow control, receive Xoff interrupt. (normal default condition)
Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

IER BIT-6:

Logic 0 = Disable the RTS interrupt. (normal default condition)
Logic 1 = Enable the RTS interrupt. The 654 issues an interrupt when the RTS pin transitions from a logic 0 to a logic 1.

IER BIT-7:

Logic 0 = Disable the CTS interrupt. (normal default condition)
Logic 1 = Enable the CTS interrupt. The 654 issues an interrupt when CTS pin transitions from a logic 0 to a logic 1.

FIFO Control Register (FCR)

This register is used to enable the FIFO's, clear the FIFO's, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are

defined as follows:

DMA MODE

See description and DMA tables on page 20.

FCR BIT-0:

Logic 0 = Disable the transmit and receive FIFO. (normal default condition)
Logic 1 = Enable the transmit and receive FIFO. This bit must be a "1" when other FCR bits are written to or they will not be programmed.

FCR BIT-1:

Logic 0 = No FIFO receive reset. (normal default condition)
Logic 1 = Clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

FCR BIT-2:

Logic 0 = No FIFO transmit reset. (normal default condition)
Logic 1 = Clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

FCR BIT-3:

Logic 0 = Set DMA mode "0". (normal default condition)
Logic 1 = Set DMA mode "1."

Transmit operation in mode "0":

When the 654 is in the ST16C450 mode (FIFO's disabled, FCR bit-0 = logic 0) or in the FIFO mode (FIFO's enabled, FCR bit-0 = logic 1, FCR bit-3 = logic 0) and when there are no characters in the transmit FIFO or transmit holding register, the -TXRDY pin will be a logic 0. Once active the -TXRDY pin will go to a logic 1 after the first character is loaded into the transmit holding register.

Receive operation in mode "0":

When the 654 is in mode "0" (FCR bit-0 = logic 0) or in the FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 0) and there is at least one character in the receive FIFO, the -RXRDY pin will be a logic 0. Once active the -RXRDY pin will go to a logic 1 when there are no more

characters in the receiver.

Transmit operation in mode "1":

When the 654 is in FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 1), the -TXRDY pin will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 if one or more FIFO locations are empty.

Receive operation in mode "1":

When the 654 is in FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 1) and the trigger level has been reached, or a Receive Time Out has occurred, the -RXRDY pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO.

FCR BIT 4-5: (logic 0 or cleared is the default condition, TX trigger level = 8)

These bits are used to set the trigger level for the transmit FIFO interrupt. The ST16C654 will issue a transmit empty interrupt when the number of characters in FIFO drops below the selected trigger level.

BIT-5	BIT-4	TX FIFO trigger level
0	0	8
0	1	16
1	0	32
1	1	56

FCR BIT 6-7: (logic 0 or cleared is the default condition, Rx trigger level = 8)

These bits are used to set the trigger level for the receive FIFO interrupt. An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However the FIFO will continue to be loaded until it is full.

BIT-7	BIT-6	RX FIFO trigger level
0	0	8
0	1	16
1	0	56
1	1	60

Interrupt Status Register (ISR)

The 654 provides six levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. A lower level interrupt may be seen after rereading the interrupt status bits. The Interrupt Source Table 7 (below) shows the data values (bits 0-5) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Interrupt generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is when incoming data fills beyond the trigger level.
- RXRDY Time-out is by the 4-char delay timer.
- TXRDY is by TX trigger level.
- MSR is by any of the MSR bits, 0, 1, 2 and 3.
- Receive Xoff/Special char. is by the detection of a Xoff or Special character.
- CTS is by the change of state on the input pin, and RTS is when auto RTS flow control is enabled and the receiver changes the state of the output pin.

Interrupt clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY and RXRDY time out are cleared by unloading data out of the FIFO below the trigger level.
- TXRDY interrupt is cleared by a read to the ISR register.
- MSR interrupt is cleared by a read to the MSR register.
- Xoff or Special character interrupt is cleared by a read to the ISR register.
- RTS and CTS status change interrupts are cleared by a read to the MSR register.

ISR BIT-0:

Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

Logic 1 = No interrupt pending. (normal default condition)

Table 7, INTERRUPT SOURCE TABLE

Priority Level	[ISR BITS]						Source of the interrupt
	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
X	0	0	0	0	0	1	None (Default)
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Received Data Ready)
2	0	0	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	0	0	MSR (Modem Status Register)
5	0	1	0	0	0	0	RXRDY (Received Xoff signal)/ Special character
6	1	0	0	0	0	0	CTS, RTS change of state

ISR BIT 1-3: (logic 0 or cleared is the default condition)
 These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (See Interrupt Source

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

Table below).

ISR BIT 4-5: (logic 0 or cleared is the default condition)
 These bits are enabled when EFR bit-4 is set to a logic

BIT-2	Word length	Stop bit length (Bit time(s))
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

1. ISR bit-4 indicates that matching Xoff character(s) have been detected. ISR bit-5 indicates that CTS, RTS have been generated. Note that once set to a logic 1, the

LCR Bit-5	LCR Bit-4	LCR Bit-3	Parity selection
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity "1"
1	1	1	Forced parity "0"

ISR bit-4 will stay a logic 1 until Xon character(s) are received.

ISR BIT 6-7: (logic 0 or cleared is the default condition)
 These bits are set to a logic 0 when the FIFO is not being used. They are set to a logic 1 when the FIFO's are enabled.

Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR BIT 0-1: (logic 0 or cleared is the default condition)
 These two bits specify the word length to be transmitted or received.

LCR BIT-2: (logic 0 or cleared is the default condition)
 The length of stop bit is specified by this bit in conjunction with the programmed word length.

LCR BITS 3-5:

Parity can be programmed using these bits as shown in the table below:

LCR BIT-6:

When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR bit-6 to a logic 0.

Logic 0 = No TX break condition. (normal default condition)

Logic 1 = Forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition.

LCR BIT-7:

The internal baud rate counter latch enable.

Logic 0 = Divisor latch disabled. (normal default condition)

Logic 1 = Divisor latch enabled.

Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

MCR BIT-0:

Logic 0 = Force -DTR output to a logic 1. (normal default condition)

Logic 1 = Force -DTR output to a logic 0.

MCR BIT-1:

Logic 0 = Force -RTS output to a logic 1. (normal default condition)

Logic 1 = Force -RTS output to a logic 0.

Automatic RTS may be used for hardware flow control by enabling EFR bit-6 (See EFR bit-6).

MCR BIT-2:

This bit is used in the Loop-back mode only. In the loop-back mode this bit is used to write the state of the modem -RI interface signal via -OP1.

MCR BIT-3: (Used to control the modem -CD signal in the loop-back mode.)

Logic 0 = Forces INT (A-D) outputs to the three state mode during the 16 mode. (normal default condition) In the Loop-back mode, sets -OP2 (-CD) internally to a logic 1.

Logic 1 = Forces the INT (A-D) outputs to the active mode during the 16 mode. In the Loop-back mode,

sets -OP2 (-CD) internally to a logic 0.

MCR BIT-4:

Logic 0 = Disable loop-back mode. (normal default condition)

Logic 1 = Enable local loop-back mode (diagnostics).

MCR BIT-5:

Logic 0 = Disable Xon any function (for 16C550 compatibility). (normal default condition)

Logic 1 = Enable Xon any function. In this mode any RX character received will enable Xon.

MCR BIT-6:

Logic 0 = Enable the standard modem receive and transmit input/output interface. (normal default condition)

Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. While in this mode, the TX/RX output/Inputs are routed to the infrared encoder/decoder. The data input and output levels will conform to the IrDA infrared interface requirement. As such, while in this mode the infrared TX output will be a logic 0 during idle data conditions.

MCR BIT-7:

Logic 0 = Divide by one. The input clock (crystal or external) is divided by sixteen and then presented to the Programmable Baud Rate Generator (BGR) without further modification, i.e., divide by one. (normal, default condition)

Logic 1 = Divide by four. The divide by one clock described in MCR bit-7 equals a logic 0, is further divided by four (also see Programmable Baud Rate Generator section).

Line Status Register (LSR)

This register provides the status of data transfers between the 654 and the CPU.

LSR BIT-0:

Logic 0 = No data in receive holding register or FIFO. (normal default condition)

Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR BIT-1:

Logic 0 = No overrun error. (normal default condition)

Logic 1 = Overrun error. A data overrun error occurred

in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR BIT-2:

Logic 0 = No parity error. (normal default condition)
Logic 1 = Parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.

LSR BIT-3:

Logic 0 = No framing error. (normal default condition)
Logic 1 = Framing error. The receive character did not have a valid stop bit(s). In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:

Logic 0 = No break condition. (normal default condition)
Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character (0x00) is loaded into the FIFO, even for a longer break signal.

LSR BIT-5:

This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

LSR BIT-6:

This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmit FIFO and transmit shift register

are both empty.

LSR BIT-7:

Logic 0 = No Error. (normal default condition)
Logic 1 = At least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when the last remaining bad character is read out of the FIFO.

Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device that the 654 is connected to. The lower nibble of this register is used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state and are reset to a logic 0 whenever the CPU reads this register.

MSR BIT-0:

Logic 0 = No -CTS Change (normal default condition)
Logic 1 = The -CTS input to the 654 has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-1:

Logic 0 = No -DSR Change. (normal default condition)
Logic 1 = The -DSR input to the 654 has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-2:

Logic 0 = No -RI Change. (normal default condition)
Logic 1 = The -RI input to the 654 has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.

MSR BIT-3:

Logic 0 = No -CD Change. (normal default condition)
Logic 1 = Indicates that the -CD input to the has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-4:

-CTS functions as hardware flow control signal input if it is enabled via EFR bit-7. The transmit holding register flow control is enabled/disabled by MSR bit-4. Flow control (when enabled) allows the starting and stop-

ping the transmissions based on the external modem - CTS signal. A logic 1 at the -CTS pin will stop 654 transmissions as soon as current character has finished transmission.

Normally MSR bit-4 bit is the compliment of the -CTS input. However in the loop-back mode, this bit is equivalent to the RTS bit in the MCR register.

MSR BIT-5:

DSR (active high, logical 1). Normally this bit is the compliment of the -DSR input. In the loop-back mode, this bit is equivalent to the DTR bit in the MCR register.

MSR BIT-6:

RI (active high, logical 1). Normally this bit is the compliment of the -RI input. In the loop-back mode this bit is equivalent to the OP1 bit in the MCR register.

MSR BIT-7:

CD (active high, logical 1). Normally this bit is the compliment of the -CD input. In the loop-back mode this bit is equivalent to the OP2 bit in the MCR register.

Scratchpad Register (SPR)

The ST16C654 provides a temporary data register to store 8 bits of user information.

Enhanced Feature Register (EFR)

Enhanced features are enabled or disabled using this register.

Bits-0 through 4 provide single or dual character software flow control selection. When the Xon1 and Xon2 and/or Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters.

EFR BIT 0-3: (logic 0 or cleared is the default condition)
Combinations of software flow control can be selected by programming these bits. See Table 8 for details.

EFR BIT-4:

Enhanced function control bit. The content of the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 can be modified and latched. After modifying any bits in the enhanced registers, EFR bit-4 can be set to a logic

Table 8, SOFTWARE FLOW CONTROL FUNCTIONS

Cont-3	Cont-2	Cont-1	Cont-0	TX, RX software flow controls
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1 and Xon2; Xoff1 and Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1. Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2, Xoff1 and Xoff2 Receiver compares Xon1 and Xon2, Xoff1 and Xoff2
0	0	1	1	No transmit flow control Receiver compares Xon1 and Xon2, Xoff1 and Xoff2

0 to latch the new values. This feature prevents existing software from altering or overwriting the 654 enhanced functions.

Logic 0 = Disable write access to IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are set to a logic 0 to be compatible with ST16C554 mode. (normal default condition).

Logic 1 = Enable write access to these bits (shown shaded in Table 6).

EFR BIT-5:

Logic 0 = Special Character Detect Disabled. (normal default condition)

Logic 1 = Special Character Detect Enabled. The 654 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Bit-0 in the X-registers corresponds with the LSB bit for the receive character. When this feature is enabled, the normal software flow control must be disabled (EFR bits 0-3 must be set to a logic 0).

EFR BIT-6:

Automatic RTS may be used for hardware flow control by enabling EFR bit-6. When AUTORTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and -RTS will go to a logic 1 at the next trigger level. -RTS will return to a logic 0 when data is unloaded below the next lower trigger level (Programmed trigger level -1). -RTS functions normally when automatic hardware flow control is disabled.

0 = Automatic RTS flow control is disabled. (normal default condition)

1 = Enable Automatic RTS flow control.

EFR bit-7:

Automatic CTS Flow Control.

Logic 0 = Automatic CTS flow control is disabled. (normal default condition)

Logic 1 = Enable Automatic CTS flow control. Transmission will stop when -CTS goes to a logic 1. Transmission will resume when the -CTS pin returns to a logic 0.

FIFO READY REGISTER

This register is applicable to 100 pin ST16C654s only. The FIFO register provides the real-time status of the transmit and receive FIFO's. Each TX and RX channel (A-D) has its own 64 byte FIFO. When any of the eight TX/RX FIFO's become full, a bit associated with its TX/RX function and channel A-D is set in the FIFO status register. This read-only register can be accessed only when FSR pin is low.

FIFO channel A-D RDY Bit 0-3:

0 = The transmit FIFO A-D associated with this bit is full. This channel will not accept any more transmit data.

1 = One or more empty locations exist in the FIFO.

FIFORdy Bit 4-7:

0 = The receive FIFO is above the programmed trigger level or time-out is occurred.

1 = Receiver is ready and is below the programmed trigger level.

ST16C654 EXTERNAL RESET CONDITIONS

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7= input signals
FCR	FCR BITS 0-7=0
EFR	EFR BITS 0-7=0

SIGNALS	RESET STATE
TXA-D	High
-RTS A-D	High
-DTRA-D	High
-RXRDY A-D	High
-TXRDY A-D	Low

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), V_{CC}=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
T _{1w} , T _{2w}	Clock pulse duration	20		20		ns	
T _{3w}	Oscillator/Clock frequency		8		24	MHz	
T _{6s}	Address setup time	10		5		ns	
T _{7w}	-IOR strobe width	50		30		ns	
T _{7h}	Address hold time	5		5		ns	
T _{9d}	Read cycle delay	50		50		ns	
T _{12d}	Delay from -IOR to data	45		35		ns	
T _{12h}	Data disable time		30		20	ns	
T _{13w}	-IOW strobe width	40		30		ns	
T _{15d}	Write cycle delay	50		50		ns	
T _{16s}	Data setup time	20		15		ns	
T _{16h}	Data hold time	15		10		ns	
T _{17d}	Delay from -IOW to output		50		50	ns	100 pF load
T _{18d}	Delay to set interrupt from MODEM input		50		35	ns	100 pF load
T _{19d}	Delay to reset interrupt from -IOR		50		35	ns	100 pF load
T _{20d}	Delay from stop to set interrupt		1		1	Rclk	
T _{21d}	Delay from -IOR to reset interrupt		200		200	ns	100 pF load
T _{22d}	Delay from start to interrupt		100		100	ns	
T _{23d}	Delay from initial INT reset to transmit start	8	24	8	24	Rclk	
T _{24d}	Delay from -IOW to reset interrupt		175		175	ns	
T _{25d}	Delay from stop to set -RxRdy		1		1	Rclk	
T _{26d}	Delay from -IOR to reset -RxRdy		175		175	ns	
T _{27d}	Delay from -IOW to set -TxRdy		175		175	ns	
T _{28d}	Delay from start to reset -TxRdy		8		8	Rclk	
T _{30s}	Address setup time	10		10		ns	
T _{30w}	Chip select strobe width	66		50		ns	
T _{30h}	Address hold time	15		15		ns	
T _{30d}	Read cycle delay	70		70		ns	
T _{31d}	Delay from -CS to data		35		25	ns	
T _{31h}	Data disable time		25		15	ns	
T _{32s}	R/-W strobe setup time	10		10		ns	
T _{32h}	R/-W strobe hold time	10		10		ns	
T _{32d}	Write cycle delay	70		70		ns	
T _{33s}	Data setup time	20		15		ns	
T _{33h}	Data hold time	10		10		ns	
T _R	Reset pulse width	40		40		ns	
N	Baud rate divisor	1	2 ¹⁶ -1	1	2 ¹⁶ -1	Rclk	

ABSOLUTE MAXIMUM RATINGS

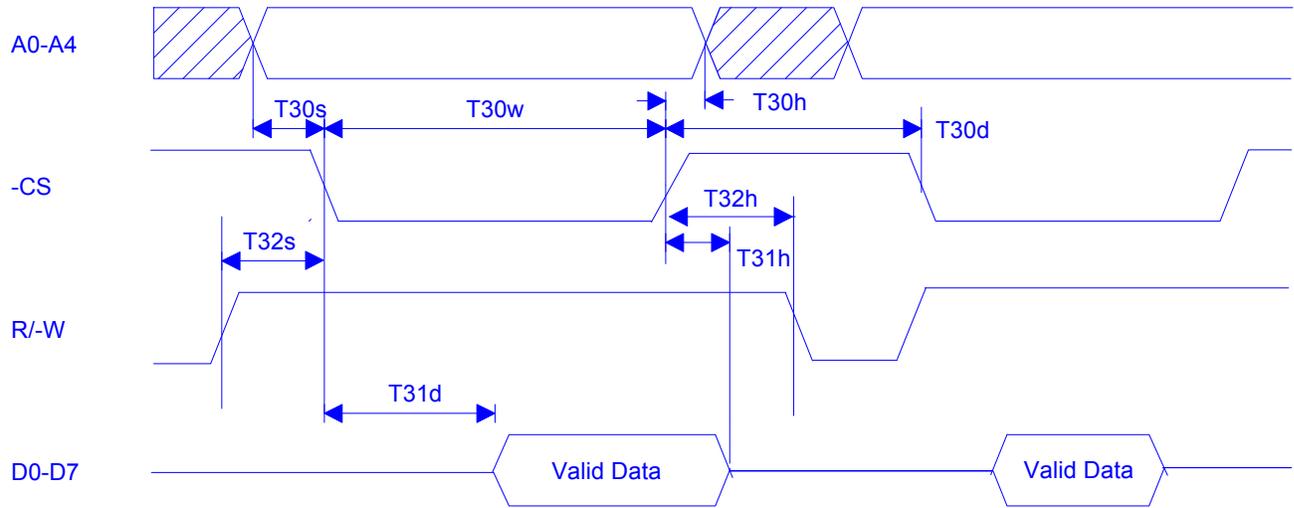
Supply range	7 Volts
Voltage at any pin	GND - 0.3 V to VCC +0.3 V
Operating temperature	-40° C to +85° C
Storage temperature	-65° C to 150° C
Package dissipation	500 mW
Package Thermal Resistance (in degC/W)	100 QFP: t _{ja} = 45, t _{jc} = 12; 68 PLCC: t _{ja} = 43, t _{jc} = 17; 64 TQFP: t _{ja} = 66, t _{jc} = 14.

DC ELECTRICAL CHARACTERISTICS

T_A = 0° - 70°C (-40° - +85°C for Industrial grade packages), V_{cc} = 3.3 - 5.0 V ± 10% unless otherwise specified.

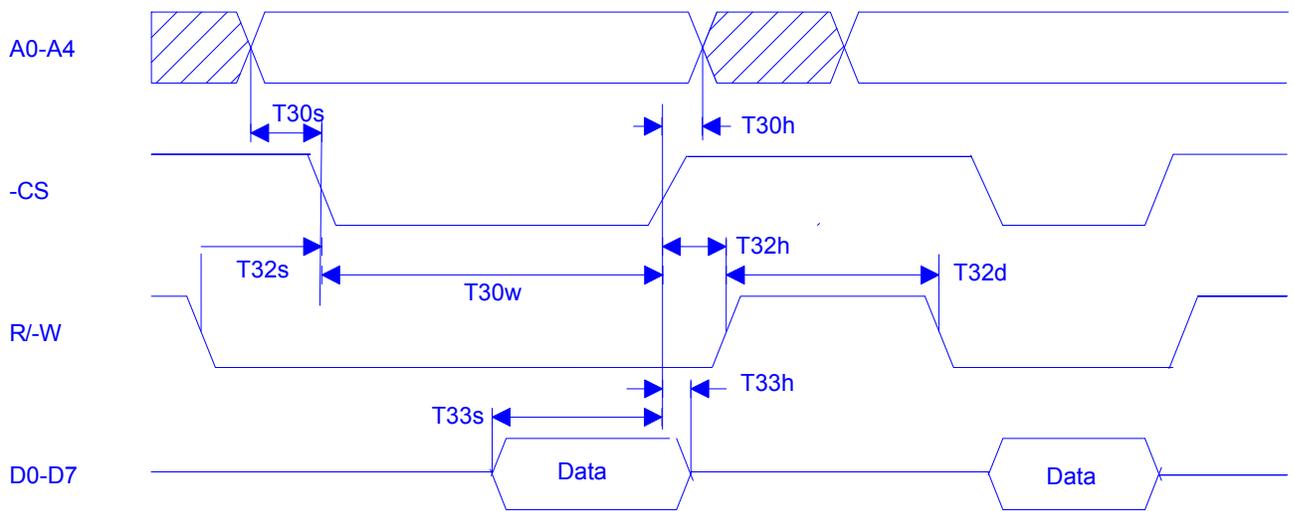
Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
V _{ILCK}	Clock input low level	-0.3	0.6	-0.5	0.6	V	
V _{IHCK}	Clock input high level	2.4	VCC	3.0	VCC	V	
V _{IL}	Input low level	-0.3	0.8	-0.5	0.8	V	
V _{IH}	Input high level	2.0	VCC	2.2	VCC	V	
V _{OL}	Output low level on all outputs				0.4	V	I _{OL} = 5 mA
V _{OL}	Output low level on all outputs		0.4			V	I _{OL} = 4 mA
V _{OH}	Output high level			2.4		V	I _{OH} = -5 mA
V _{OH}	Output high level	2.0				V	I _{OH} = -1 mA
I _{IL}	Input leakage		±10		±10	µA	
I _{CL}	Clock leakage		±10		±10	µA	
I _{CC}	Avg power supply current		3		6	mA	
C _P	Input capacitance		5		5	pF	
R _{IN}	Internal pull-up resistance	3			15	kΩ	

Note: See the Symbol Description Table, for a listing of pins having internal pull-up resistors.



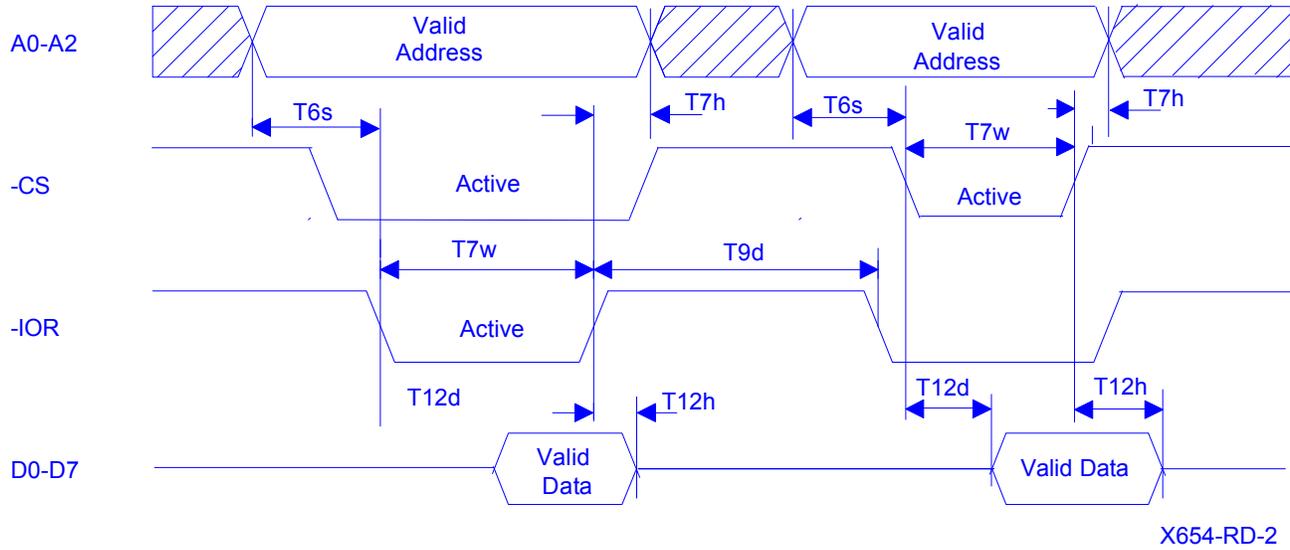
8654-RD-1

General read timing in 68 mode

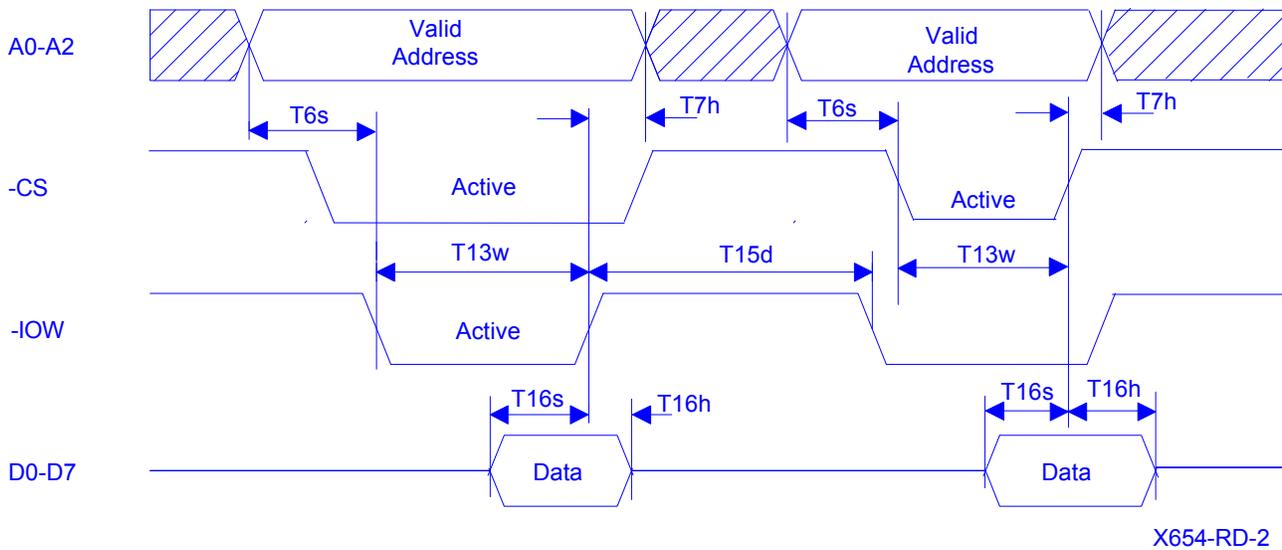


8654-WD-1

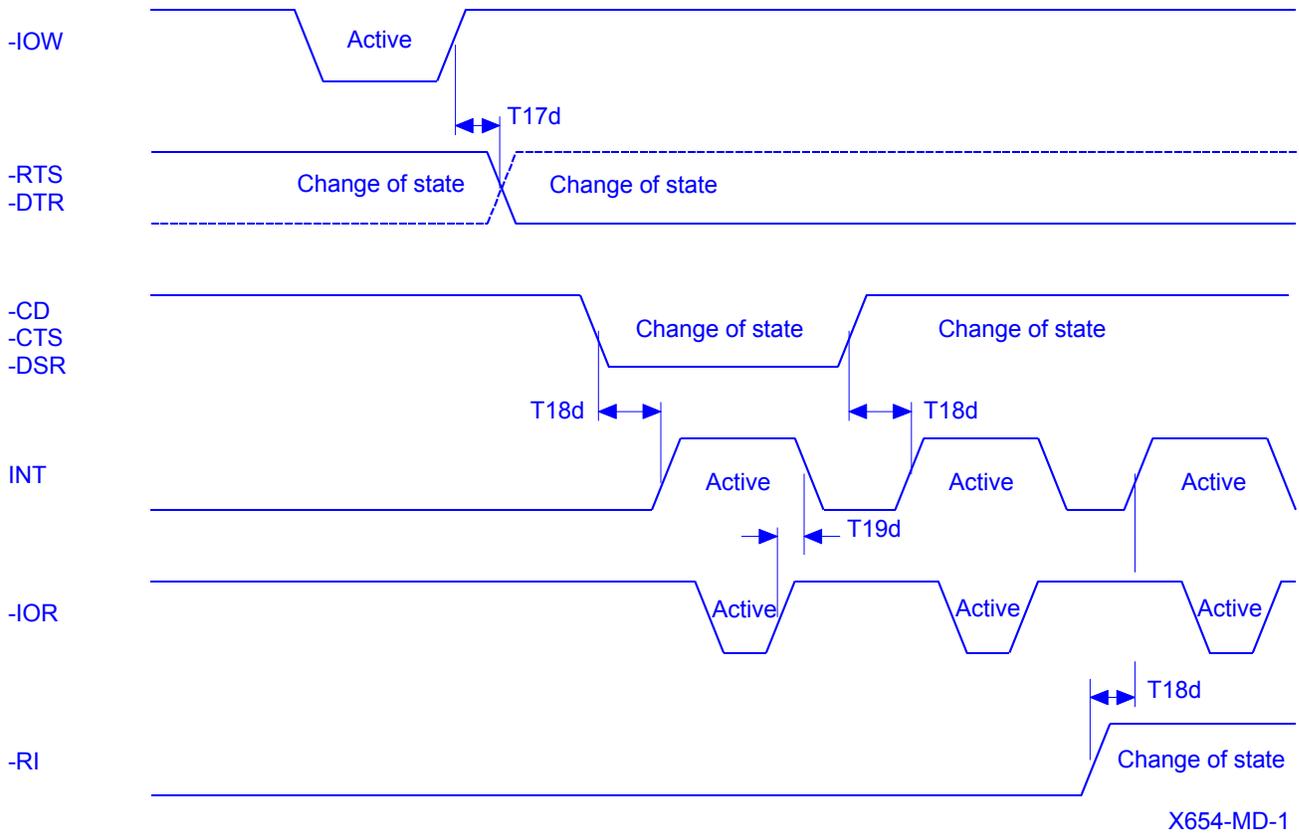
General write timing in 68 mode



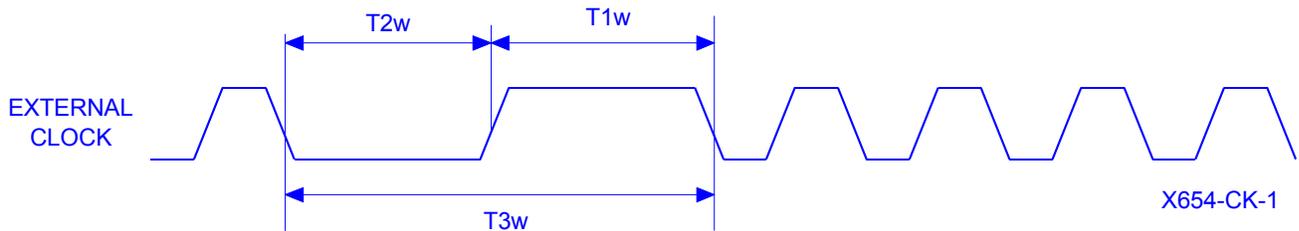
General read timing in 16 mode



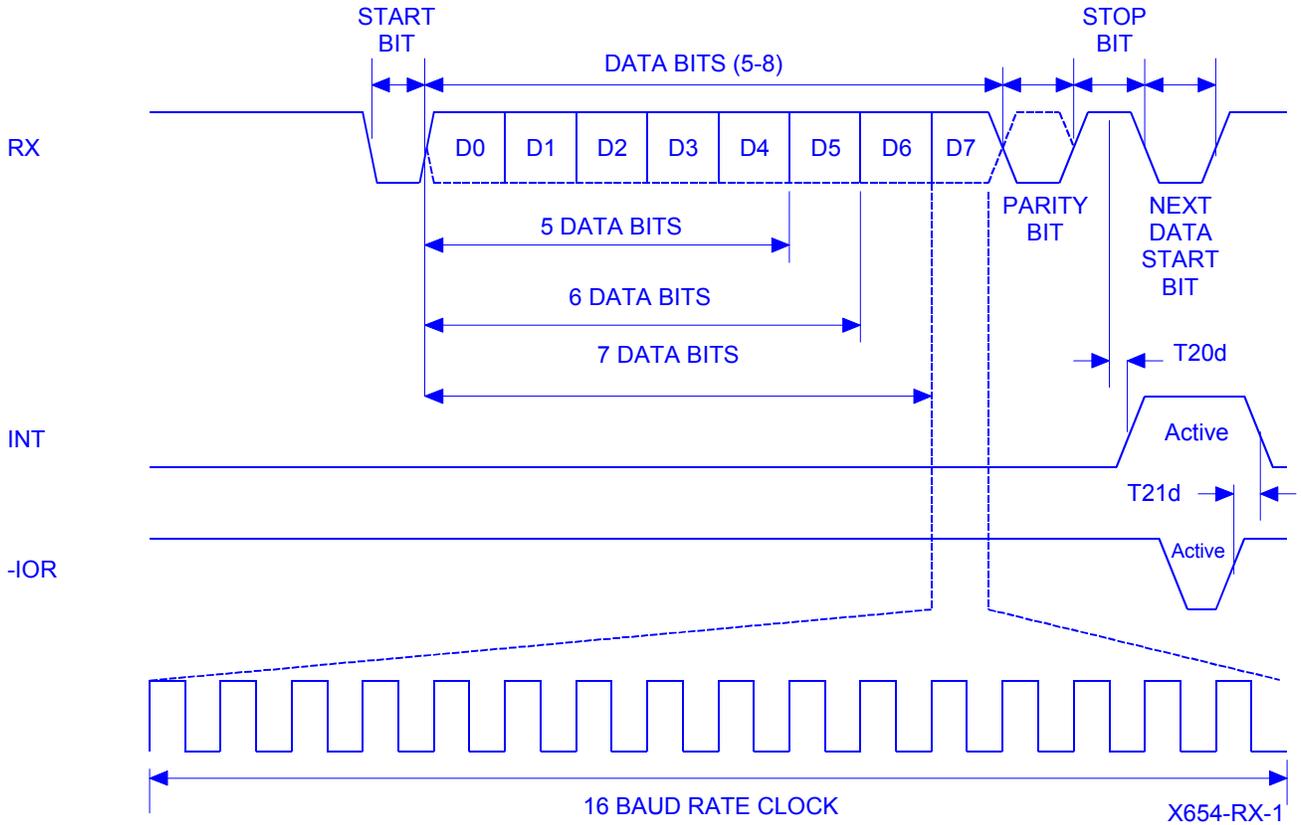
General write timing in 16 mode



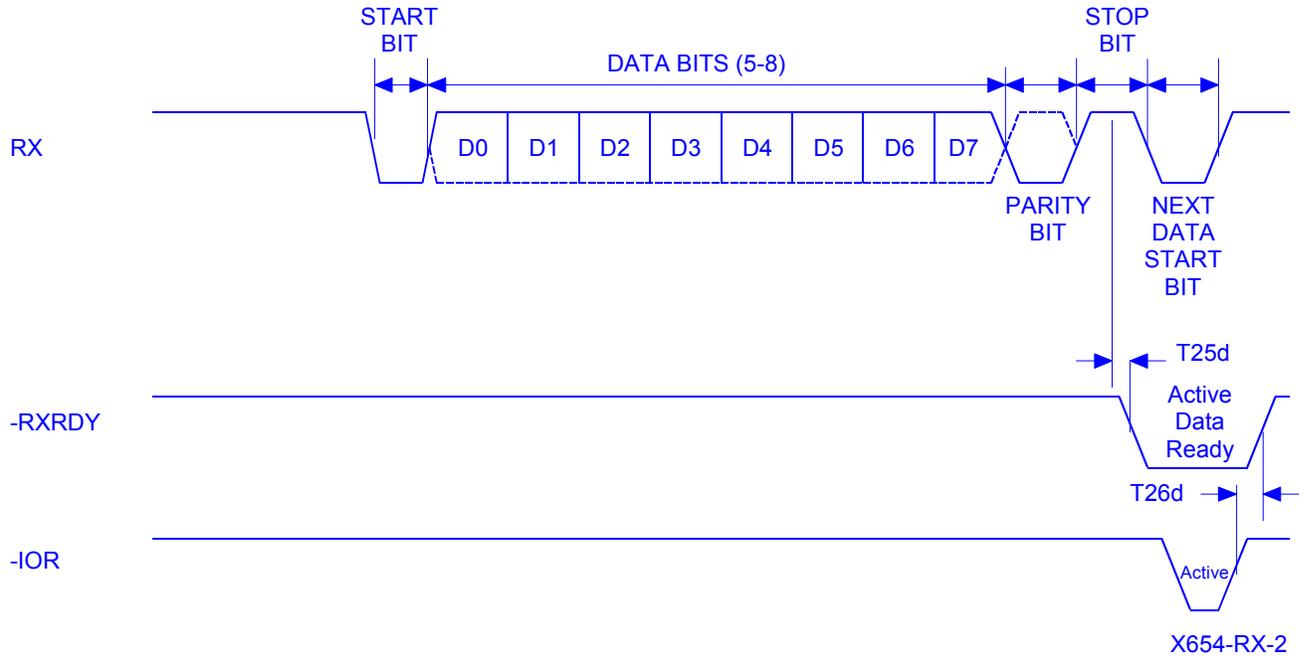
Modem input/output timing



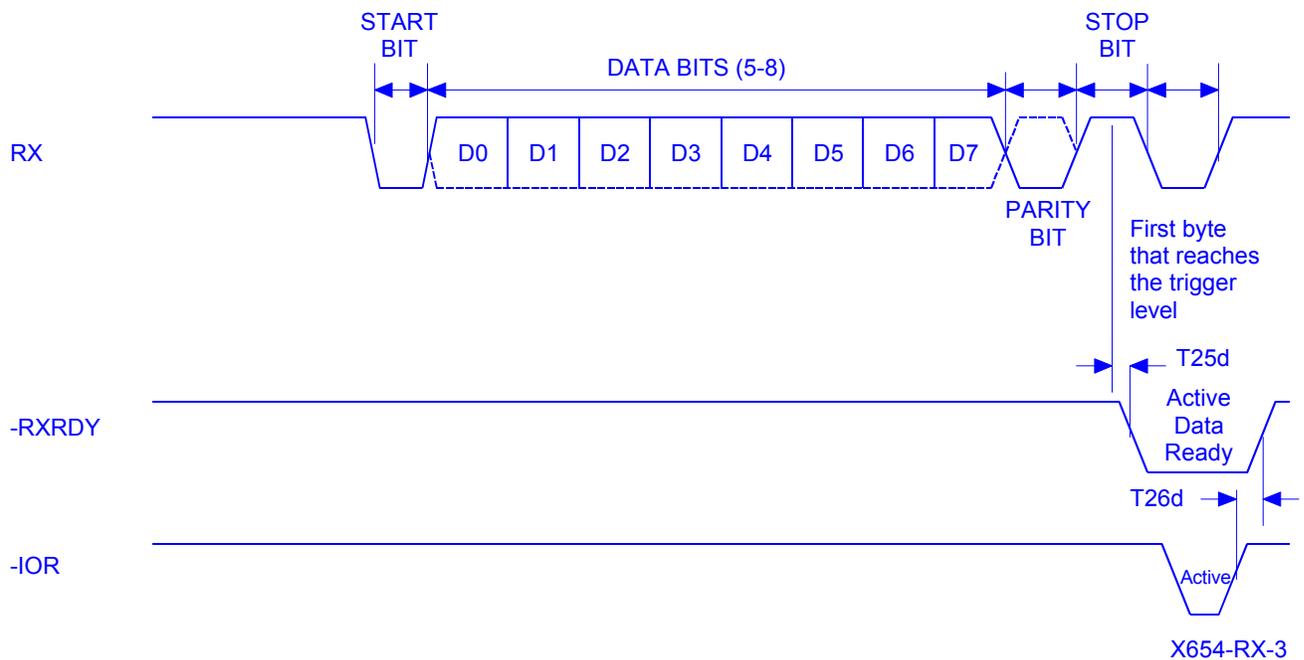
External clock timing



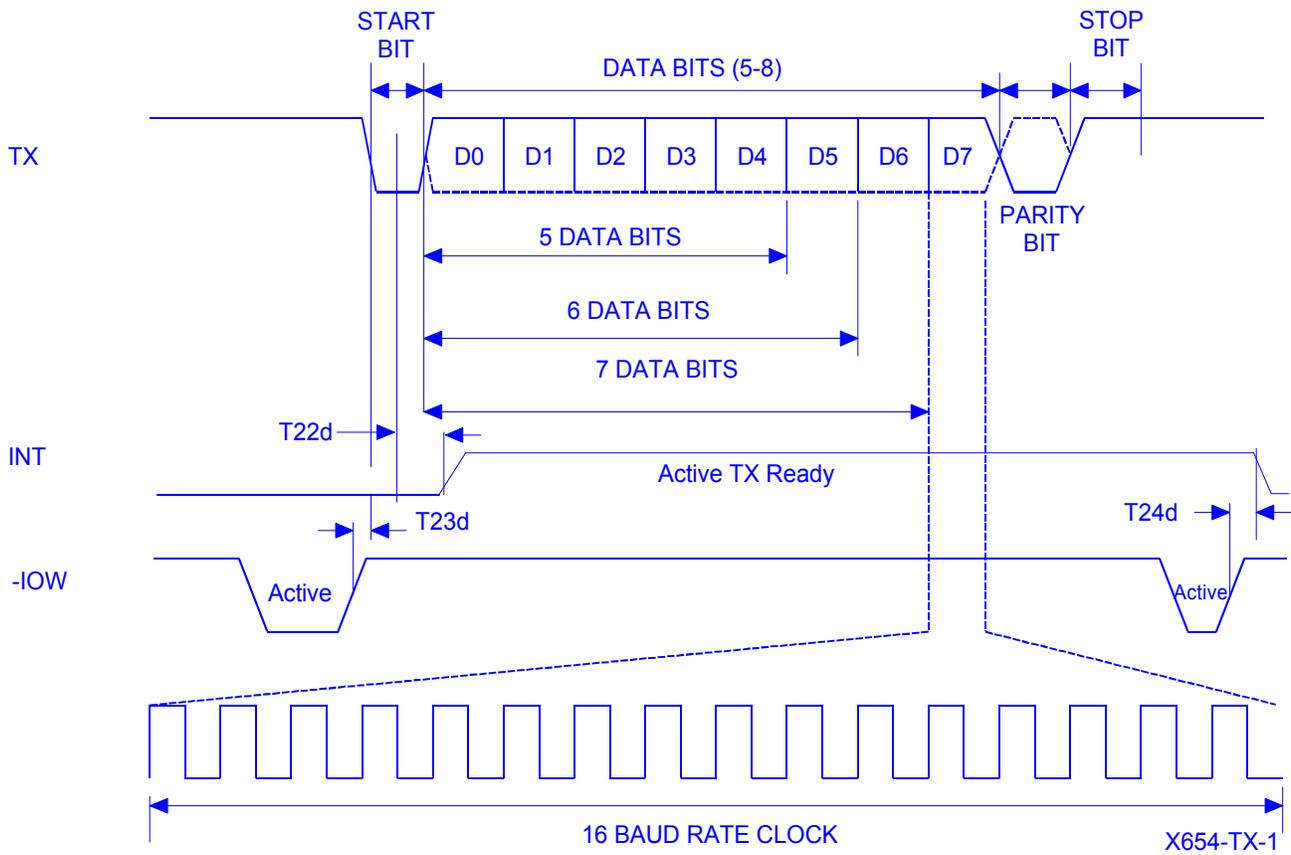
Receive timing



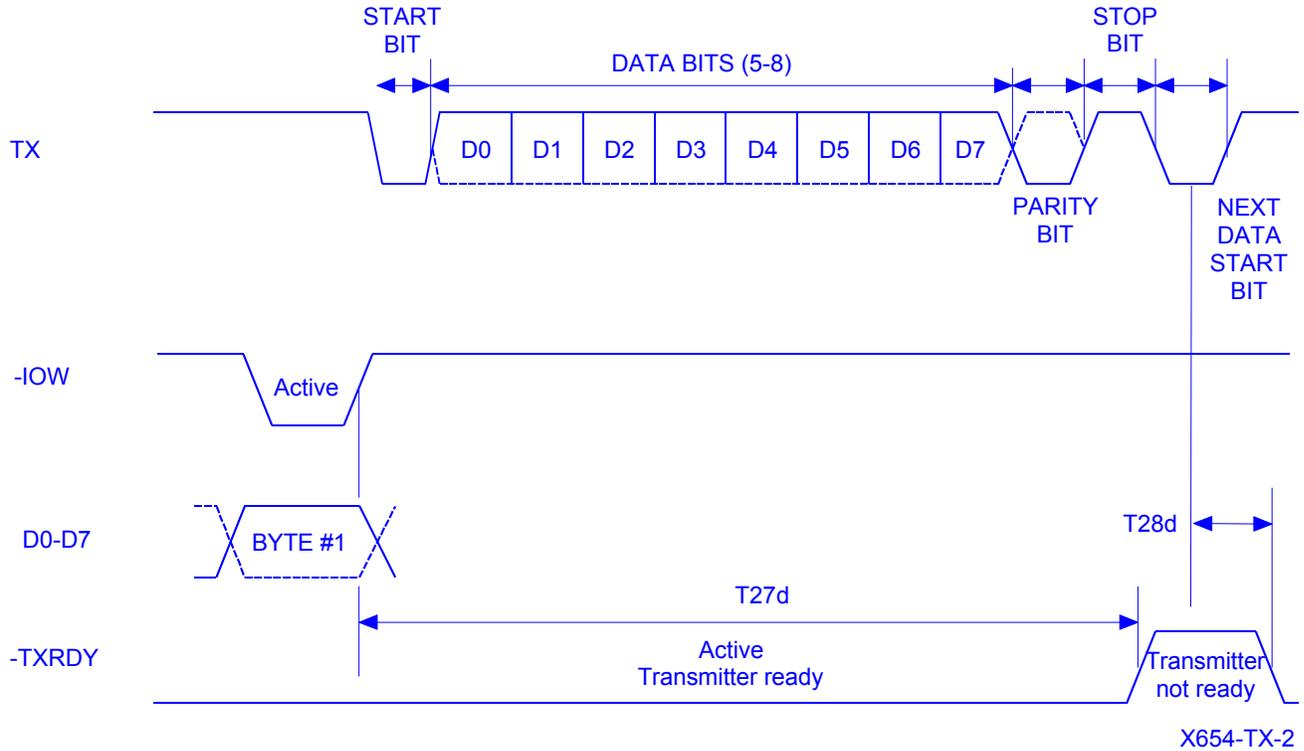
Receive ready timing in non-FIFO mode



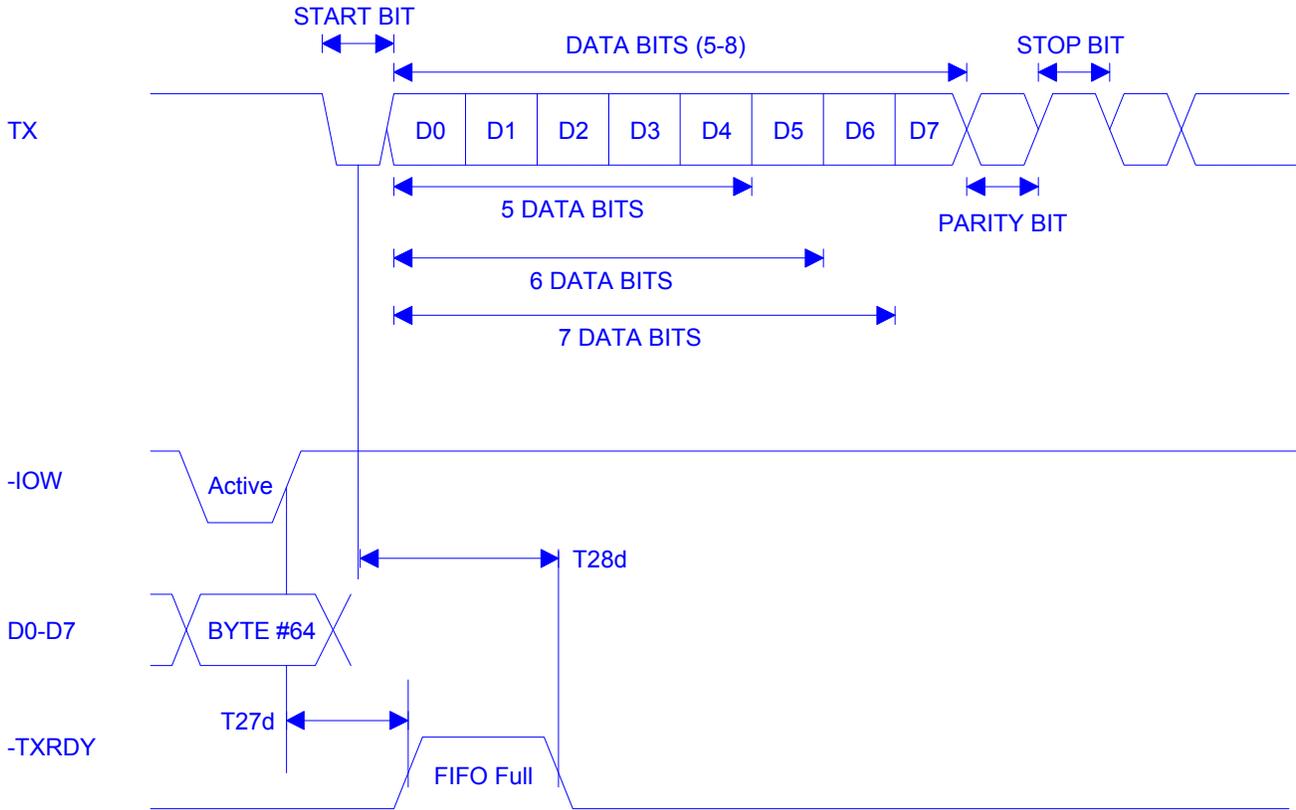
Receive timing in FIFO mode



Transmit timing

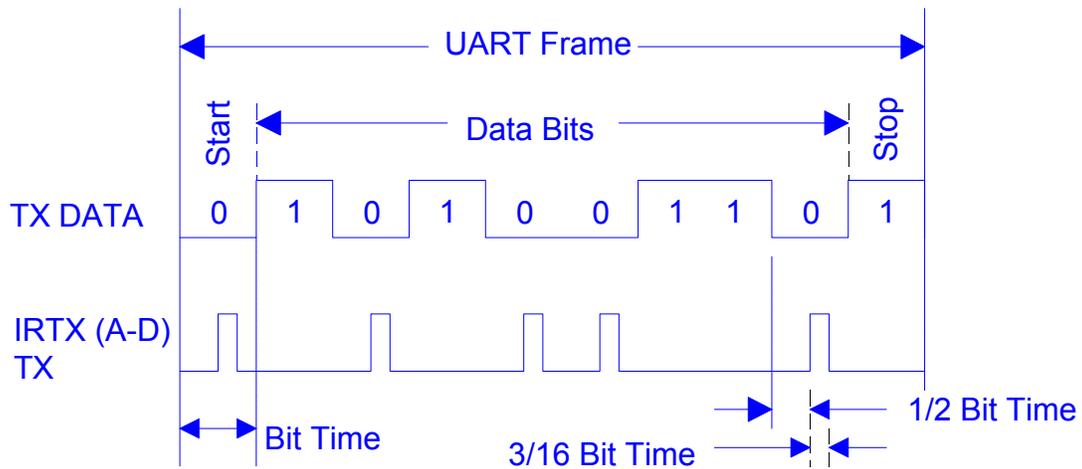


Transmit ready timing in non-FIFO mode

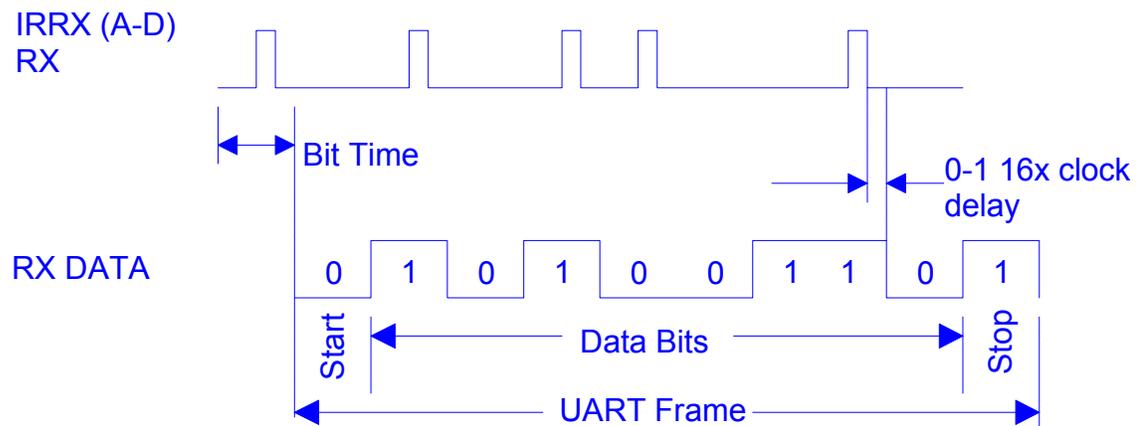


X654-TX-3

Transmit ready timing in FIFO mode



Infrared transmit timing



X654-IR-1

Infrared receive timing

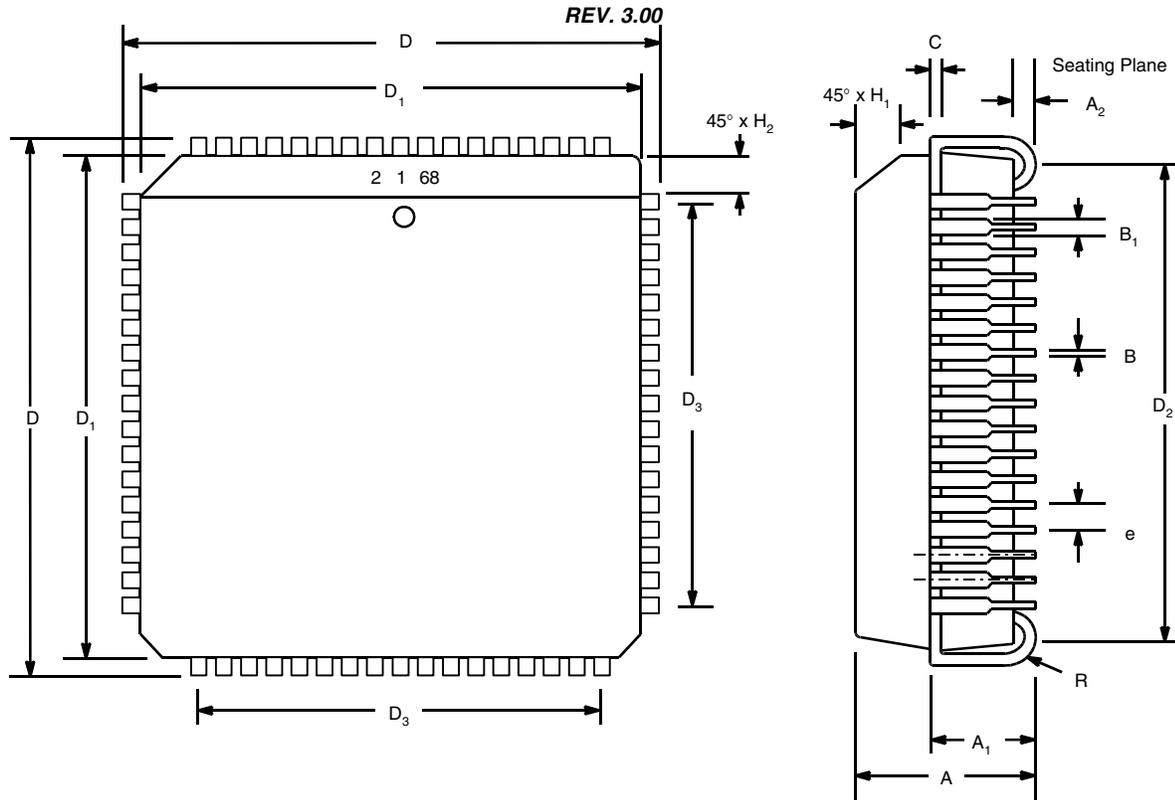


DATA SHEET REVISION HISTORY

4.40	Improved and clearer timing diagrams; better pin descriptions; clarified DMA operation; more detailed explanation of interrupt behaviour.	Sep 2001
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64 LEAD THIN QUAD FLAT PACK

(10 x 10 x 1.4 mm TQFP)



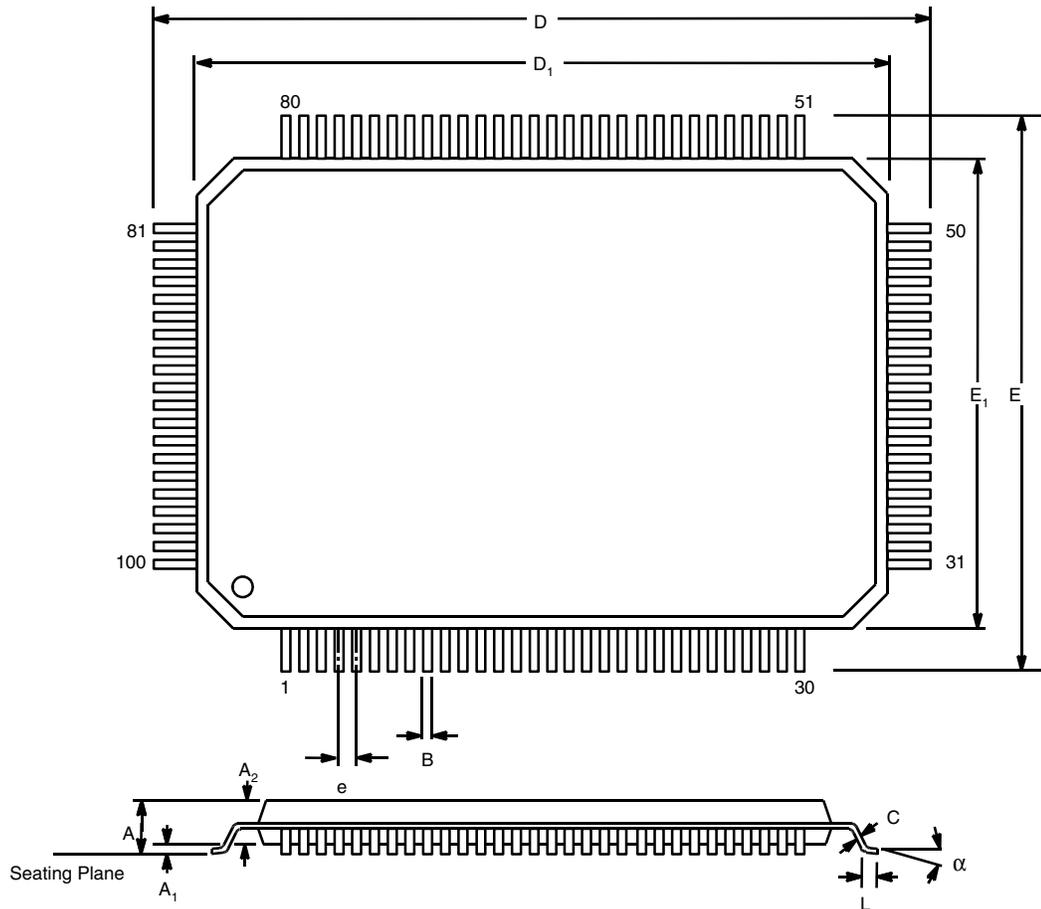
Note: The control dimension is the inch column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.200	4.19	5.08
A1	0.090	0.130	2.29	3.30
A2	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.985	0.995	25.02	25.27
D1	0.950	0.958	24.13	24.33
D2	0.890	0.930	22.61	23.62
D3	0.800 typ.		20.32 typ.	
e	0.050 BSC		1.27 BSC	
H1	0.042	0.056	1.07	1.42
H2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

100 LEAD PLASTIC QUAD FLAT PACK

(14 mm x 20 mm QFP, 1.60 mm Form)

REV. 2.00



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.134	2.55	3.40
A1	0.002	0.020	0.05	0.50
A2	0.100	0.120	2.50	2.90
B	0.009	0.016	0.22	0.40
C	0.004	0.009	0.11	0.23
D	0.904	0.923	22.95	23.45
D1	0.783	0.791	19.90	20.10
E	0.667	0.687	16.95	17.45
E1	0.547	0.555	13.90	14.10
e	0.0256 BSC		0.65 BSC	
L	0.029	0.040	0.73	1.03
α	0°	7°	0°	7°



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