.

S6C0670

8 BIT 384 / 402 CHANNEL TFT-LCD SOURCE DRIVER

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Ver. 1.0

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S6C0670 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Aug.1999
1.0	"Resistor strings" , "CLK1 pulse high period"	Mar.2000

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CONTENTS

INTRODUCTION

The S6C0670 is a 384 / 402 channel output, TFT-LCD source driver for an 256 gray scale LCD panel. Data input is based on digital input consisting of 8 bits by 6 dots, which can realize a full-color display of 16,700,000 color by output of 256 values gamma-corrected.

This device has an internal D/A (Digital-to-Analog) converter for each output and 16 (8-by-2) reference voltages. Because the output dynamic range is as large as 7.8 - 14.8 Vp-p, it is unnecessary to operate level inversion of the LCD's common electrode. Besides, to be able to deal with dot-line inversion when mounted on a single-side, output gray scale voltages with different polarity can be output to the odd number output pins and the even output pins.

S6C0670 can be adopted to larger panel, and SHL (shift direction selection) pin makes the use of the LCD panel connection conveniently. Maximum operation clock frequency is 75 MHz at 3.0 V logic operation, single edge and it can be applied to the TFT-LCD panel of UXGA standard.

FEATURES

- TFT active matrix LCD source driver LSI

- 256 G/S is possible through 16 (8 by 2) reference voltages and D/A converter

- Both dot inversion display and N-line inversion display are possible

- CMOS level input

- Compatible with gamma-correction

- Input data inversion function (DATPOL1,2)

- Single edge, Double edge compatible (DEC)

- Logic supply voltage: 2.5 - 3.6 V

- LCD driver supply voltage: 8.0 - 15.0 V

- Output dynamic range: 7.8 - 14.8 Vp-p

- Maximum operating frequency: fMAX = 75 MHz

	(internal data transmission rate at 3.0 V operation, single edge)

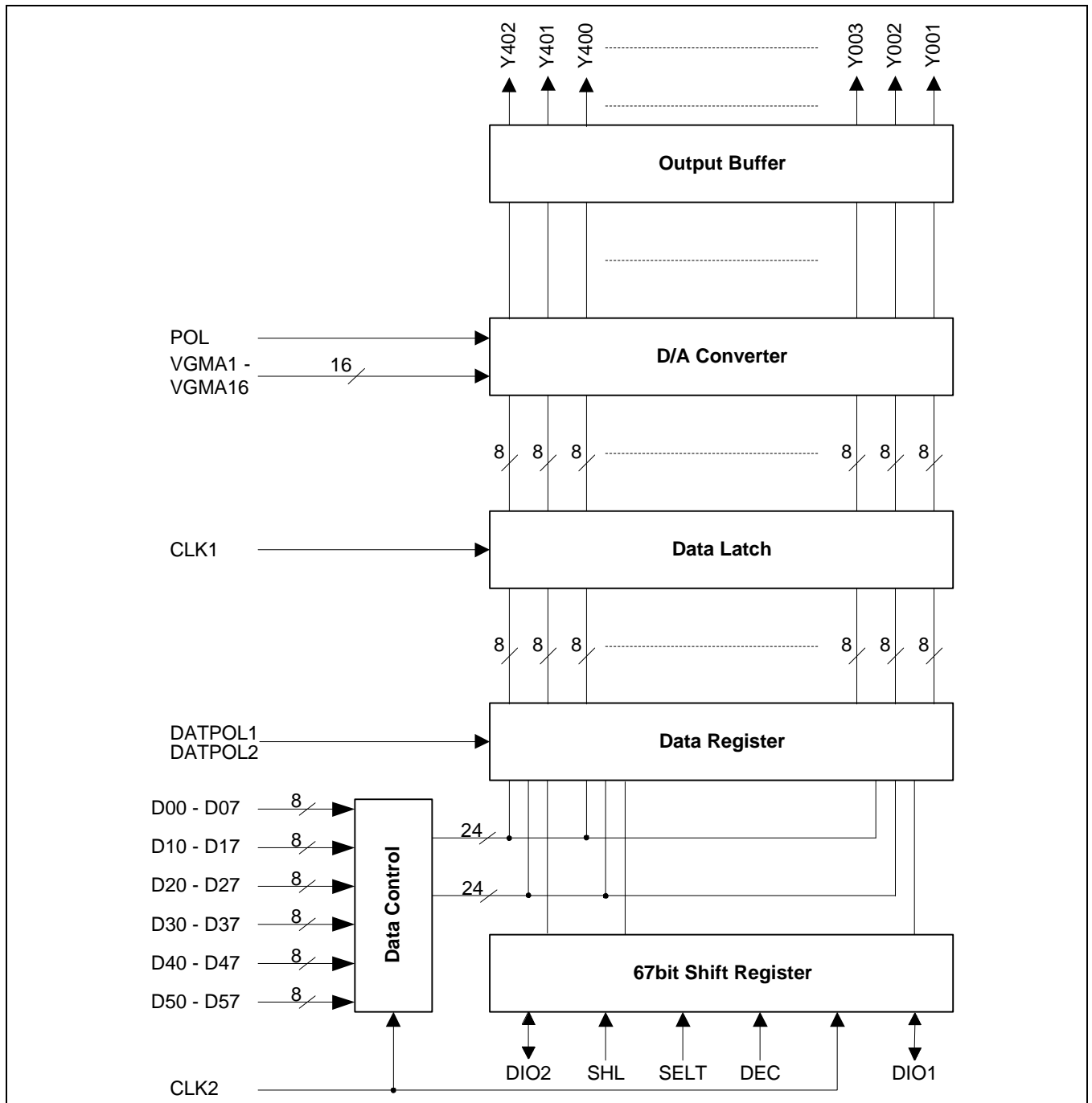- Output: 384 / 402 outputs

- TCP available

BLOCK DIAGRAM

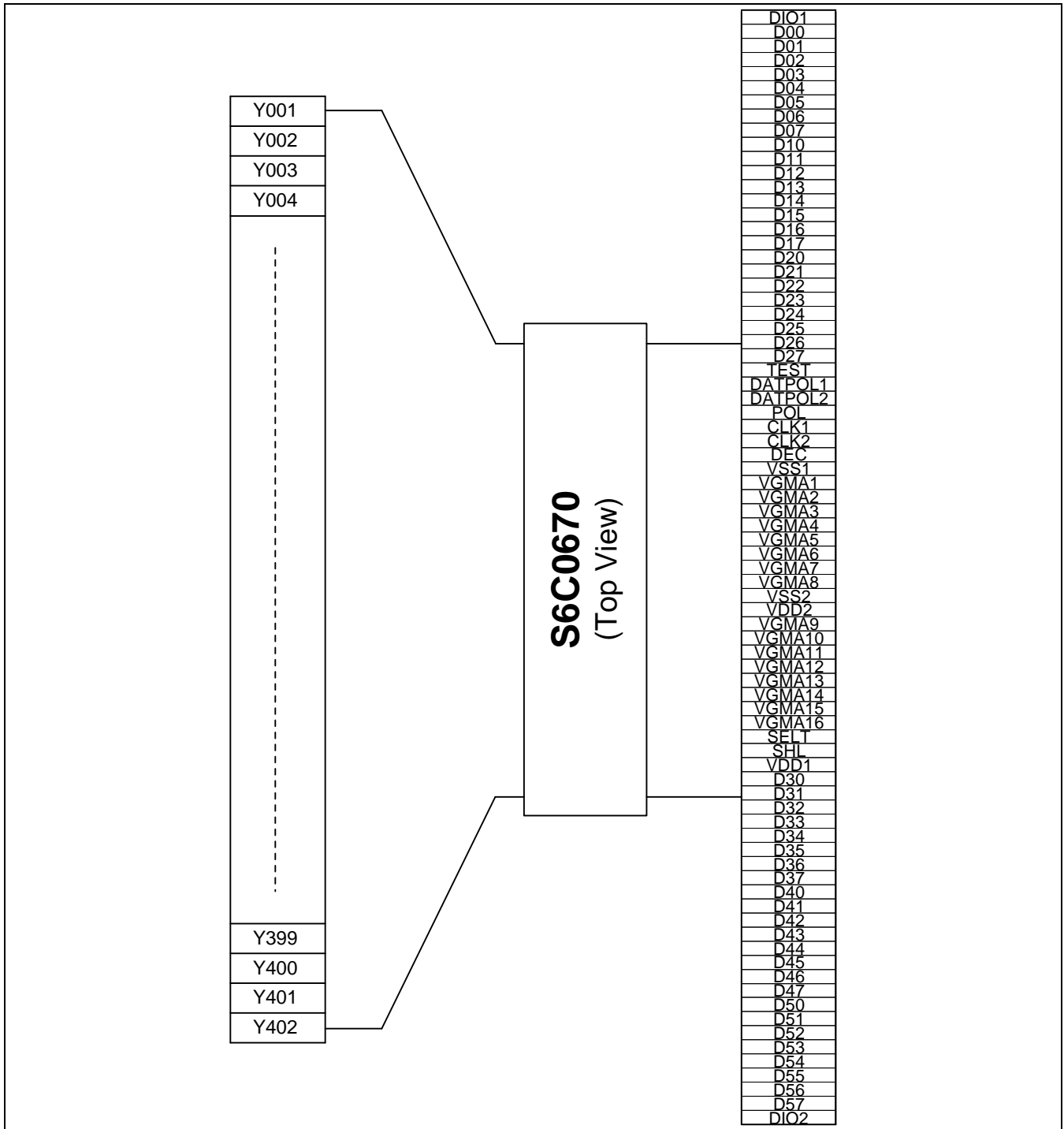

Figure 1. S6C0670 Block Diagram

PIN ASSIGNMENTS

Figure 2. S6C0670 Pin Assignments

PIN DESCRIPTIONS

Symbol	Pin Name	Description
VDD1	Logic power supply	2.5 - 3.6 V
VDD2	Driver power supply	8.0 - 15.0 V
VSS1	Logic ground	Ground (0 V)
VSS2	Driver ground	Ground (0 V)
Y1 - Y402	Driver outputs	The D/A converted 256 gray-scale analog voltage is output.
D0<0:7> - D5<0:7>	Display data input	The display data is input with a width of 48 bits, gray-scale data (8 bits) by 6 dots (R,G,B) DX0: LSB, DX7: MSB
SHL	Shift direction control input	This pin controls the direction of shift register in cascade connection. The shift direction of the shift registers is as follows. SHL = H: DIO1 input, Y1 $\rightarrow$ Y402, DIO2 output SHL = L: DIO2 input, Y402 $\rightarrow$ Y1, DIO1 output
DIO1	Start pulse input/output	SHL = H: Used as the start pulse input pin. SHL = L: Used as the start pulse output pin.
DIO2	Start pulse input/output	SHL = H: Used as the start pulse output pin. SHL = L: Used as the start pulse input pin.
DATPOL1 DATPOL2	Data inversion input	DATPOL1,2 = L: Display data is not inverted DATPOL1 = H: Display data of D0<0:7> - D2<0:7> is inverted DATPOL2 = H: Display data of D3<0:7> - D5<0:7> is inverted
POL	Polarity input	POL = H: The reference voltage for odd number outputs are VGMA9 – VGMA16 and those for even number outputs are VGMA1 – VGMA8. POL = L: The reference voltage for odd number outputs are VGMA1 – VGMA8 and those for even number outputs are VGMA9 – VGMA16.
CLK2	Shift clock input	Refer to the shift register's shift clock input. When DEC is Low, the display data is loaded to the data register at the rising edge of CLK2.When DEC is High, the display data is loaded to the data register at the rising and falling edge of CLK2.
CLK1	Latch input	Latches the contents of the data register at rising edge and transfers them to the D/A converter. Also, after CLK1 input, clears the internal shift register contents. After 1 pulse input on start, operates normally. CLK1 input timing refers to the "Relationships between CLK1 start pulse (DIO1, DIO2) and blanking period" of the switching characteristic waveform. Outputs the G/S data at falling edge.
VGMA1 – VGMA16	Gamma corrected power supplies	Input the gamma corrected power supplies from external source. VDD2 > VGMA1 > VGMA2 > …… > VGMA15 > VGMA16 > VSS2 Keep gray-scale power supply unchanged during the gray-scale voltage output.
SELT	Output selection input	SELT = L: 384 Output (Y193 - Y210 are disabled), SELT = H: 402 Output
DEC	Double edge selection input	DEC = L: Single Edge, the display data is loaded to the data register at the rising edge of CLK2. DEC = H: Double Edge, the display data is loaded to the data register at the rising and falling edge of CLK2.
TEST	Test input	TEST = L: Normal operation mode TEST = H: Test mode (OP AMP CUT-OFF, Rpd = 10kΩ)

OPERATION DESCRIPTION

DISPLAY DATA TRANSFER

(1) DEC = "L"
When DIO1 (or DIO2) pulse is loaded into internal latch on the rising edge of CLK2, DIO1 (or DIO2) pulse enables the operation of data transfer, so display data is valid on the next rising edge of CLK2. Once all the data of 402 (or 384) channels is loaded into internal latch, it goes into stand-by state automatically, and any new data is not accepted even though CLK2 is provided until next DIO1 (or DIO2) input. When next DIO1 (or DIO2) is provided, new display data is valid on the 2nd rising edge of CLK2 after the rising edge of DIO1 (or DIO2).

(2) DEC = "H"
When DIO1 (or DIO2) pulse is loaded into internal latch on the rising (or falling) edge of CLK2, DIO1 (or DIO2) pulse enables the operation of data transfer. display data is valid on the next falling (or rising) edge of CLK2. Once all the data of 402 (or 384) channels is loaded into internal latch, it goes into stand-by state automatically, and any new data is not accepted even though CLK2 is provided until next DIO1 (or DIO2) input. When next DIO1 (or DIO2) is provided, new display data is valid on the 2nd edge of CLK2 after the rising edge of DIO1 (or DIO2).

EXTENSION OF OUTPUT

Output pin can be adjusted to an extended screen by cascade connection.

(1) SHL = "L"
Connect DIO1 pin of previous stage to the DIO2 pin of next stage and all the input pins
except DIO1 and DIO2 are connected together in each device.

(2) SHL = "H"
Connect DIO2 pin of previous stage to the DIO1 pin of next stage and all the input pins
except DIO2 and DIO1 are connected together in each device.

RELATIONSHIP BETWEEN INPUT DATA VALUE AND OUTPUT VOLTAGE

The LCD drive output voltages are determined by the input data and 16 (8 by 2) gamma corrected power supplies (VGMA1 - VGMA16). Besides, to be able to deal with dot line inversion when mounted on a single-side, gradation voltages with different polarity can be output to the odd number output pins and the even number output pins. Among 8-by-2 gamma corrected voltages, input gray-scale voltages of the same polarity with respect to the common voltage, for the respective 8 gamma corrected voltages of VGMA1 - VGMA8 and VGMA9 - VGMA16.

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SHL = H

OUTPUT	Y1	Y2	Y3	......	Y400	Y401	Y402
-	First			→	Last		
DATA	D00 - D07	D10 - D17	D20 - D27	......	D30 - D37	D40 - D47	D50 - D57

SHL = L

OUTPUT	Y1	Y2	Y3	......	Y400	Y401	Y402
-	Last			←	First		
DATA	D00 - D07	D10 - D17	D20 - D27	......	D30 - D37	D40 - D47	D50 - D57
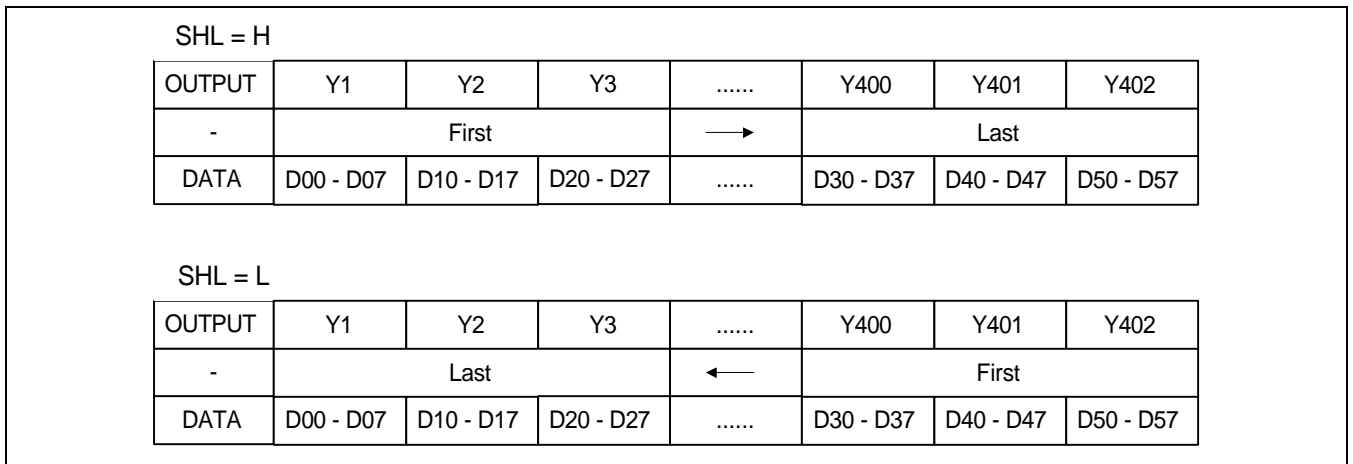
Figure 3. Relationship between Shift Direction and Output Data
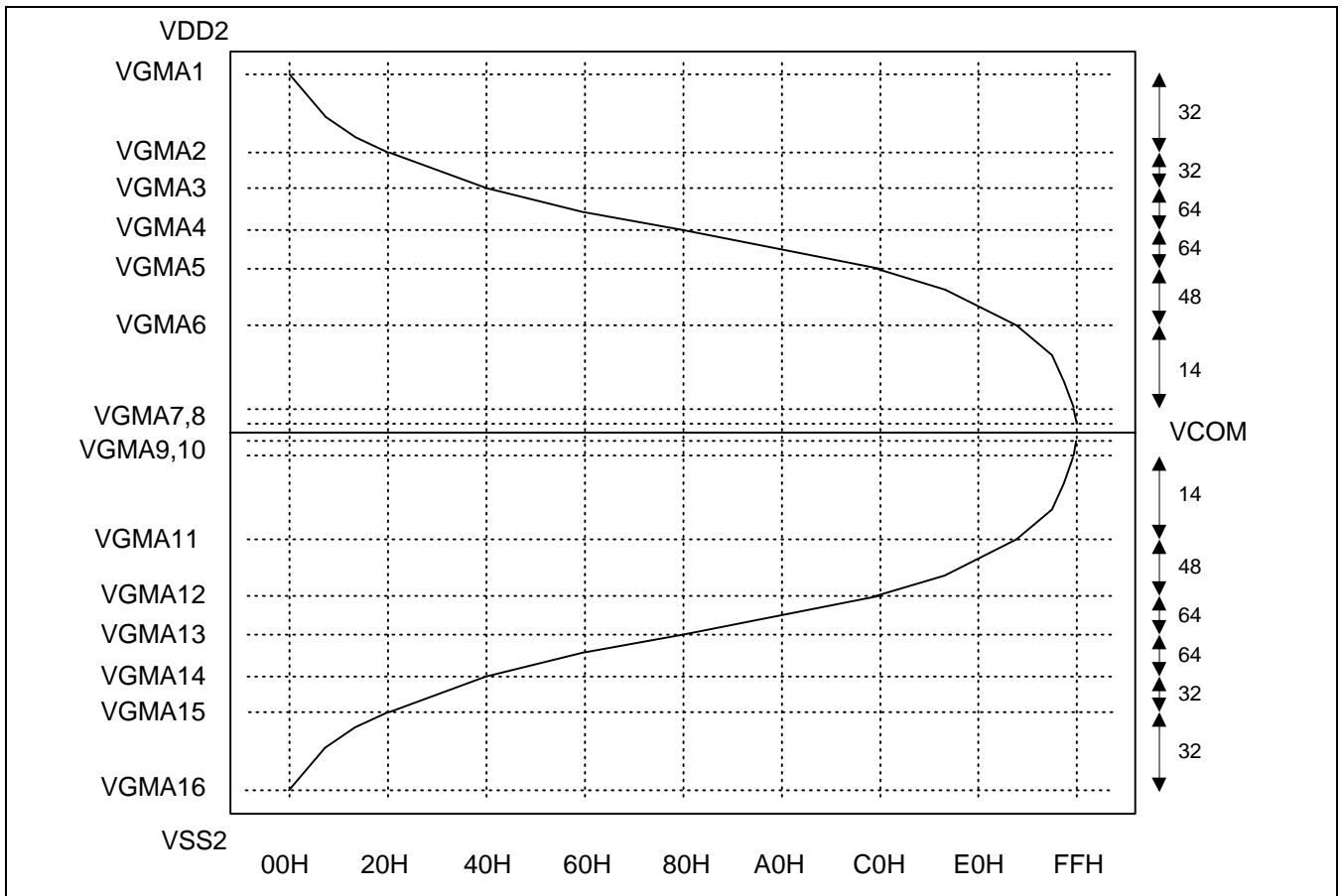
Figure 4. Gamma Correction Curve

Table 1. Resistor Strings (R0 - R254, unit: W)

Name	Value	Name	Value	Name	Value	Name	Value
R0	404	R32	74	R64	50	R96	36
R1	320	R33	73	R65	49	R97	36
R2	263	R34	72	R66	48	R98	36
R3	224	R35	72	R67	47	R99	36
R4	196	R36	71	R68	46	R100	36
R5	177	R37	71	R69	45	R101	36
R6	163	R38	71	R70	44	R102	36
R7	153	R39	70	R71	43	R103	36
R8	144	R40	70	R72	42	R104	36
R9	138	R41	69	R73	41	R105	36
R10	132	R42	69	R74	40	R106	35
R11	127	R43	69	R75	40	R107	35
R12	122	R44	68	R76	39	R108	35
R13	118	R45	68	R77	38	R109	35
R14	113	R46	67	R78	38	R110	35
R15	109	R47	67	R79	37	R111	35
R16	106	R48	66	R80	37	R112	35
R17	102	R49	65	R81	37	R113	35
R18	99	R50	65	R82	36	R114	35
R19	96	R15	64	R83	36	R115	34
R20	93	R52	63	R84	36	R116	34
R21	90	R53	62	R85	36	R117	34
R22	88	R54	61	R86	36	R118	34
R23	86	R55	60	R87	36	R119	34
R24	84	R56	59	R88	36	R120	34
R25	82	R57	58	R89	36	R121	34
R26	80	R58	57	R90	36	R122	34
R27	79	R59	56	R91	36	R123	34
R28	77	R60	55	R92	36	R124	34
R29	76	R61	53	R93	36	R125	33
R30	75	R62	52	R94	36	R126	33
R31	74	R63	51	R95	36	R127	33

Table 1. Resistor Strings (R0 - R254, unit: W) (Continued)

Name	Value	Name	Value	Name	Value	Name	Value
R128	33	R160	33	R192	38	R224	65
R129	33	R161	33	R193	39	R225	69
R130	33	R162	33	R194	39	R226	73
R131	33	R163	33	R195	39	R227	77
R132	33	R164	33	R196	40	R228	82
R133	33	R165	33	R197	40	R229	87
R134	33	R166	33	R198	40	R230	92
R135	33	R167	33	R199	41	R231	97
R136	33	R168	33	R200	41	R232	103
R137	33	R169	33	R201	41	R233	109
R138	33	R170	33	R202	42	R234	115
R139	33	R171	33	R203	42	R235	122
R140	33	R172	33	R204	42	R236	128
R141	33	R173	33	R205	42	R237	134
R142	33	R174	33	R206	43	R238	141
R143	33	R175	33	R207	43	R239	147
R144	33	R176	33	R208	43	R240	154
R145	33	R177	33	R209	43	R241	161
R146	33	R178	34	R210	44	R242	168
R147	33	R179	34	R211	44	R243	177
R148	33	R180	34	R212	45	R244	187
R149	33	R181	34	R213	45	R245	199
R150	33	R182	35	R214	46	R246	215
R151	33	R183	35	R215	47	R247	238
R152	33	R184	35	R216	48	R248	270
R153	33	R185	36	R217	49	R249	318
R154	33	R186	36	R218	51	R250	396
R155	33	R187	36	R219	52	R251	533
R156	33	R188	37	R220	54	R252	811
R157	33	R189	37	R221	56	R253	817
R158	33	R190	38	R222	59	R254	831
R159	33	R191	38	R223	62		

RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

Table 2. Relationship between Input Data and Output Voltage Value (1)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
00H	0	0	0	0	0	0	0	0	VH0	VGMA1
01H	0	0	0	0	0	0	0	1	VH1	$VGMA1 + (VGMA2 - VGMA1) \times 404 / 4288$
02H	0	0	0	0	0	0	1	0	VH2	$VGMA1 + (VGMA2 - VGMA1) \times 724 / 4288$
03H	0	0	0	0	0	0	1	1	VH3	$VGMA1 + (VGMA2 - VGMA1) \times 987 / 4288$
04H	0	0	0	0	0	1	0	0	VH4	$VGMA1 + (VGMA2 - VGMA1) \times 1211 / 4288$
05H	0	0	0	0	0	1	0	1	VH5	$VGMA1 + (VGMA2 - VGMA1) \times 1408 / 4288$
06H	0	0	0	0	0	1	1	0	VH6	$VGMA1 + (VGMA2 - VGMA1) \times 1585 / 4288$
07H	0	0	0	0	0	1	1	1	VH7	$VGMA1 + (VGMA2 - VGMA1) \times 1748 / 4288$
08H	0	0	0	0	1	0	0	0	VH8	$VGMA1 + (VGMA2 - VGMA1) \times 1900 / 4288$
09H	0	0	0	0	1	0	0	1	VH9	$VGMA1 + (VGMA2 - VGMA1) \times 2044 / 4288$
0AH	0	0	0	0	1	0	1	0	VH10	$VGMA1 + (VGMA2 - VGMA1) \times 2182 / 4288$
0BH	0	0	0	0	1	0	1	1	VH11	$VGMA1 + (VGMA2 - VGMA1) \times 2314 / 4288$
0CH	0	0	0	0	1	1	0	0	VH12	$VGMA1 + (VGMA2 - VGMA1) \times 2441 / 4288$
0DH	0	0	0	0	1	1	0	1	VH13	$VGMA1 + (VGMA2 - VGMA1) \times 2562 / 4288$
0EH	0	0	0	0	1	1	1	0	VH14	$VGMA1 + (VGMA2 - VGMA1) \times 2680 / 4288$
0FH	0	0	0	0	1	1	1	1	VH15	$VGMA1 + (VGMA2 - VGMA1) \times 2793 / 4288$
10H	0	0	0	1	0	0	0	0	VH16	$VGMA1 + (VGMA2 - VGMA1) \times 2903 / 4288$
11H	0	0	0	1	0	0	0	1	VH17	$VGMA1 + (VGMA2 - VGMA1) \times 3008 / 4288$
12H	0	0	0	1	0	0	1	0	VH18	$VGMA1 + (VGMA2 - VGMA1) \times 3110 / 4288$
13H	0	0	0	1	0	0	1	1	VH19	$VGMA1 + (VGMA2 - VGMA1) \times 3209 / 4288$
14H	0	0	0	1	0	1	0	0	VH20	$VGMA1 + (VGMA2 - VGMA1) \times 3305 / 4288$
15H	0	0	0	1	0	1	0	1	VH21	$VGMA1 + (VGMA2 - VGMA1) \times 3398 / 4288$
16H	0	0	0	1	0	1	1	0	VH22	$VGMA1 + (VGMA2 - VGMA1) \times 3488 / 4288$
17H	0	0	0	1	0	1	1	1	VH23	$VGMA1 + (VGMA2 - VGMA1) \times 3576 / 4288$
18H	0	0	0	1	1	0	0	0	VH24	$VGMA1 + (VGMA2 - VGMA1) \times 3661 / 4288$
19H	0	0	0	1	1	0	0	1	VH25	$VGMA1 + (VGMA2 - VGMA1) \times 3745 / 4288$
1AH	0	0	0	1	1	0	1	0	VH26	$VGMA1 + (VGMA2 - VGMA1) \times 3826 / 4288$
1BH	0	0	0	1	1	0	1	1	VH27	$VGMA1 + (VGMA2 - VGMA1) \times 3906 / 4288$
1CH	0	0	0	1	1	1	0	0	VH28	$VGMA1 + (VGMA2 - VGMA1) \times 3985 / 4288$
1DH	0	0	0	1	1	1	0	1	VH29	$VGMA1 + (VGMA2 - VGMA1) \times 4062 / 4288$
1EH	0	0	0	1	1	1	1	0	VH30	$VGMA1 + (VGMA2 - VGMA1) \times 4138 / 4288$
1FH	0	0	0	1	1	1	1	1	VH31	$VGMA1 + (VGMA2 - VGMA1) \times 4214 / 4288$
20H	0	0	1	0	0	0	0	0	VH32	VGMA2
21H	0	0	1	0	0	0	0	1	VH33	$VGMA2 + (VGMA3 - VGMA2) \times 74 / 2065$
22H	0	0	1	0	0	0	1	0	VH34	$VGMA2 + (VGMA3 - VGMA2) \times 147 / 2065$
23H	0	0	1	0	0	0	1	1	VH35	$VGMA2 + (VGMA3 - VGMA2) \times 219 / 2065$
24H	0	0	1	0	0	1	0	0	VH36	$VGMA2 + (VGMA3 - VGMA2) \times 291 / 2065$
25H	0	0	1	0	0	1	0	1	VH37	$VGMA2 + (VGMA3 - VGMA2) \times 362 / 2065$
26H	0	0	1	0	0	1	1	0	VH38	$VGMA2 + (VGMA3 - VGMA2) \times 433 / 2065$
27H	0	0	1	0	0	1	1	1	VH39	$VGMA2 + (VGMA3 - VGMA2) \times 504 / 2065$

NOTE: VDD2>VGMA1>VGMA2>VGMA3>VGMA4>VGMA5>VGMA6>VGMA7>VGMA8

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Table 2. Relationship between Input Data and Output Voltage Value (2)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
28H	0	0	1	0	1	0	0	0	VH40	VGMA2 + (VGMA3 - VGMA2) $\times$ 574 / 2065
29H	0	0	1	0	1	0	0	1	VH41	VGMA2 + (VGMA3 - VGMA2) $\times$ 644 / 2065
2AH	0	0	1	0	1	0	1	0	VH42	VGMA2 + (VGMA3 - VGMA2) $\times$ 713 / 2065
2BH	0	0	1	0	1	0	1	1	VH43	VGMA2 + (VGMA3 - VGMA2) $\times$ 782 / 2065
2CH	0	0	1	0	1	1	0	0	VH44	VGMA2 + (VGMA3 - VGMA2) $\times$ 851 / 2065
2DH	0	0	1	0	1	1	0	1	VH45	VGMA2 + (VGMA3 - VGMA2) $\times$ 919 / 2065
2EH	0	0	1	0	1	1	1	0	VH46	VGMA2 + (VGMA3 - VGMA2) $\times$ 987 / 2065
2FH	0	0	1	0	1	1	1	1	VH47	VGMA2 + (VGMA3 - VGMA2) $\times$ 1054 / 2065
30H	0	0	1	1	0	0	0	0	VH48	VGMA2 + (VGMA3 - VGMA2) $\times$ 1120 / 2065
31H	0	0	1	1	0	0	0	1	VH49	VGMA2 + (VGMA3 - VGMA2) $\times$ 1186 / 2065
32H	0	0	1	1	0	0	1	0	VH50	VGMA2 + (VGMA3 - VGMA2) $\times$ 1251 / 2065
33H	0	0	1	1	0	0	1	1	VH51	VGMA2 + (VGMA3 - VGMA2) $\times$ 1316 / 2065
34H	0	0	1	1	0	1	0	0	VH52	VGMA2 + (VGMA3 - VGMA2) $\times$ 1380 / 2065
35H	0	0	1	1	0	1	0	1	VH53	VGMA2 + (VGMA3 - VGMA2) $\times$ 1442 / 2065
36H	0	0	1	1	0	1	1	0	VH54	VGMA2 + (VGMA3 - VGMA2) $\times$ 1504 / 2065
37H	0	0	1	1	0	1	1	1	VH55	VGMA2 + (VGMA3 - VGMA2) $\times$ 1565 / 2065
38H	0	0	1	1	1	0	0	0	VH56	VGMA2 + (VGMA3 - VGMA2) $\times$ 1625 / 2065
39H	0	0	1	1	1	0	0	1	VH57	VGMA2 + (VGMA3 - VGMA2) $\times$ 1684 / 2065
3AH	0	0	1	1	1	0	1	0	VH58	VGMA2 + (VGMA3 - VGMA2) $\times$ 1742 / 2065
3BH	0	0	1	1	1	0	1	1	VH59	VGMA2 + (VGMA3 - VGMA2) $\times$ 1799 / 2065
3CH	0	0	1	1	1	1	0	0	VH60	VGMA2 + (VGMA3 - VGMA2) $\times$ 1854 / 2065
3DH	0	0	1	1	1	1	0	1	VH61	VGMA2 + (VGMA3 - VGMA2) $\times$ 1909 / 2065
3EH	0	0	1	1	1	1	1	0	VH62	VGMA2 + (VGMA3 - VGMA2) $\times$ 1962 / 2065
3FH	0	0	1	1	1	1	1	1	VH63	VGMA2 + (VGMA3 - VGMA2) $\times$ 2014 / 2065
40H	0	1	0	0	0	0	0	0	VH64	VGMA3
41H	0	1	0	0	0	0	0	1	VH65	VGMA3 + (VGMA4 - VGMA3) $\times$ 50 / 2368
42H	0	1	0	0	0	0	1	0	VH66	VGMA3 + (VGMA4 - VGMA3) $\times$ 99 / 2368
43H	0	1	0	0	0	0	1	1	VH67	VGMA3 + (VGMA4 - VGMA3) $\times$ 146 / 2368
44H	0	1	0	0	0	1	0	0	VH68	VGMA3 + (VGMA4 - VGMA3) $\times$ 193 / 2368
45H	0	1	0	0	0	1	0	1	VH69	VGMA3 + (VGMA4 - VGMA3) $\times$ 238 / 2368
46H	0	1	0	0	0	1	1	0	VH70	VGMA3 + (VGMA4 - VGMA3) $\times$ 283 / 2368
47H	0	1	0	0	0	1	1	1	VH71	VGMA3 + (VGMA4 - VGMA3) $\times$ 326 / 2368
48H	0	1	0	0	1	0	0	0	VH72	VGMA3 + (VGMA4 - VGMA3) $\times$ 369 / 2368
49H	0	1	0	0	1	0	0	1	VH73	VGMA3 + (VGMA4 - VGMA3) $\times$ 411 / 2368
4AH	0	1	0	0	1	0	1	0	VH74	VGMA3 + (VGMA4 - VGMA3) $\times$ 452 / 2368
4BH	0	1	0	0	1	0	1	1	VH75	VGMA3 + (VGMA4 - VGMA3) $\times$ 492 / 2368
4CH	0	1	0	0	1	1	0	0	VH76	VGMA3 + (VGMA4 - VGMA3) $\times$ 532 / 2368
4DH	0	1	0	0	1	1	0	1	VH77	VGMA3 + (VGMA4 - VGMA3) $\times$ 571 / 2368
4EH	0	1	0	0	1	1	1	0	VH78	VGMA3 + (VGMA4 - VGMA3) $\times$ 609 / 2368
4FH	0	1	0	0	1	1	1	1	VH79	VGMA3 + (VGMA4 - VGMA3) $\times$ 647 / 2368

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Table 2. Relationship between Input Data and Output Voltage Value (3)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
50H	0	1	0	1	0	0	0	0	VH80	VGMA3 + (VGMA4 - VGMA3) $\times$ 684 / 2368
51H	0	1	0	1	0	0	0	1	VH81	VGMA3 + (VGMA4 - VGMA3) $\times$ 722 / 2368
52H	0	1	0	1	0	0	1	0	VH82	VGMA3 + (VGMA4 - VGMA3) $\times$ 758 / 2368
53H	0	1	0	1	0	0	1	1	VH83	VGMA3 + (VGMA4 - VGMA3) $\times$ 795 / 2368
54H	0	1	0	1	0	1	0	0	VH84	VGMA3 + (VGMA4 - VGMA3) $\times$ 831 / 2368
55H	0	1	0	1	0	1	0	1	VH85	VGMA3 + (VGMA4 - VGMA3) $\times$ 867 / 2368
56H	0	1	0	1	0	1	1	0	VH86	VGMA3 + (VGMA4 - VGMA3) $\times$ 903 / 2368
57H	0	1	0	1	0	1	1	1	VH87	VGMA3 + (VGMA4 - VGMA3) $\times$ 938 / 2368
58H	0	1	0	1	1	0	0	0	VH88	VGMA3 + (VGMA4 - VGMA3) $\times$ 974 / 2368
59H	0	1	0	1	1	0	0	1	VH89	VGMA3 + (VGMA4 - VGMA3) $\times$ 1009 / 2368
5AH	0	1	0	1	1	0	1	0	VH90	VGMA3 + (VGMA4 - VGMA3) $\times$ 1045 / 2368
5BH	0	1	0	1	1	0	1	1	VH91	VGMA3 + (VGMA4 - VGMA3) $\times$ 1080 / 2368
5CH	0	1	0	1	1	1	0	0	VH92	VGMA3 + (VGMA4 - VGMA3) $\times$ 1116 / 2368
5DH	0	1	0	1	1	1	0	1	VH93	VGMA3 + (VGMA4 - VGMA3) $\times$ 1151 / 2368
5EH	0	1	0	1	1	1	1	0	VH94	VGMA3 + (VGMA4 - VGMA3) $\times$ 1187 / 2368
5FH	0	1	0	1	1	1	1	1	VH95	VGMA3 + (VGMA4 - VGMA3) $\times$ 1222 / 2368
60H	0	1	1	0	0	0	0	0	VH96	VGMA3 + (VGMA4 - VGMA3) $\times$ 1258 / 2368
61H	0	1	1	0	0	0	0	1	VH97	VGMA3 + (VGMA4 - VGMA3) $\times$ 1294 / 2368
62H	0	1	1	0	0	0	1	0	VH98	VGMA3 + (VGMA4 - VGMA3) $\times$ 1329 / 2368
63H	0	1	1	0	0	0	1	1	VH99	VGMA3 + (VGMA4 - VGMA3) $\times$ 1365 / 2368
64H	0	1	1	0	0	1	0	0	VH100	VGMA3 + (VGMA4 - VGMA3) $\times$ 1401 / 2368
65H	0	1	1	0	0	1	0	1	VH101	VGMA3 + (VGMA4 - VGMA3) $\times$ 1436 / 2368
66H	0	1	1	0	0	1	1	0	VH102	VGMA3 + (VGMA4 - VGMA3) $\times$ 1472 / 2368
67H	0	1	1	0	0	1	1	1	VH103	VGMA3 + (VGMA4 - VGMA3) $\times$ 1507 / 2368
68H	0	1	1	0	1	0	0	0	VH104	VGMA3 + (VGMA4 - VGMA3) $\times$ 1543 / 2368
69H	0	1	1	0	1	0	0	1	VH105	VGMA3 + (VGMA4 - VGMA3) $\times$ 1579 / 2368
6AH	0	1	1	0	1	0	1	0	VH106	VGMA3 + (VGMA4 - VGMA3) $\times$ 1614 / 2368
6BH	0	1	1	0	1	0	1	1	VH107	VGMA3 + (VGMA4 - VGMA3) $\times$ 1649 / 2368
6CH	0	1	1	0	1	1	0	0	VH108	VGMA3 + (VGMA4 - VGMA3) $\times$ 1685 / 2368
6DH	0	1	1	0	1	1	0	1	VH109	VGMA3 + (VGMA4 - VGMA3) $\times$ 1720 / 2368
6EH	0	1	1	0	1	1	1	0	VH110	VGMA3 + (VGMA4 - VGMA3) $\times$ 1755 / 2368
6FH	0	1	1	0	1	1	1	1	VH111	VGMA3 + (VGMA4 - VGMA3) $\times$ 1790 / 2368
70H	0	1	1	1	0	0	0	0	VH112	VGMA3 + (VGMA4 - VGMA3) $\times$ 1825 / 2368
71H	0	1	1	1	0	0	0	1	VH113	VGMA3 + (VGMA4 - VGMA3) $\times$ 1860 / 2368
72H	0	1	1	1	0	0	1	0	VH114	VGMA3 + (VGMA4 - VGMA3) $\times$ 1895 / 2368
73H	0	1	1	1	0	0	1	1	VH115	VGMA3 + (VGMA4 - VGMA3) $\times$ 1929 / 2368
74H	0	1	1	1	0	1	0	0	VH116	VGMA3 + (VGMA4 - VGMA3) $\times$ 1964 / 2368
75H	0	1	1	1	0	1	0	1	VH117	VGMA3 + (VGMA4 - VGMA3) $\times$ 1998 / 2368
76H	0	1	1	1	0	1	1	0	VH118	VGMA3 + (VGMA4 - VGMA3) $\times$ 2032 / 2368
77H	0	1	1	1	0	1	1	1	VH119	VGMA3 + (VGMA4 - VGMA3) $\times$ 2066 / 2368

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Table 2. Relationship between Input Data and Output Voltage Value (4)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
78H	0	1	1	1	1	0	0	0	VH120	VGMA3 + (VGMA4 - VGMA3) × 2100 / 2368
79H	0	1	1	1	1	0	0	1	VH121	VGMA3 + (VGMA4 - VGMA3) × 2134 / 2368
7AH	0	1	1	1	1	0	1	0	VH122	VGMA3 + (VGMA4 - VGMA3) × 2168 / 2368
7BH	0	1	1	1	1	0	1	1	VH123	VGMA3 + (VGMA4 - VGMA3) × 2201 / 2368
7CH	0	1	1	1	1	1	0	0	VH124	VGMA3 + (VGMA4 - VGMA3) × 2235 / 2368
7DH	0	1	1	1	1	1	0	1	VH125	VGMA3 + (VGMA4 - VGMA3) × 2268 / 2368
7EH	0	1	1	1	1	1	1	0	VH126	VGMA3 + (VGMA4 - VGMA3) × 2302 / 2368
7FH	0	1	1	1	1	1	1	1	VH127	VGMA3 + (VGMA4 - VGMA3) × 2335 / 2368
80H	1	0	0	0	0	0	0	0	VH128	VGMA4
81H	1	0	0	0	0	0	0	1	VH129	VGMA4 + (VGMA5 - VGMA4) × 33 / 2149
82H	1	0	0	0	0	0	1	0	VH130	VGMA4 + (VGMA5 - VGMA4) × 66 / 2149
83H	1	0	0	0	0	0	1	1	VH131	VGMA4 + (VGMA5 - VGMA4) × 100 / 2149
84H	1	0	0	0	0	1	0	0	VH132	VGMA4 + (VGMA5 - VGMA4) × 133 / 2149
85H	1	0	0	0	0	1	0	1	VH133	VGMA4 + (VGMA5 - VGMA4) × 166 / 2149
86H	1	0	0	0	0	1	1	0	VH134	VGMA4 + (VGMA5 - VGMA4) × 199 / 2149
87H	1	0	0	0	0	1	1	1	VH135	VGMA4 + (VGMA5 - VGMA4) × 232 / 2149
88H	1	0	0	0	1	0	0	0	VH136	VGMA4 + (VGMA5 - VGMA4) × 266 / 2149
89H	1	0	0	0	1	0	0	1	VH137	VGMA4 + (VGMA5 - VGMA4) × 299 / 2149
8AH	1	0	0	0	1	0	1	0	VH138	VGMA4 + (VGMA5 - VGMA4) × 332 / 2149
8BH	1	0	0	0	1	0	1	1	VH139	VGMA4 + (VGMA5 - VGMA4) × 365 / 2149
8CH	1	0	0	0	1	1	0	0	VH140	VGMA4 + (VGMA5 - VGMA4) × 399 / 2149
8DH	1	0	0	0	1	1	0	1	VH141	VGMA4 + (VGMA5 - VGMA4) × 432 / 2149
8EH	1	0	0	0	1	1	1	0	VH142	VGMA4 + (VGMA5 - VGMA4) × 465 / 2149
8FH	1	0	0	0	1	1	1	1	VH143	VGMA4 + (VGMA5 - VGMA4) × 498 / 2149
90H	1	0	0	1	0	0	0	0	VH144	VGMA4 + (VGMA5 - VGMA4) × 532 / 2149
91H	1	0	0	1	0	0	0	1	VH145	VGMA4 + (VGMA5 - VGMA4) × 565 / 2149
92H	1	0	0	1	0	0	1	0	VH146	VGMA4 + (VGMA5 - VGMA4) × 598 / 2149
93H	1	0	0	1	0	0	1	1	VH147	VGMA4 + (VGMA5 - VGMA4) × 632 / 2149
94H	1	0	0	1	0	1	0	0	VH148	VGMA4 + (VGMA5 - VGMA4) × 665 / 2149
95H	1	0	0	1	0	1	0	1	VH149	VGMA4 + (VGMA5 - Value4) × 698 / 2149
96H	1	0	0	1	0	1	1	0	VH150	VGMA4 + (VGMA5 - VGMA4) × 732 / 2149
97H	1	0	0	1	0	1	1	1	VH151	VGMA4 + (VGMA5 - VGMA4) × 765 / 2149
98H	1	0	0	1	1	0	0	0	VH152	VGMA4 + (VGMA5 - VGMA4) × 798 / 2149
99H	1	0	0	1	1	0	0	1	VH153	VGMA4 + (VGMA5 - VGMA4) × 831 / 2149
9AH	1	0	0	1	1	0	1	0	VH154	VGMA4 + (VGMA5 - VGMA4) × 864 / 2149
9BH	1	0	0	1	1	0	1	1	VH155	VGMA4 + (VGMA5 - VGMA4) × 897 / 2149
9CH	1	0	0	1	1	1	0	0	VH156	VGMA4 + (VGMA5 - VGMA4) × 930 / 2149
9DH	1	0	0	1	1	1	0	1	VH157	VGMA4 + (VGMA5 - VGMA4) × 963 / 2149
9EH	1	0	0	1	1	1	1	0	VH158	VGMA4 + (VGMA5 - VGMA4) × 996 / 2149
9FH	1	0	0	1	1	1	1	1	VH159	VGMA4 + (VGMA5 - VGMA4) × 1029 / 2149

Table 2. Relationship between Input Data and Output Voltage Value (5)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
A0H	1	0	1	0	0	0	0	0	VH160	VGMA4 + (VGMA5 - VGMA4) $\times$ 1062 / 2149
A1H	1	0	1	0	0	0	0	1	VH161	VGMA4 + (VGMA5 - VGMA4) $\times$ 1094 / 2149
A2H	1	0	1	0	0	0	1	0	VH162	VGMA4 + (VGMA5 - VGMA4) $\times$ 1127 / 2149
A3H	1	0	1	0	0	0	1	1	VH163	VGMA4 + (VGMA5 - VGMA4) $\times$ 1159 / 2149
A4H	1	0	1	0	0	1	0	0	VH164	VGMA4 + (VGMA5 - VGMA4) $\times$ 1192 / 2149
A5H	1	0	1	0	0	1	0	1	VH165	VGMA4 + (VGMA5 - VGMA4) $\times$ 1224 / 2149
A6H	1	0	1	0	0	1	1	0	VH166	VGMA4 + (VGMA5 - VGMA4) $\times$ 1257 / 2149
A7H	1	0	1	0	0	1	1	1	VH167	VGMA4 + (VGMA5 - VGMA4) $\times$ 1289 / 2149
A8H	1	0	1	0	1	0	0	0	VH168	VGMA4 + (VGMA5 - VGMA4) $\times$ 1322 / 2149
A9H	1	0	1	0	1	0	0	1	VH169	VGMA4 + (VGMA5 - VGMA4) $\times$ 1354 / 2149
AAH	1	0	1	0	1	0	1	0	VH170	VGMA4 + (VGMA5 - VGMA4) $\times$ 1387 / 2149
ABH	1	0	1	0	1	0	1	1	VH171	VGMA4 + (VGMA5 - VGMA4) $\times$ 1419 / 2149
ACH	1	0	1	0	1	1	0	0	VH172	VGMA4 + (VGMA5 - VGMA4) $\times$ 1452 / 2149
ADH	1	0	1	0	1	1	0	1	VH173	VGMA4 + (VGMA5 - VGMA4) $\times$ 1485 / 2149
AEH	1	0	1	0	1	1	1	0	VH174	VGMA4 + (VGMA5 - VGMA4) $\times$ 1517 / 2149
AFH	1	0	1	0	1	1	1	1	VH175	VGMA4 + (VGMA5 - VGMA4) $\times$ 1550 / 2149
B0H	1	0	1	1	0	0	0	0	VH176	VGMA4 + (VGMA5 - VGMA4) $\times$ 1583 / 2149
B1H	1	0	1	1	0	0	0	1	VH177	VGMA4 + (VGMA5 - VGMA4) $\times$ 1617 / 2149
B2H	1	0	1	1	0	0	1	0	VH178	VGMA4 + (VGMA5 - VGMA4) $\times$ 1650 / 2149
B3H	1	0	1	1	0	0	1	1	VH179	VGMA4 + (VGMA5 - VGMA4) $\times$ 1684 / 2149
B4H	1	0	1	1	0	1	0	0	VH180	VGMA4 + (VGMA5 - VGMA4) $\times$ 1717 / 2149
B5H	1	0	1	1	0	1	0	1	VH181	VGMA4 + (VGMA5 - VGMA4) $\times$ 1752 / 2149
B6H	1	0	1	1	0	1	1	0	VH182	VGMA4 + (VGMA5 - VGMA4) $\times$ 1786 / 2149
B7H	1	0	1	1	0	1	1	1	VH183	VGMA4 + (VGMA5 - VGMA4) $\times$ 1821 / 2149
B8H	1	0	1	1	1	0	0	0	VH184	VGMA4 + (VGMA5 - VGMA4) $\times$ 1856 / 2149
B9H	1	0	1	1	1	0	0	1	VH185	VGMA4 + (VGMA5 - VGMA4) $\times$ 1891 / 2149
BAH	1	0	1	1	1	0	1	0	VH186	VGMA4 + (VGMA5 - VGMA4) $\times$ 1927 / 2149
BBH	1	0	1	1	1	0	1	1	VH187	VGMA4 + (VGMA5 - VGMA4) $\times$ 1963 / 2149
BCH	1	0	1	1	1	1	0	0	VH188	VGMA4 + (VGMA5 - VGMA4) $\times$ 1999 / 2149
BDH	1	0	1	1	1	1	0	1	VH189	VGMA4 + (VGMA5 - Value4) $\times$ 2036 / 2149
BEH	1	0	1	1	1	1	1	0	VH190	VGMA4 + (VGMA5 - VGMA4) $\times$ 2073 / 2149
BFH	1	0	1	1	1	1	1	1	VH191	VGMA4 + (VGMA5 - VGMA4) $\times$ 2111 / 2149
C0H	1	1	0	0	0	0	0	0	VH192	VGMA5
C1H	1	1	0	0	0	0	0	1	VH193	VGMA5 + (VGMA6 - VGMA5) $\times$ 38 / 3080
C2H	1	1	0	0	0	0	1	0	VH194	VGMA5 + (VGMA6 - VGMA5) $\times$ 77 / 3080
C3H	1	1	0	0	0	0	1	1	VH195	VGMA5 + (VGMA6 - VGMA5) $\times$ 116 / 3080
C4H	1	1	0	0	0	1	0	0	VH196	VGMA5 + (VGMA6 - VGMA5) $\times$ 155 / 3080
C5H	1	1	0	0	0	1	0	1	VH197	VGMA5 + (VGMA6 - VGMA5) $\times$ 195 / 3080
C6H	1	1	0	0	0	1	1	0	VH198	VGMA5 + (VGMA6 - VGMA5) $\times$ 235 / 3080
C7H	1	1	0	0	0	1	1	1	VH199	VGMA5 + (VGMA6 - VGMA5) $\times$ 276 / 3080

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Table 2. Relationship between Input Data and Output Voltage Value (6)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
C8H	1	1	0	0	1	0	0	0	VH200	$VGMA5 + (VGMA6 - VGMA5) \times 316 / 3080$
C9H	1	1	0	0	1	0	0	1	VH201	$VGMA5 + (VGMA6 - VGMA5) \times 357 / 3080$
CAH	1	1	0	0	1	0	1	0	VH202	$VGMA5 + (VGMA6 - VGMA5) \times 399 / 3080$
CBH	1	1	0	0	1	0	1	1	VH203	$VGMA5 + (VGMA6 - VGMA5) \times 440 / 3080$
CCH	1	1	0	0	1	1	0	0	VH204	$VGMA5 + (VGMA6 - VGMA5) \times 482 / 3080$
CDH	1	1	0	0	1	1	0	1	VH205	$VGMA5 + (VGMA6 - VGMA5) \times 524 / 3080$
CEH	1	1	0	0	1	1	1	0	VH206	$VGMA5 + (VGMA6 - VGMA5) \times 566 / 3080$
CFH	1	1	0	0	1	1	1	1	VH207	$VGMA5 + (VGMA6 - VGMA5) \times 609 / 3080$
D0H	1	1	0	1	0	0	0	0	VH208	$VGMA5 + (VGMA6 - VGMA5) \times 651 / 3080$
D1H	1	1	0	1	0	0	0	1	VH209	$VGMA5 + (VGMA6 - VGMA5) \times 694 / 3080$
D2H	1	1	0	1	0	0	1	0	VH210	$VGMA5 + (VGMA6 - VGMA5) \times 738 / 3080$
D3H	1	1	0	1	0	0	1	1	VH211	$VGMA5 + (VGMA6 - VGMA5) \times 782 / 3080$
D4H	1	1	0	1	0	1	0	0	VH212	$VGMA5 + (VGMA6 - VGMA5) \times 826 / 3080$
D5H	1	1	0	1	0	1	0	1	VH213	$VGMA5 + (VGMA6 - VGMA5) \times 871 / 3080$
D6H	1	1	0	1	0	1	1	0	VH214	$VGMA5 + (VGMA6 - VGMA5) \times 916 / 3080$
D7H	1	1	0	1	0	1	1	1	VH215	$VGMA5 + (VGMA6 - VGMA5) \times 962 / 3080$
D8H	1	1	0	1	1	0	0	0	VH216	$VGMA5 + (VGMA6 - VGMA5) \times 1009 / 3080$
D9H	1	1	0	1	1	0	0	1	VH217	$VGMA5 + (VGMA6 - VGMA5) \times 1057 / 3080$
DAH	1	1	0	1	1	0	1	0	VH218	$VGMA5 + (VGMA6 - VGMA5) \times 1106 / 3080$
DBH	1	1	0	1	1	0	1	1	VH219	$VGMA5 + (VGMA6 - VGMA5) \times 1157 / 3080$
DCH	1	1	0	1	1	1	0	0	VH220	$VGMA5 + (VGMA6 - VGMA5) \times 1209 / 3080$
DDH	1	1	0	1	1	1	0	1	VH221	$VGMA5 + (VGMA6 - VGMA5) \times 1263 / 3080$
DEH	1	1	0	1	1	1	1	0	VH222	$VGMA5 + (VGMA6 - VGMA5) \times 1320 / 3080$
DFH	1	1	0	1	1	1	1	1	VH223	$VGMA5 + (VGMA6 - VGMA5) \times 1379 / 3080$
E0H	1	1	1	0	0	0	0	0	VH224	$VGMA5 + (VGMA6 - VGMA5) \times 1441 / 3080$
E1H	1	1	1	0	0	0	0	1	VH225	$VGMA5 + (VGMA6 - VGMA5) \times 1506 / 3080$
E2H	1	1	1	0	0	0	1	0	VH226	$VGMA5 + (VGMA6 - VGMA5) \times 1574 / 3080$
E3H	1	1	1	0	0	0	1	1	VH227	$VGMA5 + (VGMA6 - VGMA5) \times 1647 / 3080$
E4H	1	1	1	0	0	1	0	0	VH228	$VGMA5 + (VGMA6 - VGMA5) \times 1724 / 3080$
E5H	1	1	1	0	0	1	0	1	VH229	$VGMA5 + (VGMA6 - VGMA5) \times 1805 / 3080$
E6H	1	1	1	0	0	1	1	0	VH230	$VGMA5 + (VGMA6 - VGMA5) \times 1892 / 3080$
E7H	1	1	1	0	0	1	1	1	VH231	$VGMA5 + (VGMA6 - VGMA5) \times 1983 / 3080$
E8H	1	1	1	0	1	0	0	0	VH232	$VGMA5 + (VGMA6 - VGMA5) \times 2081 / 3080$
E9H	1	1	1	0	1	0	0	1	VH233	$VGMA5 + (VGMA6 - VGMA5) \times 2184 / 3080$
EAH	1	1	1	0	1	0	1	0	VH234	$VGMA5 + (VGMA6 - VGMA5) \times 2293 / 3080$
EBH	1	1	1	0	1	0	1	1	VH235	$VGMA5 + (VGMA6 - VGMA5) \times 2409 / 3080$
ECH	1	1	1	0	1	1	0	0	VH236	$VGMA5 + (VGMA6 - VGMA5) \times 2530 / 3080$
EDH	1	1	1	0	1	1	0	1	VH237	$VGMA5 + (VGMA6 - VGMA5) \times 2658 / 3080$
EEH	1	1	1	0	1	1	1	0	VH238	$VGMA5 + (VGMA6 - VGMA5) \times 2792 / 3080$
EFH	1	1	1	0	1	1	1	1	VH239	$VGMA5 + (VGMA6 - VGMA5) \times 2933 / 3080$

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Table 2. Relationship between Input Data and Output Voltage Value (7)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
F0H	1	1	1	1	0	0	0	0	VH240	VGMA6
F1H	1	1	1	1	0	0	0	1	VH241	VGMA6 + (VGMA7 - VGMA6) $\times$ 154 / 4641
F2H	1	1	1	1	0	0	1	0	VH242	VGMA6 + (VGMA7 - VGMA6) $\times$ 314 / 4641
F3H	1	1	1	1	0	0	1	1	VH243	VGMA6 + (VGMA7 - VGMA6) $\times$ 482 / 4641
F4H	1	1	1	1	0	1	0	0	VH244	VGMA6 + (VGMA7 - VGMA6) $\times$ 659 / 4641
F5H	1	1	1	1	0	1	0	1	VH245	VGMA6 + (VGMA7 - VGMA6) $\times$ 846 / 4641
F6H	1	1	1	1	0	1	1	0	VH246	VGMA6 + (VGMA7 - VGMA6) $\times$ 1045 / 4641
F7H	1	1	1	1	0	1	1	1	VH247	VGMA6 + (VGMA7 - VGMA6) $\times$ 1260 / 4641
F8H	1	1	1	1	1	0	0	0	VH248	VGMA6 + (VGMA7 - VGMA6) $\times$ 1498 / 4641
F9H	1	1	1	1	1	0	0	1	VH249	VGMA6 + (VGMA7 - VGMA6) $\times$ 1768 / 4641
FAH	1	1	1	1	1	0	1	0	VH250	VGMA6 + (VGMA7 - VGMA6) $\times$ 2086 / 4641
FBH	1	1	1	1	1	0	1	1	VH251	VGMA6 + (VGMA7 - VGMA6) $\times$ 2482 / 4641
FCH	1	1	1	1	1	1	0	0	VH252	VGMA6 + (VGMA7 - VGMA6) $\times$ 3014 / 4641
FDH	1	1	1	1	1	1	0	1	VH253	VGMA6 + (VGMA7 - VGMA6) $\times$ 3825 / 4641
FEH	1	1	1	1	1	1	1	0	VH254	VGMA7
FFH	1	1	1	1	1	1	1	1	VH255	VGMA8

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Table 2. Relationship between Input Data and Output Voltage Value (8)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
00H	0	0	0	0	0	0	0	0	VL0	VGMA16
01H	0	0	0	0	0	0	0	1	VL1	$VGMA16 + (VGMA15 - VGMA16) \times 404 / 4288$
02H	0	0	0	0	0	0	1	0	VL2	$VGMA16 + (VGMA15 - VGMA16) \times 724 / 4288$
03H	0	0	0	0	0	0	1	1	VL3	$VGMA16 + (VGMA15 - VGMA16) \times 987 / 4288$
04H	0	0	0	0	0	1	0	0	VL4	$VGMA16 + (VGMA15 - VGMA16) \times 1211 / 4288$
05H	0	0	0	0	0	1	0	1	VL5	$VGMA16 + (VGMA15 - VGMA16) \times 1408 / 4288$
06H	0	0	0	0	0	1	1	0	VL6	$VGMA16 + (VGMA15 - VGMA16) \times 1585 / 4288$
07H	0	0	0	0	0	1	1	1	VL7	$VGMA16 + (VGMA15 - VGMA16) \times 1748 / 4288$
08H	0	0	0	0	1	0	0	0	VL8	$VGMA16 + (VGMA15 - VGMA16) \times 1900 / 4288$
09H	0	0	0	0	1	0	0	1	VL9	$VGMA16 + (VGMA15 - VGMA16) \times 2044 / 4288$
0AH	0	0	0	0	1	0	1	0	VL10	$VGMA16 + (VGMA15 - VGMA16) \times 2182 / 4288$
0BH	0	0	0	0	1	0	1	1	VL11	$VGMA16 + (VGMA15 - VGMA16) \times 2314 / 4288$
0CH	0	0	0	0	1	1	0	0	VL12	$VGMA16 + (VGMA15 - VGMA16) \times 2441 / 4288$
0DH	0	0	0	0	1	1	0	1	VL13	$VGMA16 + (VGMA15 - VGMA16) \times 2562 / 4288$
0EH	0	0	0	0	1	1	1	0	VL14	$VGMA16 + (VGMA15 - VGMA16) \times 2680 / 4288$
0FH	0	0	0	0	1	1	1	1	VL15	$VGMA16 + (VGMA15 - VGMA16) \times 2793 / 4288$
10H	0	0	0	1	0	0	0	0	VL16	$VGMA16 + (VGMA15 - VGMA16) \times 2903 / 4288$
11H	0	0	0	1	0	0	0	1	VL17	$VGMA16 + (VGMA15 - VGMA16) \times 3008 / 4288$
12H	0	0	0	1	0	0	1	0	VL18	$VGMA16 + (VGMA15 - VGMA16) \times 3110 / 4288$
13H	0	0	0	1	0	0	1	1	VL19	$VGMA16 + (VGMA15 - VGMA16) \times 3209 / 4288$
14H	0	0	0	1	0	1	0	0	VL20	$VGMA16 + (VGMA15 - VGMA16) \times 3305 / 4288$
15H	0	0	0	1	0	1	0	1	VL21	$VGMA16 + (VGMA15 - VGMA16) \times 3398 / 4288$
16H	0	0	0	1	0	1	1	0	VL22	$VGMA16 + (VGMA15 - VGMA16) \times 3488 / 4288$
17H	0	0	0	1	0	1	1	1	VL23	$VGMA16 + (VGMA15 - VGMA16) \times 3576 / 4288$
18H	0	0	0	1	1	0	0	0	VL24	$VGMA16 + (VGMA15 - VGMA16) \times 3661 / 4288$
19H	0	0	0	1	1	0	0	1	VL25	$VGMA16 + (VGMA15 - VGMA16) \times 3745 / 4288$
1AH	0	0	0	1	1	0	1	0	VL26	$VGMA16 + (VGMA15 - VGMA16) \times 3826 / 4288$
1BH	0	0	0	1	1	0	1	1	VL27	$VGMA16 + (VGMA15 - VGMA16) \times 3906 / 4288$
1CH	0	0	0	1	1	1	0	0	VL28	$VGMA16 + (VGMA15 - VGMA16) \times 3985 / 4288$
1DH	0	0	0	1	1	1	0	1	VL29	$VGMA16 + (VGMA15 - VGMA16) \times 4062 / 4288$
1EH	0	0	0	1	1	1	1	0	VL30	$VGMA16 + (VGMA15 - VGMA16) \times 4138 / 4288$
1FH	0	0	0	1	1	1	1	1	VL31	$VGMA16 + (VGMA15 - VGMA16) \times 4214 / 4288$
20H	0	0	1	0	0	0	0	0	VL32	VGMA15
21H	0	0	1	0	0	0	0	1	VL33	$VGMA15 + (VGMA14 - VGMA15) \times 74 / 2065$
22H	0	0	1	0	0	0	1	0	VL34	$VGMA15 + (VGMA14 - VGMA15) \times 147 / 2065$
23H	0	0	1	0	0	0	1	1	VL35	$VGMA15 + (VGMA14 - VGMA15) \times 219 / 2065$
24H	0	0	1	0	0	1	0	0	VL36	$VGMA15 + (VGMA14 - VGMA15) \times 291 / 2065$
25H	0	0	1	0	0	1	0	1	VL37	$VGMA15 + (VGMA14 - VGMA15) \times 362 / 2065$
26H	0	0	1	0	0	1	1	0	VL38	$VGMA15 + (VGMA14 - VGMA15) \times 433 / 2065$
27H	0	0	1	0	0	1	1	1	VL39	$VGMA15 + (VGMA14 - VGMA15) \times 504 / 2065$

NOTE: VSS2<VGMA16<VGMA15<VGMA14<VGMA13<VGMA12<VGMA11<VGMA10<VGMA9

Table 2. Relationship between Input Data and Output Voltage Value (9)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
28H	0	0	1	0	1	0	0	0	VL40	$VGMA15 + (VGMA14 - VGMA15) \times 574 / 2065$
29H	0	0	1	0	1	0	0	1	VL41	$VGMA15 + (VGMA14 - VGMA15) \times 644 / 2065$
2AH	0	0	1	0	1	0	1	0	VL42	$VGMA15 + (VGMA14 - VGMA15) \times 713 / 2065$
2BH	0	0	1	0	1	0	1	1	VL43	$VGMA15 + (VGMA14 - VGMA15) \times 782 / 2065$
2CH	0	0	1	0	1	1	0	0	VL44	$VGMA15 + (VGMA14 - VGMA15) \times 851 / 2065$
2DH	0	0	1	0	1	1	0	1	VL45	$VGMA15 + (VGMA14 - VGMA15) \times 919 / 2065$
2EH	0	0	1	0	1	1	1	0	VL46	$VGMA15 + (VGMA14 - VGMA15) \times 987 / 2065$
2FH	0	0	1	0	1	1	1	1	VL47	$VGMA15 + (VGMA14 - VGMA15) \times 1054 / 2065$
30H	0	0	1	1	0	0	0	0	VL48	$VGMA15 + (VGMA14 - VGMA15) \times 1120 / 2065$
31H	0	0	1	1	0	0	0	1	VL49	$VGMA15 + (VGMA14 - VGMA15) \times 1186 / 2065$
32H	0	0	1	1	0	0	1	0	VL50	$VGMA15 + (VGMA14 - VGMA15) \times 1251 / 2065$
33H	0	0	1	1	0	0	1	1	VL51	$VGMA15 + (VGMA14 - VGMA15) \times 1316 / 2065$
34H	0	0	1	1	0	1	0	0	VL52	$VGMA15 + (VGMA14 - VGMA15) \times 1380 / 2065$
35H	0	0	1	1	0	1	0	1	VL53	$VGMA15 + (VGMA14 - VGMA15) \times 1442 / 2065$
36H	0	0	1	1	0	1	1	0	VL54	$VGMA15 + (VGMA14 - VGMA15) \times 1504 / 2065$
37H	0	0	1	1	0	1	1	1	VL55	$VGMA15 + (VGMA14 - VGMA15) \times 1565 / 2065$
38H	0	0	1	1	1	0	0	0	VL56	$VGMA15 + (VGMA14 - VGMA15) \times 1625 / 2065$
39H	0	0	1	1	1	0	0	1	VL57	$VGMA15 + (VGMA14 - VGMA15) \times 1684 / 2065$
3AH	0	0	1	1	1	0	1	0	VL58	$VGMA15 + (VGMA14 - VGMA15) \times 1742 / 2065$
3BH	0	0	1	1	1	0	1	1	VL59	$VGMA15 + (VGMA14 - VGMA15) \times 1799 / 2065$
3CH	0	0	1	1	1	1	0	0	VL60	$VGMA15 + (VGMA14 - VGMA15) \times 1854 / 2065$
3DH	0	0	1	1	1	1	0	1	VL61	$VGMA15 + (VGMA14 - VGMA15) \times 1909 / 2065$
3EH	0	0	1	1	1	1	1	0	VL62	$VGMA15 + (VGMA14 - VGMA15) \times 1962 / 2065$
3FH	0	0	1	1	1	1	1	1	VL63	$VGMA15 + (VGMA14 - VGMA15) \times 2014 / 2065$
40H	0	1	0	0	0	0	0	0	VL64	VGMA14
41H	0	1	0	0	0	0	0	1	VL65	$VGMA14 + (VGMA13 - VGMA14) \times 50 / 2368$
42H	0	1	0	0	0	0	1	0	VL66	$VGMA14 + (VGMA13 - VGMA14) \times 99 / 2368$
43H	0	1	0	0	0	0	1	1	VL67	$VGMA14 + (VGMA13 - VGMA14) \times 146 / 2368$
44H	0	1	0	0	0	1	0	0	VL68	$VGMA14 + (VGMA13 - VGMA14) \times 193 / 2368$
45H	0	1	0	0	0	1	0	1	VL69	$VGMA14 + (VGMA13 - VGMA14) \times 238 / 2368$
46H	0	1	0	0	0	1	1	0	VL70	$VGMA14 + (VGMA13 - VGMA14) \times 283 / 2368$
47H	0	1	0	0	0	1	1	1	VL71	$VGMA14 + (VGMA13 - VGMA14) \times 326 / 2368$
48H	0	1	0	0	1	0	0	0	VL72	$VGMA14 + (VGMA13 - VGMA14) \times 369 / 2368$
49H	0	1	0	0	1	0	0	1	VL73	$VGMA14 + (VGMA13 - VGMA14) \times 411 / 2368$
4AH	0	1	0	0	1	0	1	0	VL74	$VGMA14 + (VGMA13 - VGMA14) \times 452 / 2368$
4BH	0	1	0	0	1	0	1	1	VL75	$VGMA14 + (VGMA13 - VGMA14) \times 492 / 2368$
4CH	0	1	0	0	1	1	0	0	VL76	$VGMA14 + (VGMA13 - VGMA14) \times 532 / 2368$
4DH	0	1	0	0	1	1	0	1	VL77	$VGMA14 + (VGMA13 - VGMA14) \times 571 / 2368$
4EH	0	1	0	0	1	1	1	0	VL78	$VGMA14 + (VGMA13 - VGMA14) \times 609 / 2368$
4FH	0	1	0	0	1	1	1	1	VL79	$VGMA14 + (VGMA13 - VGMA14) \times 647 / 2368$

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Table 2. Relationship between Input Data and Output Voltage Value (10)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
50H	0	1	0	1	0	0	0	0	VL80	VGMA14 + (VGMA13 - VGMA14) × 684 / 2368
51H	0	1	0	1	0	0	0	1	VL81	VGMA14 + (VGMA13 - VGMA14) × 722 / 2368
52H	0	1	0	1	0	0	1	0	VL82	VGMA14 + (VGMA13 - VGMA14) × 758 / 2368
53H	0	1	0	1	0	0	1	1	VL83	VGMA14 + (VGMA13 - VGMA14) × 795 / 2368
54H	0	1	0	1	0	1	0	0	VL84	VGMA14 + (VGMA13 - VGMA14) × 831 / 2368
55H	0	1	0	1	0	1	0	1	VL85	VGMA14 + (VGMA13 - VGMA14) × 867 / 2368
56H	0	1	0	1	0	1	1	0	VL86	VGMA14 + (VGMA13 - VGMA14) × 903 / 2368
57H	0	1	0	1	0	1	1	1	VL87	VGMA14 + (VGMA13 - VGMA14) × 938 / 2368
58H	0	1	0	1	1	0	0	0	VL88	VGMA14 + (VGMA13 - VGMA14) × 974 / 2368
59H	0	1	0	1	1	0	0	1	VL89	VGMA14 + (VGMA13 - VGMA14) × 1009 / 2368
5AH	0	1	0	1	1	0	1	0	VL90	VGMA14 + (VGMA13 - VGMA14) × 1045 / 2368
5BH	0	1	0	1	1	0	1	1	VL91	VGMA14 + (VGMA13 - VGMA14) × 1080 / 2368
5CH	0	1	0	1	1	1	0	0	VL92	VGMA14 + (VGMA13 - VGMA14) × 1116 / 2368
5DH	0	1	0	1	1	1	0	1	VL93	VGMA14 + (VGMA13 - VGMA14) × 1151 / 2368
5EH	0	1	0	1	1	1	1	0	VL94	VGMA14 + (VGMA13 - VGMA14) × 1187 / 2368
5FH	0	1	0	1	1	1	1	1	VL95	VGMA14 + (VGMA13 - VGMA14) × 1222 / 2368
60H	0	1	1	0	0	0	0	0	VL96	VGMA14 + (VGMA13 - VGMA14) × 1258 / 2368
61H	0	1	1	0	0	0	0	1	VL97	VGMA14 + (VGMA13 - VGMA14) × 1294 / 2368
62H	0	1	1	0	0	0	1	0	VL98	VGMA14 + (VGMA13 - VGMA14) × 1329 / 2368
63H	0	1	1	0	0	0	1	1	VL99	VGMA14 + (VGMA13 - VGMA14) × 1365 / 2368
64H	0	1	1	0	0	1	0	0	VL100	VGMA14 + (VGMA13 - VGMA14) × 1401 / 2368
65H	0	1	1	0	0	1	0	1	VL101	VGMA14 + (VGMA13 - VGMA14) × 1436 / 2368
66H	0	1	1	0	0	1	1	0	VL102	VGMA14 + (VGMA13 - VGMA14) × 1472 / 2368
67H	0	1	1	0	0	1	1	1	VL103	VGMA14 + (VGMA13 - VGMA14) × 1507 / 2368
68H	0	1	1	0	1	0	0	0	VL104	VGMA14 + (VGMA13 - VGMA14) × 1543 / 2368
69H	0	1	1	0	1	0	0	1	VL105	VGMA14 + (VGMA13 - VGMA14) × 1579 / 2368
6AH	0	1	1	0	1	0	1	0	VL106	VGMA14 + (VGMA13 - VGMA14) × 1614 / 2368
6BH	0	1	1	0	1	0	1	1	VL107	VGMA14 + (VGMA13 - VGMA14) × 1649 / 2368
6CH	0	1	1	0	1	1	0	0	VL108	VGMA14 + (VGMA13 - VGMA14) × 1685 / 2368
6DH	0	1	1	0	1	1	0	1	VL109	VGMA14 + (VGMA13 - VGMA14) × 1720 / 2368
6EH	0	1	1	0	1	1	1	0	VL110	VGMA14 + (VGMA13 - VGMA14) × 1755 / 2368
6FH	0	1	1	0	1	1	1	1	VL111	VGMA14 + (VGMA13 - VGMA14) × 1790 / 2368
70H	0	1	1	1	0	0	0	0	VL112	VGMA14 + (VGMA13 - VGMA14) × 1825 / 2368
71H	0	1	1	1	0	0	0	1	VL113	VGMA14 + (VGMA13 - VGMA14) × 1860 / 2368
72H	0	1	1	1	0	0	1	0	VL114	VGMA14 + (VGMA13 - VGMA14) × 1895 / 2368
73H	0	1	1	1	0	0	1	1	VL115	VGMA14 + (VGMA13 - VGMA14) × 1929 / 2368
74H	0	1	1	1	0	1	0	0	VL116	VGMA14 + (VGMA13 - VGMA14) × 1964 / 2368
75H	0	1	1	1	0	1	0	1	VL117	VGMA14 + (VGMA13 - VGMA14) × 1998 / 2368
76H	0	1	1	1	0	1	1	0	VL118	VGMA14 + (VGMA13 - VGMA14) × 2032 / 2368
77H	0	1	1	1	0	1	1	1	VL119	VGMA14 + (VGMA13 - VGMA14) × 2066 / 2368

Table 2. Relationship between Input Data and Output Voltage Value (11)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
78H	0	1	1	1	1	0	0	0	VL120	$\text{VGMA14} + (\text{VGMA13} - \text{VGMA14}) \times 2100 / 2368$
79H	0	1	1	1	1	0	0	1	VL121	$\text{VGMA14} + (\text{VGMA13} - \text{VGMA14}) \times 2134 / 2368$
7AH	0	1	1	1	1	0	1	0	VL122	$\text{VGMA14} + (\text{VGMA13} - \text{VGMA14}) \times 2168 / 2368$
7BH	0	1	1	1	1	0	1	1	VL123	$\text{VGMA14} + (\text{VGMA13} - \text{VGMA14}) \times 2201 / 2368$
7CH	0	1	1	1	1	1	0	0	VL124	$\text{VGMA14} + (\text{VGMA13} - \text{VGMA14}) \times 2235 / 2368$
7DH	0	1	1	1	1	1	0	1	VL125	$\text{VGMA14} + (\text{VGMA13} - \text{VGMA14}) \times 2268 / 2368$
7EH	0	1	1	1	1	1	1	0	VL126	$\text{VGMA14} + (\text{VGMA13} - \text{VGMA14}) \times 2302 / 2368$
7FH	0	1	1	1	1	1	1	1	VL127	$\text{VGMA14} + (\text{VGMA13} - \text{VGMA14}) \times 2335 / 2368$
80H	1	0	0	0	0	0	0	0	VL128	VGMA13
81H	1	0	0	0	0	0	0	1	VL129	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 33 / 2149$
82H	1	0	0	0	0	0	1	0	VL130	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 66 / 2149$
83H	1	0	0	0	0	0	1	1	VL131	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 100 / 2149$
84H	1	0	0	0	0	1	0	0	VL132	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 133 / 2149$
85H	1	0	0	0	0	1	0	1	VL133	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 166 / 2149$
86H	1	0	0	0	0	1	1	0	VL134	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 199 / 2149$
87H	1	0	0	0	0	1	1	1	VL135	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 232 / 2149$
88H	1	0	0	0	1	0	0	0	VL136	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 266 / 2149$
89H	1	0	0	0	1	0	0	1	VL137	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 299 / 2149$
8AH	1	0	0	0	1	0	1	0	VL138	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 332 / 2149$
8BH	1	0	0	0	1	0	1	1	VL139	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 365 / 2149$
8CH	1	0	0	0	1	1	0	0	VL140	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 399 / 2149$
8DH	1	0	0	0	1	1	0	1	VL141	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 432 / 2149$
8EH	1	0	0	0	1	1	1	0	VL142	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 465 / 2149$
8FH	1	0	0	0	1	1	1	1	VL143	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 498 / 2149$
90H	1	0	0	1	0	0	0	0	VL144	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 532 / 2149$
91H	1	0	0	1	0	0	0	1	VL145	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 565 / 2149$
92H	1	0	0	1	0	0	1	0	VL146	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 598 / 2149$
93H	1	0	0	1	0	0	1	1	VL147	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 632 / 2149$
94H	1	0	0	1	0	1	0	0	VL148	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 665 / 2149$
95H	1	0	0	1	0	1	0	1	VL149	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 698 / 2149$
96H	1	0	0	1	0	1	1	0	VL150	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 732 / 2149$
97H	1	0	0	1	0	1	1	1	VL151	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 765 / 2149$
98H	1	0	0	1	1	0	0	0	VL152	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 798 / 2149$
99H	1	0	0	1	1	0	0	1	VL153	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 831 / 2149$
9AH	1	0	0	1	1	0	1	0	VL154	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 864 / 2149$
9BH	1	0	0	1	1	0	1	1	VL155	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 897 / 2149$
9CH	1	0	0	1	1	1	0	0	VL156	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 930 / 2149$
9DH	1	0	0	1	1	1	0	1	VL157	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 963 / 2149$
9EH	1	0	0	1	1	1	1	0	VL158	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 996 / 2149$
9FH	1	0	0	1	1	1	1	1	VL159	$\text{VGMA13} + (\text{VGMA12} - \text{VGMA13}) \times 1029 / 2149$

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Table 2. Relationship between Input Data and Output Voltage Value (12)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
A0H	1	0	1	0	0	0	0	0	VL160	$VGMA13 + (VGMA12 - VGMA13) \times 1062 / 2149$
A1H	1	0	1	0	0	0	0	1	VL161	$VGMA13 + (VGMA12 - VGMA13) \times 1094 / 2149$
A2H	1	0	1	0	0	0	1	0	VL162	$VGMA13 + (VGMA12 - VGMA13) \times 1127 / 2149$
A3H	1	0	1	0	0	0	1	1	VL163	$VGMA13 + (VGMA12 - VGMA13) \times 1159 / 2149$
A4H	1	0	1	0	0	1	0	0	VL164	$VGMA13 + (VGMA12 - VGMA13) \times 1192 / 2149$
A5H	1	0	1	0	0	1	0	1	VL165	$VGMA13 + (VGMA12 - VGMA13) \times 1224 / 2149$
A6H	1	0	1	0	0	1	1	0	VL166	$VGMA13 + (VGMA12 - VGMA13) \times 1257 / 2149$
A7H	1	0	1	0	0	1	1	1	VL167	$VGMA13 + (VGMA12 - VGMA13) \times 1289 / 2149$
A8H	1	0	1	0	1	0	0	0	VL168	$VGMA13 + (VGMA12 - VGMA13) \times 1322 / 2149$
A9H	1	0	1	0	1	0	0	1	VL169	$VGMA13 + (VGMA12 - VGMA13) \times 1354 / 2149$
AAH	1	0	1	0	1	0	1	0	VL170	$VGMA13 + (VGMA12 - VGMA13) \times 1387 / 2149$
ABH	1	0	1	0	1	0	1	1	VL171	$VGMA13 + (VGMA12 - VGMA13) \times 1419 / 2149$
ACH	1	0	1	0	1	1	0	0	VL172	$VGMA13 + (VGMA12 - VGMA13) \times 1452 / 2149$
ADH	1	0	1	0	1	1	0	1	VL173	$VGMA13 + (VGMA12 - VGMA13) \times 1485 / 2149$
AEH	1	0	1	0	1	1	1	0	VL174	$VGMA13 + (VGMA12 - VGMA13) \times 1517 / 2149$
AFH	1	0	1	0	1	1	1	1	VL175	$VGMA13 + (VGMA12 - VGMA13) \times 1550 / 2149$
B0H	1	0	1	1	0	0	0	0	VL176	$VGMA13 + (VGMA12 - VGMA13) \times 1583 / 2149$
B1H	1	0	1	1	0	0	0	1	VL177	$VGMA13 + (VGMA12 - VGMA13) \times 1617 / 2149$
B2H	1	0	1	1	0	0	1	0	VL178	$VGMA13 + (VGMA12 - VGMA13) \times 1650 / 2149$
B3H	1	0	1	1	0	0	1	1	VL179	$VGMA13 + (VGMA12 - VGMA13) \times 1684 / 2149$
B4H	1	0	1	1	0	1	0	0	VL180	$VGMA13 + (VGMA12 - VGMA13) \times 1717 / 2149$
B5H	1	0	1	1	0	1	0	1	VL181	$VGMA13 + (VGMA12 - VGMA13) \times 1752 / 2149$
B6H	1	0	1	1	0	1	1	0	VL182	$VGMA13 + (VGMA12 - VGMA13) \times 1786 / 2149$
B7H	1	0	1	1	0	1	1	1	VL183	$VGMA13 + (VGMA12 - VGMA13) \times 1821 / 2149$
B8H	1	0	1	1	1	0	0	0	VL184	$VGMA13 + (VGMA12 - VGMA13) \times 1856 / 2149$
B9H	1	0	1	1	1	0	0	1	VL185	$VGMA13 + (VGMA12 - VGMA13) \times 1891 / 2149$
BAH	1	0	1	1	1	0	1	0	VL186	$VGMA13 + (VGMA12 - VGMA13) \times 1927 / 2149$
BBH	1	0	1	1	1	0	1	1	VL187	$VGMA13 + (VGMA12 - VGMA13) \times 1963 / 2149$
BCH	1	0	1	1	1	1	0	0	VL188	$VGMA13 + (VGMA12 - VGMA13) \times 1999 / 2149$
BDH	1	0	1	1	1	1	0	1	VL189	$VGMA13 + (VGMA12 - VGMA13) \times 2036 / 2149$
BEH	1	0	1	1	1	1	1	0	VL190	$VGMA13 + (VGMA12 - VGMA13) \times 2073 / 2149$
BFH	1	0	1	1	1	1	1	1	VL191	$VGMA13 + (VGMA12 - VGMA13) \times 2111 / 2149$
C0H	1	1	0	0	0	0	0	0	VL192	$VGMA12$
C1H	1	1	0	0	0	0	0	1	VL193	$VGMA12 + (VGMA11 - VGMA12) \times 38 / 3080$
C2H	1	1	0	0	0	0	1	0	VL194	$VGMA12 + (VGMA11 - VGMA12) \times 77 / 3080$
C3H	1	1	0	0	0	0	1	1	VL195	$VGMA12 + (VGMA11 - VGMA12) \times 116 / 3080$
C4H	1	1	0	0	0	1	0	0	VL196	$VGMA12 + (VGMA11 - VGMA12) \times 155 / 3080$
C5H	1	1	0	0	0	1	0	1	VL197	$VGMA12 + (VGMA11 - VGMA12) \times 195 / 3080$
C6H	1	1	0	0	0	1	1	0	VL198	$VGMA12 + (VGMA11 - VGMA12) \times 235 / 3080$
C7H	1	1	0	0	0	1	1	1	VL199	$VGMA12 + (VGMA11 - VGMA12) \times 276 / 3080$

Table 2. Relationship between Input Data and Output Voltage Value (13)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
C8H	1	1	0	0	1	0	0	0	VL200	$VGMA12 + (VGMA11 - VGMA12) \times 316 / 3080$
C9H	1	1	0	0	1	0	0	1	VL201	$VGMA12 + (VGMA11 - VGMA12) \times 357 / 3080$
CAH	1	1	0	0	1	0	1	0	VL202	$VGMA12 + (VGMA11 - VGMA12) \times 399 / 3080$
CBH	1	1	0	0	1	0	1	1	VL203	$VGMA12 + (VGMA11 - VGMA12) \times 440 / 3080$
CCH	1	1	0	0	1	1	0	0	VL204	$VGMA12 + (VGMA11 - VGMA12) \times 482 / 3080$
CDH	1	1	0	0	1	1	0	1	VL205	$VGMA12 + (VGMA11 - VGMA12) \times 524 / 3080$
CEH	1	1	0	0	1	1	1	0	VL206	$VGMA12 + (VGMA11 - VGMA12) \times 566 / 3080$
CFH	1	1	0	0	1	1	1	1	VL207	$VGMA12 + (VGMA11 - VGMA12) \times 609 / 3080$
D0H	1	1	0	1	0	0	0	0	VL208	$VGMA12 + (VGMA11 - VGMA12) \times 651 / 3080$
D1H	1	1	0	1	0	0	0	1	VL209	$VGMA12 + (VGMA11 - VGMA12) \times 694 / 3080$
D2H	1	1	0	1	0	0	1	0	VL210	$VGMA12 + (VGMA11 - VGMA12) \times 738 / 3080$
D3H	1	1	0	1	0	0	1	1	VL211	$VGMA12 + (VGMA11 - VGMA12) \times 782 / 3080$
D4H	1	1	0	1	0	1	0	0	VL212	$VGMA12 + (VGMA11 - VGMA12) \times 826 / 3080$
D5H	1	1	0	1	0	1	0	1	VL213	$VGMA12 + (VGMA11 - VGMA12) \times 871 / 3080$
D6H	1	1	0	1	0	1	1	0	VL214	$VGMA12 + (VGMA11 - VGMA12) \times 916 / 3080$
D7H	1	1	0	1	0	1	1	1	VL215	$VGMA12 + (VGMA11 - VGMA12) \times 962 / 3080$
D8H	1	1	0	1	1	0	0	0	VL216	$VGMA12 + (VGMA11 - VGMA12) \times 1009 / 3080$
D9H	1	1	0	1	1	0	0	1	VL217	$VGMA12 + (VGMA11 - VGMA12) \times 1057 / 3080$
DAH	1	1	0	1	1	0	1	0	VL218	$VGMA12 + (VGMA11 - VGMA12) \times 1106 / 3080$
DBH	1	1	0	1	1	0	1	1	VL219	$VGMA12 + (VGMA11 - VGMA12) \times 1157 / 3080$
DCH	1	1	0	1	1	1	0	0	VL220	$VGMA12 + (VGMA11 - VGMA12) \times 1209 / 3080$
DDH	1	1	0	1	1	1	0	1	VL221	$VGMA12 + (VGMA11 - VGMA12) \times 1263 / 3080$
DEH	1	1	0	1	1	1	1	0	VL222	$VGMA12 + (VGMA11 - VGMA12) \times 1320 / 3080$
DFH	1	1	0	1	1	1	1	1	VL223	$VGMA12 + (VGMA11 - VGMA12) \times 1379 / 3080$
E0H	1	1	1	0	0	0	0	0	VL224	$VGMA12 + (VGMA11 - VGMA12) \times 1441 / 3080$
E1H	1	1	1	0	0	0	0	1	VL225	$VGMA12 + (VGMA11 - VGMA12) \times 1506 / 3080$
E2H	1	1	1	0	0	0	1	0	VL226	$VGMA12 + (VGMA11 - VGMA12) \times 1574 / 3080$
E3H	1	1	1	0	0	0	1	1	VL227	$VGMA12 + (VGMA11 - VGMA12) \times 1647 / 3080$
E4H	1	1	1	0	0	1	0	0	VL228	$VGMA12 + (VGMA11 - VGMA12) \times 1724 / 3080$
E5H	1	1	1	0	0	1	0	1	VL229	$VGMA12 + (VGMA11 - VGMA12) \times 1805 / 3080$
E6H	1	1	1	0	0	1	1	0	VL230	$VGMA12 + (VGMA11 - VGMA12) \times 1892 / 3080$
E7H	1	1	1	0	0	1	1	1	VL231	$VGMA12 + (VGMA11 - VGMA12) \times 1983 / 3080$
E8H	1	1	1	0	1	0	0	0	VL232	$VGMA12 + (VGMA11 - VGMA12) \times 2081 / 3080$
E9H	1	1	1	0	1	0	0	1	VL233	$VGMA12 + (VGMA11 - VGMA12) \times 2184 / 3080$
EAH	1	1	1	0	1	0	1	0	VL234	$VGMA12 + (VGMA11 - VGMA12) \times 2293 / 3080$
EBH	1	1	1	0	1	0	1	1	VL235	$VGMA12 + (VGMA11 - VGMA12) \times 2409 / 3080$
ECH	1	1	1	0	1	1	0	0	VL236	$VGMA12 + (VGMA11 - VGMA12) \times 2530 / 3080$
EDH	1	1	1	0	1	1	0	1	VL237	$VGMA12 + (VGMA11 - VGMA12) \times 2658 / 3080$
EEH	1	1	1	0	1	1	1	0	VL238	$VGMA12 + (VGMA11 - VGMA12) \times 2792 / 3080$
EFH	1	1	1	0	1	1	1	1	VL239	$VGMA12 + (VGMA11 - VGMA12) \times 2933 / 3080$

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Table 2. Relationship between Input Data and Output Voltage Value (14)

Input data	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
F0H	1	1	1	1	0	0	0	0	VL240	VGMA11
F1H	1	1	1	1	0	0	0	1	VL241	VGMA11 + (VGMA10 - VGMA11) $\times$ 154 / 4641
F2H	1	1	1	1	0	0	1	0	VL242	VGMA11 + (VGMA10 - VGMA11) $\times$ 314 / 4641
F3H	1	1	1	1	0	0	1	1	VL243	VGMA11 + (VGMA10 - VGMA11) $\times$ 482 / 4641
F4H	1	1	1	1	0	1	0	0	VL244	VGMA11 + (VGMA10 - VGMA11) $\times$ 659 / 4641
F5H	1	1	1	1	0	1	0	1	VL245	VGMA11 + (VGMA10 - VGMA11) $\times$ 846 / 4641
F6H	1	1	1	1	0	1	1	0	VL246	VGMA11 + (VGMA10 - VGMA11) $\times$ 1045 / 4641
F7H	1	1	1	1	0	1	1	1	VL247	VGMA11 + (VGMA10 - VGMA11) $\times$ 1260 / 4641
F8H	1	1	1	1	1	0	0	0	VL248	VGMA11 + (VGMA10 - VGMA11) $\times$ 1498 / 4641
F9H	1	1	1	1	1	0	0	1	VL249	VGMA11 + (VGMA10 - VGMA11) $\times$ 1768 / 4641
FAH	1	1	1	1	1	0	1	0	VL250	VGMA11 + (VGMA10 - VGMA11) $\times$ 2086 / 4641
FBH	1	1	1	1	1	0	1	1	VL251	VGMA11 + (VGMA10 - VGMA11) $\times$ 2482 / 4641
FCH	1	1	1	1	1	1	0	0	VL252	VGMA11 + (VGMA10 - VGMA11) $\times$ 3014 / 4641
FDH	1	1	1	1	1	1	0	1	VL253	VGMA11 + (VGMA10 - VGMA11) $\times$ 3825 / 4641
FEH	1	1	1	1	1	1	1	0	VL254	VGMA10
FFH	1	1	1	1	1	1	1	1	VL255	VGMA9

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings (VSS1 = VSS2 = 0 V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	VDD1	-0.3 to 5.0	V
Driver supply voltage	VDD2	-0.3 to 16	V
Input voltage	VGMA1 - 16	-0.3 to VDD2+0.3	V
	Others	-0.3 to VDD1+0.3	
Output voltage	DIO1, 2	-0.3 to VDD1+0.3	V
	Y1 – Y402	-0.3 to VDD2+0.3	
Operating power dissipation	Pd	300 [1]	mW
Operation temperature	Top	-20 to 75	°C
Storage temperature	Tstg	-55 to 125	°C

CAUTIONS:

If LSIs are stressed beyond those listed above "absolute maximum ratings", they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Turn on power order: VDD1 → control signal input → VDD2 → VGMA1 - VGMA16 Turn off power order: VGMA1 - VGMA16 → VDD2 → control signal input → VDD1

RECOMMENDED OPERATION CONDITIONS

Table 4. Recommended Operation Conditions (Ta = -20 to 75 °C, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD1	2.5	3.3	3.6	V
Driver supply voltage	VDD2 [1]	8.0	12.0	15.0	V
Gamma corrected voltage	VGMA1 – VGMA8	0.5 VDD2	-	VDD2 - 0.1	V
	VGMA9 – VGMA16	VSS2 + 0.1	-	0.5 VDD2	V
Driver part output voltage	Vyo	VSS2 + 0.1	-	VDD2 - 0.1	V
Maximum clock frequency (Single edge/Double edge)	fmax	VDD1 = 2.5 V		55 / 40	MHz
		VDD1 = 3.0 V		75 / 55	
Output load capacitance	CL[1]	-	-	200	pF / PIN

NOTE: 1. Relationship between TFT-LCD panel and Pd ($Pd \propto CL * (VDD2)^2 * fCLK1$)

TFT-LCD panel standard	CL = 140pF	CL = 200pF
SXGA	max. VDD2 = 15 V	max. VDD2 = 13 V
UXGA & WUXGA	max. VDD2 = 14 V	max. VDD2 = 12 V

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DC CHARACTERISTICS

Table 5. DC Characteristics (Ta = -20 to 75 °C, VDD1 = 2.5 to 3.6 V, VDD2 = 8 to 15 V, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SHL, CLK2, D00 - D57, CLK1, SELT, DATPOL1, DATPOL2, DEC, POL, DIO1 (DIO2)	0.8 VDD1	-	VDD1	V
Low level input voltage	VIL		0	-	0.2 VDD1	
Input leakage current	IL		-1	-	1	μA
High level output voltage	VOH	DIO1 (DIO2), IO = -1.0 mA	VDD1 - 0.5	-	-	V
Low level output voltage	VOL	DIO1 (DIO2), IO = +1.0 mA	-	-	0.5	
Resistor	R0 - R254	Refer to Table 1. Resistor Strings	$Rn \times 0.7$		$Rn \times 1.3$	Ω
Driver output current	IVOH	VDD2 = 10.0 V, Vx = 3.5 V, Vyo = 9.5 V[1]	-	-2.0	-1.0	mA
	IVOL	VDD2 = 10.0 V, Vx = 6.5 V, Vyo = 0.5 V[1]	1.0	2.0	-	mA
Output voltage deviation	ΔVO	VSS2 + 0.1 V to VDD2 - 1.5 V	-	±7	±15	mV
		VDD2 - 1.5 V to VDD2 - 0.1 V	-	±10	±20	
Output RMS voltage deviation	dVrms[2]	Input data: 00H to FFH	-	±3	±10	
Output voltage range	Vyo	Input data: 00H to FFH	VSS2 + 0.1	-	VDD2 – 0.1	V
Logic part dynamic current	IDD1	VDD1 = 3.0 V [3]	-	4.0	7.0	mA
Driver part dynamic current	IDD2	VDD2 = 10 V [4]	-	10.0	15.0	

NOTES:

1. Vyo is the output voltage of analog output pins Y1 to Y402.
   Vx is the voltage applied to analog output pins Y1 to Y402.
2. dVrms is a maximum deviation value from ideal difference between high output and low output at the same gray scale.
3. CLK1 period is defined to be 15.6 μs at fCLK2 = 54 MHz, DEC = L, data pattern = 10101010
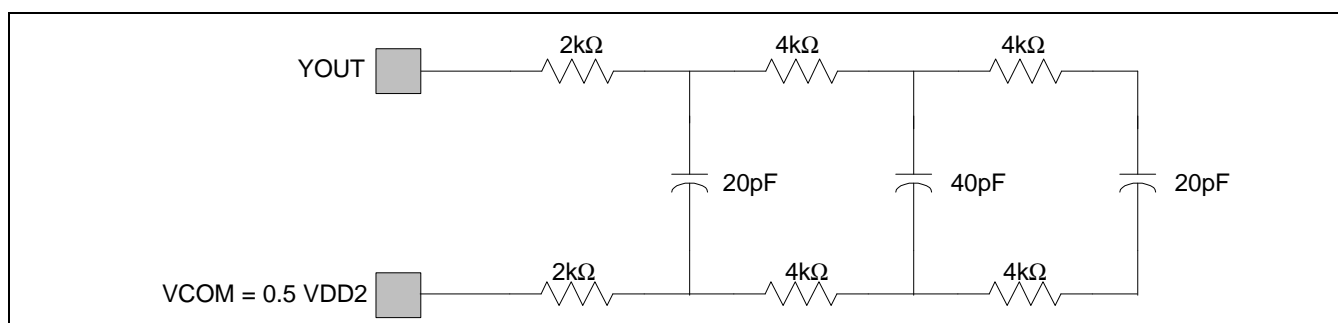   (checkerboard pattern), Ta = 25 °C.
4, Yout Load Condition

Figure 5. Yout Load Condition

SINGLE EDGE AC CHARACTERISTICS

Table 6. AC Characteristics (Ta = -20 to 75 °C, VDD2 = 8 to 15 V, VSS1 = VSS2 = 0 V, DEC = L)

Parameter	Symbol	Condition	VDD1 = 2.5 to 3.0 V		VDD1 = 3.0 to 3.6 V		Unit
			Min.	Max.	Min.	Max.	
Clock pulse width	PWCLK	-	18	-	13	-	ns
Clock pulse low period	PWCLK(L)	-	3	-	2	-	
Clock pulse high period	PWCLK(H)	-	3	-	2	-	
Data setup time	tSETUP1	-	3	-	2	-	
Data hold time	tHOLD1	-	0	-	0	-	
Start pulse setup time	tSETUP2	-	3	-	2	-	
Start pulse hold time	tHOLD2	-	0	-	0	-	
DATPOL-CLK2 setup time	tSETUP4	-	3	-	2	-	
DATPOL-CLK2 hold time	tHOLD4	-	0	-	0	-	
Start pulse delay time	tPLH1	CL = 20 pF	-	15	-	11	
CLK1 setup time	tSETUP3	-	2	-	2	-	CLK2 period
Driver output delay time1	tPHL1	PWCLK1 = 1 µs, Refer Figure 5. Yout Load Condition	-	4	-	4	µs
Driver output delay time2	tPHL2		-	8	-	8	
CLK1 pulse high period	PWCLK1	-	(3CLK2)	2	(3CLK2)	2	
Data invalid period	tINV	-	1	-	1	-	CLK2 period
Last data timing	tLDT	-	1	-	1	-	
CLK1-CLK2 time	tCLK1-CLK2	CLK1↑ or ↓ → CLK2↑	8	-	6	-	ns
POL-CLK1 time	tPOL-CLK1	POL↑ or ↓ → CLK1↑	8	-	6	-	ns

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DOUBLE EDGE AC CHARACTERISTICS

Table 7. AC Characteristics (Ta = -20 to 75 °C, VDD2 = 8 to 15 V, VSS1 = VSS2 = 0 V, DEC = H)

Parameter	Symbol	Condition	VDD1 = 2.5 to 3.0 V		VDD1 = 3.0 to 3.6 V		Unit
			Min.	Max.	Min.	Max.	
Clock pulse width	PWCLK	-	25	-	18	-	ns
Clock pulse low period	PWCLK(L)	-	4	-	3	-	
Clock pulse high period	PWCLK(H)	-	4	-	3	-	
Data setup time	tSETUP1	-	4	-	3	-	
Data hold time	tHOLD1	-	0	-	0	-	
Start pulse setup time	tSETUP2	-	4	-	3	-	
Start pulse hold time	tHOLD2	-	0	-	0	-	
DATPOL-CLK2 setup time	tSETUP4	-	4	-	3	-	
DATPOL-CLK2 hold time	tHOLD4	-	0	-	0	-	
Start pulse delay time	tPLH1	CL = 20 pF	-	15	-	15	
CLK1 setup time	tSETUP3	-	1	-	1	-	CLK2 period
Driver output delay time1	tPHL1	PWCLK1 = 1 µs , Figure 5. Yout Load Condition	-	4	-	4	µs
Driver output delay time2	tPHL2		-	8	-	8	
CLK1 pulse high period	PWCLK1	-	(3CLK2)	2	(3CLK2)	2	
Data invalid period	tINV	-	0.5	-	0.5	-	CLK2 period
Last data timing	tLDT		1	-	1	-	
CLK1-CLK2 time	tCLK1-CLK2	CLK1↑ or ↓ → CLK2↑	8	-	6	-	ns
POL-CLK1 time	tPOL-CLK1	POL↑ or ↓ → CLK1↑	8	-	6	-	ns

SINGLE EDGE WAVEFORMS (VIH = 0.8 VDD1, VIL = 0.2 VDD1)
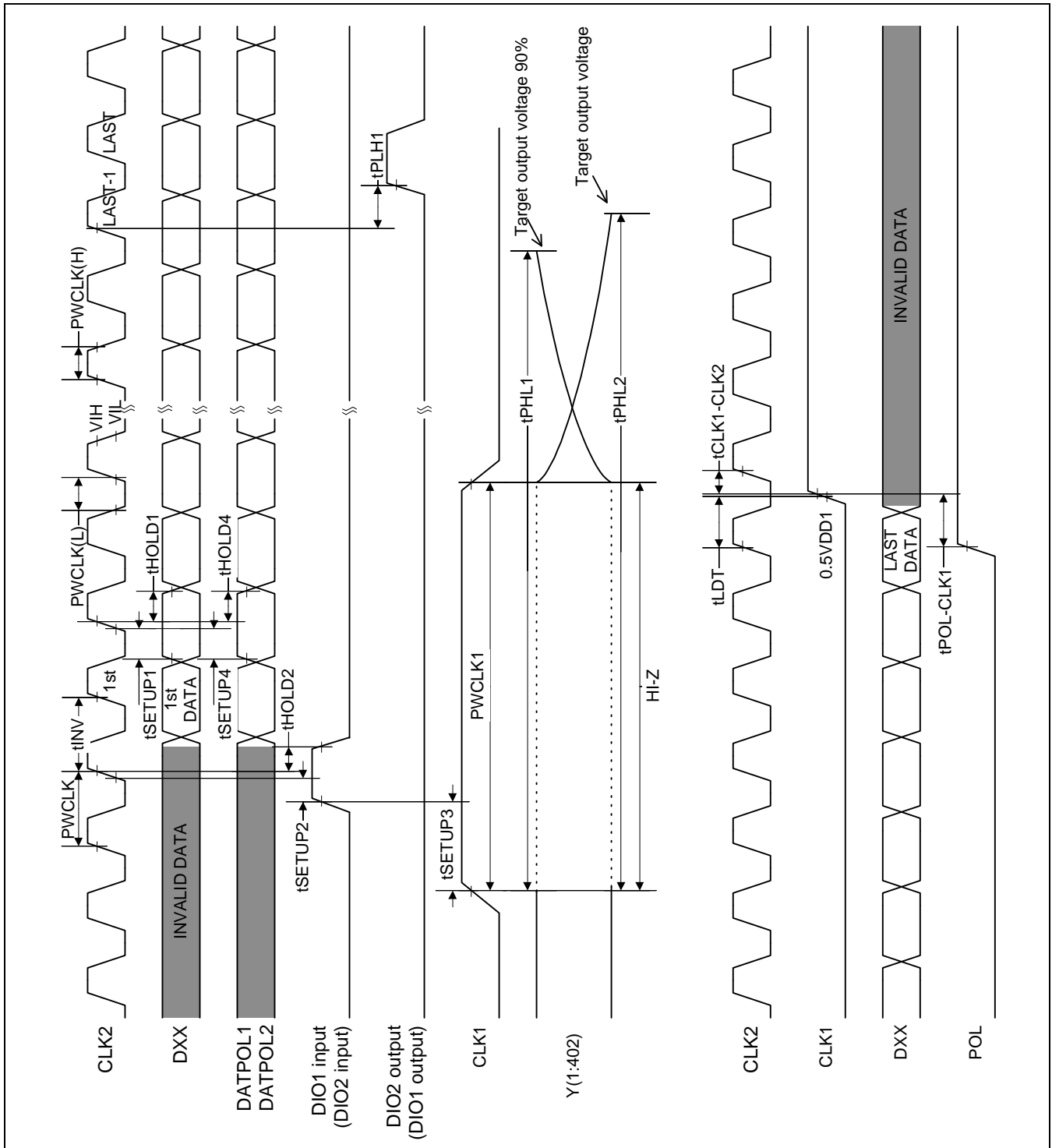
Figure 6. Waveforms, DEC = L

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DOUBLE EDGE WAVEFORMS (VIH = 0.8 VDD1, VIL = 0.2 VDD1)
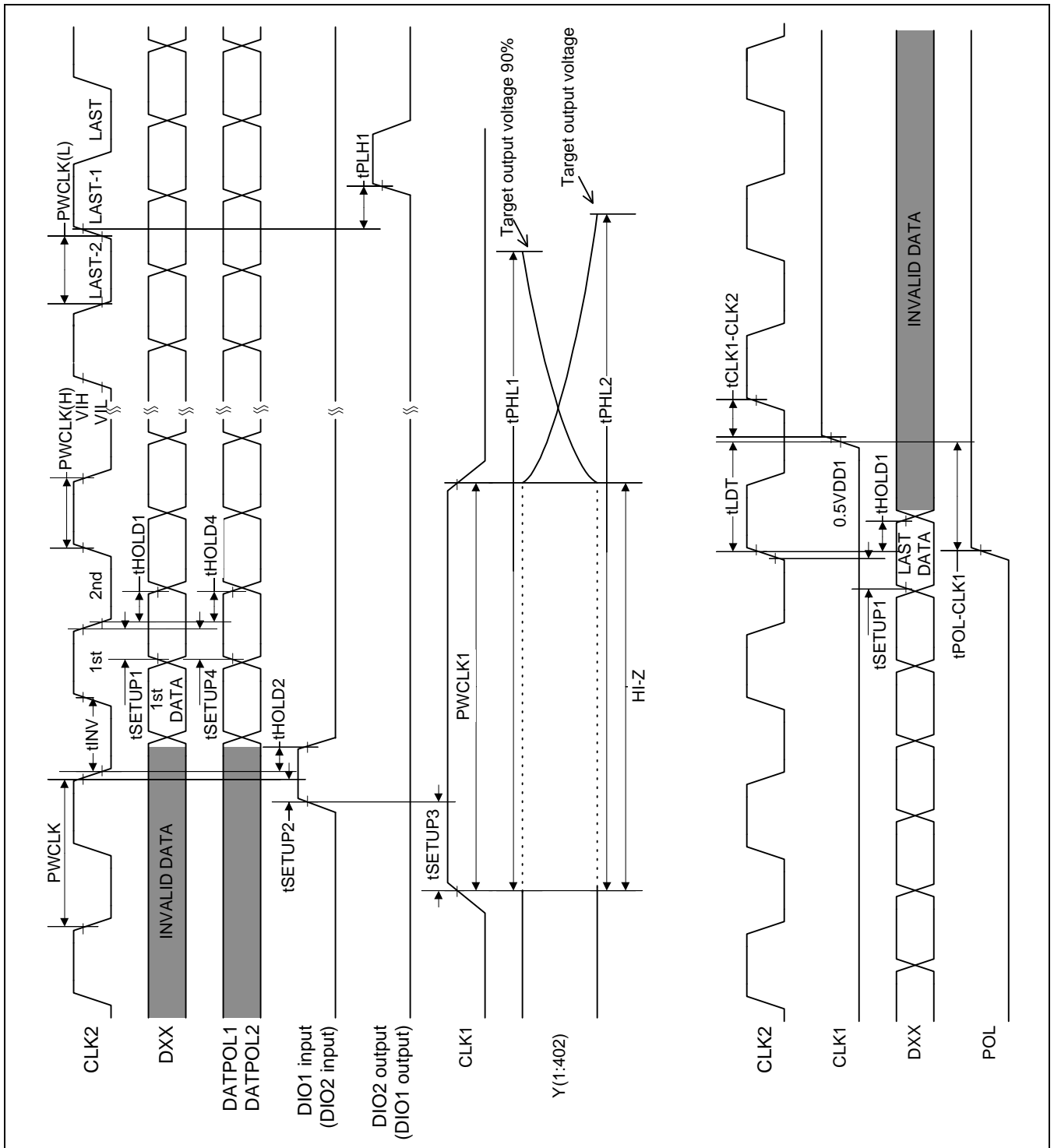

Figure 7. Waveforms, DEC = H

RELATIONSHIPS BETWEEN CLK1, START PULSE (DIO1, DIO2) AND BLANKING PERIOD

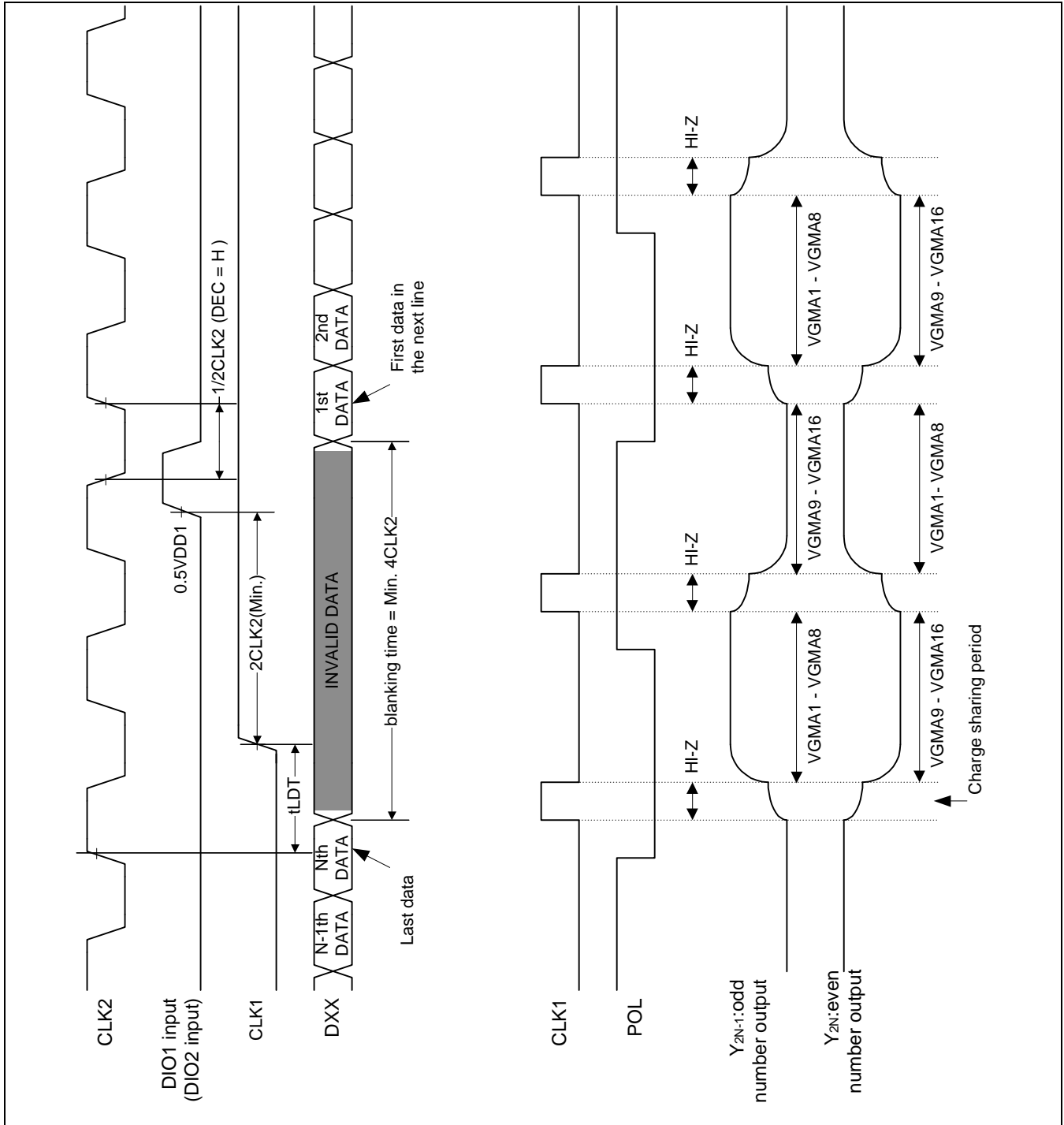**Figure 8. Waveforms**