

## MSM54V24632A

131,072-Word × 32-Bit × 2-Bank SGRAM without Graphics Functions

### DESCRIPTION

The MSM54V24632A is a synchronous graphics random access memory without graphics oriented functions; Block Write, Write per bit, Single write and Burst stop. It is organized as 128K words × 32 bits × 2 banks.

This device can operate up to 125MHz by using synchronous interface.

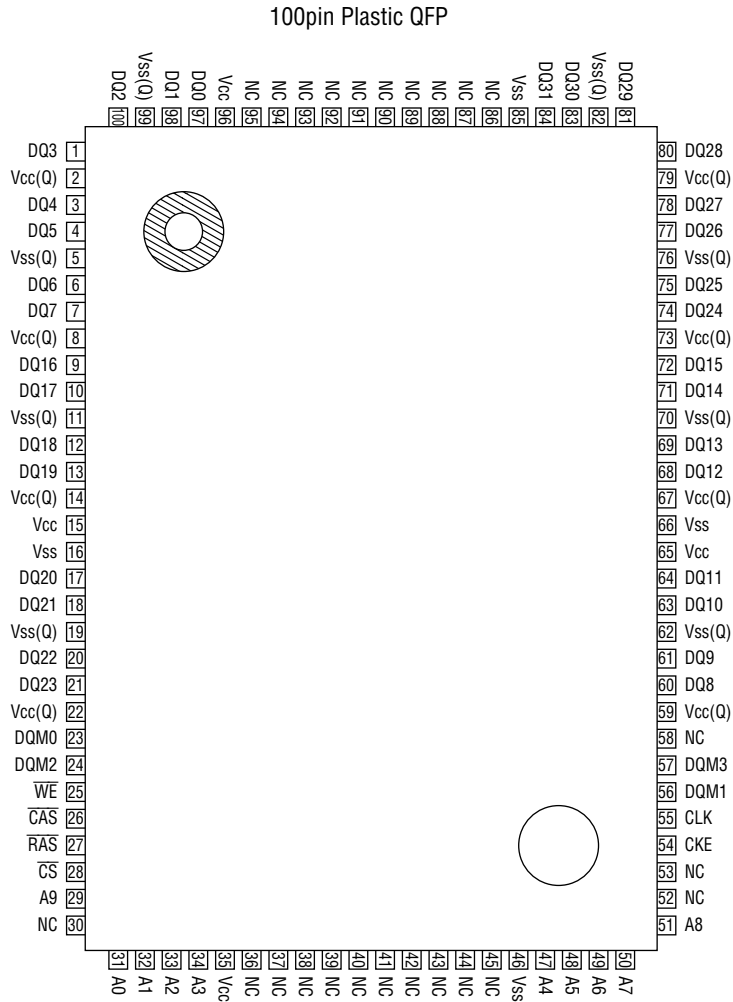
### FEATURES

- 131,072-words × 32 bits × 2 banks memory
- Single 3.3 V±0.3 V power supply
- LVTTTL compatible inputs and outputs
- All input signals are latched at rising edge of system clock
- Auto precharge and controlled precharge
- Internal pipelined operation: column address can be changed every clock cycle
- Dual internal banks controlled by A9 (Bank Address: BA)
- Independent byte operation via DQM0 to DQM3
- Simplified function (No Block write, Write per bit, Single write and Burst stop)
- Programmable burst sequence (Sequential / Interleave)
- Programmable burst length (1, 2, 4, 8 and full page)
- Programmable  $\overline{\text{CAS}}$  latency (1, 2 and 3)
- Power Down operation and Clock Suspend operation
- Auto refresh and Self refresh capability
- 1,024 refresh cycle / 16 ms
- Package :  
100-pin plastic QFP (QFP100-P-1420-0.65-BK4) (Product : MSM54V24632A-xxGS-BK4)  
xx indicates speed rank.

### PRODUCT FAMILY

Family	Clock Frequency MHz (Max.)	Package
MSM54V24632A-8	125	100-pin Plastic QFP (14 × 20 mm)
MSM54V24632A-10	100	
MSM54V24632A-12	83	

**PIN CONFIGURATION (TOP VIEW)**



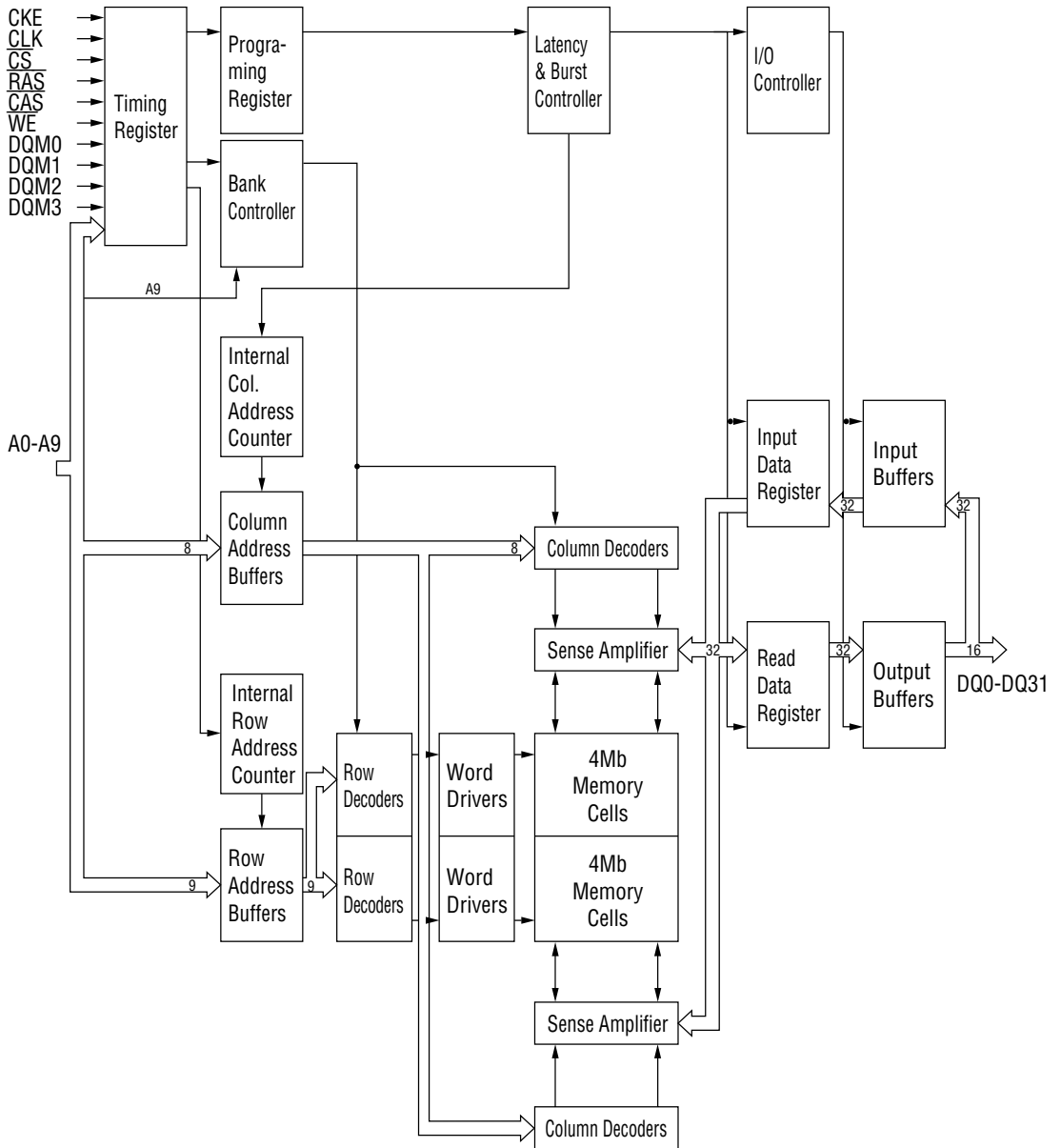
Pin Name	Function	Pin Name	Function
CLK	System Clock	DQM0-DQM3	Data Input/Output Mask
$\overline{CS}$	Chip Select	DQi	Data Input/Output
CKE	Clock Enable	V <sub>CC</sub>	Power Supply (3.3 V)
A0 - A8	Address	V <sub>SS</sub>	Ground (0 V)
A9	Bank Select Address	V <sub>CC(Q)</sub>	Data Output Power Supply (3.3 V)
$\overline{RAS}$	Row Address Strobe	V <sub>SS(Q)</sub>	Data Output Ground (0 V)
$\overline{CAS}$	Column Address Strobe	NC	No Connection
$\overline{WE}$	Write Enable		

Note: The same power supply voltage must be provided to every V<sub>CC</sub> pin and V<sub>CC(Q)</sub> pin. The same GND voltage level must be provided to every V<sub>SS</sub> pin and V<sub>SS(Q)</sub> pin.

## PIN DESCRIPTION

CLK	Fetches all inputs at the "H" edge.
$\overline{\text{CS}}$	Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE, DQM0, DQM1, DQM2 and DQM3.
CKE	Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command.
Address	Row & column multiplexed. Row address: RA0 – RA8 Column address: CA0 – CA7
A9	Selects bank to be activated during row address latch time and selects bank for precharge and read/write during column address latch time. A9= "L" : Bank A, A9= "H" : Bank B
$\overline{\text{RAS}}$ $\overline{\text{CAS}}$ $\overline{\text{WE}}$	Functionality depends on the combination. For details, see the function truth table.
DQM0 ~DQM3	Masks the read data of two clocks later when DQM0~DQM3 is set "H" at the "H" edge of the clock signal. Masks the write data of the same clock when DQM0~DQM3 is set "H" at the "H" edge of the clock signal.
DQi	Data inputs/outputs are multiplexed on the same pin.

**BLOCK DIAGRAM**



## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

(Voltages referenced to  $V_{SS}$ )

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 to 4.6	V
$V_{CC}$ Supply Voltage	$V_{CC}, V_{CCQ}$	-0.5 to 4.6	V
Storage Temperature	$T_{stg}$	-55 to 150	°C
Power Dissipation	$P_D^*$	1	W
Short Circuit Current	$I_{OS}$	50	mA
Operating Temperature	$T_{opr}$	0 to 70	°C

\*:  $T_a = 25^\circ\text{C}$ 

### Recommended Operating Conditions

(Voltages referenced to  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}, V_{CCQ}$	3.0	3.3	3.6	V
Input High Voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.2$	V
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V

### Capacitance

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	$C_{IN1}$	—	5	pF
Input Capacitance (CLK, CKE, $\overline{CS}$ , $\overline{RAS}$ , CAS, WE, DQM0~DQM3)	$C_{IN2}$	—	5	pF
Input/Output Capacitance (DQ0 - DQ31)	$C_{OUT}$	—	7	pF

## DC Characteristics

Parameter	Symbol	Condition			Version						Unit	Note
		Bank	CKE	Others	-8		-10		-12			
					Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	$V_{OH}$	—	—	$I_{OH} = -2 \text{ mA}$	2.4	—	2.4	—	2.4	—	V	
Output Low Voltage	$V_{OL}$	—	—	$I_{OL} = 2 \text{ mA}$	—	0.4	—	0.4	—	0.4	V	
Input Leakage Current	$I_{LI}$	—	—	—	-10	10	-10	10	-10	10	$\mu\text{A}$	
Output Leakage Current	$I_{LO}$	—	—	—	-10	10	-10	10	-10	10	$\mu\text{A}$	
Average Power Supply Current (Operating)	$I_{CC1}$	One Bank Active	$CKE \geq V_{IH}$	$t_{CC} = \text{min}$ $t_{RC} = \text{min}$ No Burst	—	180	—	160	—	140	mA	1, 2
	$I_{CC1D}$	Both Banks Active	$CKE \geq V_{IH}$	$t_{CC} = \text{min}$ $t_{RC} = \text{min}$ $t_{RRD} = \text{min}$ No Burst	—	240	—	200	—	180	mA	1, 2
Power Supply Current (Stand by)	$I_{CC2}$	Both Banks Precharge	$CKE \geq V_{IH}$	$t_{CC} = \text{min}$	—	80	—	70	—	60	mA	3
Average Power Supply Current (Clock Suspension)	$I_{CC3S}$	Both Banks Active	$CKE \leq V_{IL}$	$t_{CC} = \text{min}$	—	35	—	30	—	25	mA	3
Average Power Supply Current (Active Stand by)	$I_{CC3}$	One Bank Active	$CKE \geq V_{IH}$	$t_{CC} = \text{min}$	—	95	—	80	—	70	mA	3
Power Supply Current (Burst)	$I_{CC4}$	Both Banks Active	$CKE \geq V_{IH}$	$t_{CC} = \text{min}$	—	210	—	180	—	160	mA	1, 2
Power Supply Current (Auto-Refresh)	$I_{CC5}$	One Bank Active	$CKE \geq V_{IH}$	$t_{CC} = \text{min}$ $t_{RC} = \text{min}$	—	170	—	150	—	130	mA	2
Average Power Supply Current (Self-Refresh)	$I_{CC6}$	Both Banks Precharge	$CKE \leq V_{IL}$	$t_{CC} = \text{min}$	—	2	—	2	—	2	mA	
Average Power Supply Current (Power down)	$I_{CC7}$	Both Banks Precharge	$CKE \leq V_{IL}$	$t_{CC} = \text{min}$	—	2	—	2	—	2	mA	

- Notes:
1. Measured with outputs open.
  2. Address and data can be changed once or not be changed during one cycle.
  3. Address and data can be changed once or not be changed during two cycles.

**Mode Set Address Keys**

Operation Code			$\overline{\text{CAS}}$ Latency				Burst Type		Burst Length				
A8	A7	TM	A6	A5	A4	CL	A3	BT	A2	A1	A0	BT = 0	BT = 1
0	0	Mode Setting	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	1	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
			1	0	0	Reserved			1	0	0	Reserved	Reserved
			1	0	1	Reserved			1	0	1	Reserved	Reserved
			1	1	0	Reserved			1	1	0	Reserved	Reserved
			1	1	1	Reserved			1	1	1	Full Page	Reserved

Note: A9 should stay "L" during mode set cycle.

**POWER ON SEQUENCE**

1. With inputs in NOP state, turn on the power supply and start the system clock.
2. After the  $V_{CC}$  voltage has reached the specified level, pause for 200  $\mu\text{s}$  or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Apply an Auto-refresh eight or more times.
5. Enter the mode register setting command.

## AC Characteristics 1

Note 1, 2

Parameter		Symbol	MSM54V24632A-8		MSM54V24632A-10		MSM54V24632A-12		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Clock Cycles Time	CL = 3	t <sub>CC</sub>	8	—	10	—	12	—	ns	
	CL = 2		12	—	15	—	18	—	ns	
	CL = 1		24	—	30	—	36	—	ns	
Access Time from Clock	CL = 3	t <sub>AC</sub>	—	7	—	9	—	10	ns	3, 4
	CL = 2		—	10	—	13	—	15	ns	3, 4
	CL = 1		—	22	—	27	—	32	ns	3, 4
Clock "H" Pulse Time		t <sub>CH</sub>	2.5	—	3	—	4	—	ns	
Clock "L" Pulse Time		t <sub>CL</sub>	2.5	—	3	—	4	—	ns	
Input Setup Time		t <sub>SI</sub>	2.5	—	3	—	3	—	ns	
Input Hold Time		t <sub>HI</sub>	1	—	1	—	1.5	—	ns	
Output Low Impedance Time form Clock		t <sub>OLZ</sub>	3	—	3	—	3	—	ns	
Output High Impedance Time form Clock		t <sub>OHZ</sub>	—	6	—	8	—	10	ns	
Output Hold from Clock		t <sub>OH</sub>	3	—	3	—	3	—	ns	3
RAS Cycle Time		t <sub>RC</sub>	72	—	90	—	106	—	ns	
RAS Precharge Time		t <sub>RP</sub>	24	—	30	—	36	—	ns	
RAS Active Time		t <sub>RAS</sub>	48	10 <sup>5</sup>	60	10 <sup>5</sup>	72	10 <sup>5</sup>	ns	
RAS to CAS Delay Time		t <sub>RCD</sub>	24	—	30	—	36	—	ns	
Write Recovery Time		t <sub>WR</sub>	16	—	20	—	24	—	ns	
Write Command Input Time form Output		t <sub>OWD</sub>	16	—	20	—	24	—	ns	
RAS to RAS Bank Active Delay Time		t <sub>RRD</sub>	16	—	20	—	24	—	ns	
Refresh Time		t <sub>REF</sub>	—	16	—	16	—	16	ms	
Power-down Exit Set-up Time		t <sub>PDE</sub>	8	—	10	—	12	—	ns	
Input Level Transition Time		t <sub>T</sub>	1	5	1	5	1	5	ns	

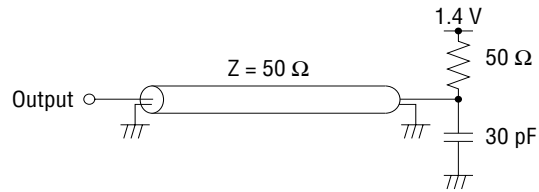


AC Characteristics 2

Note 1, 2

Parameter	Symbol	MSM54V24632A-8			MSM54V24632A-10			MSM54V24632A-12			Unit	Note
CL		3	2	1	3	2	1	3	2	1		
t <sub>CK</sub>		8	12	24	10	15	30	12	18	36	ns	
CAS to $\overline{\text{CAS}}$ Delay Time (Min.)	I <sub>CCD</sub>	1	1	1	1	1	1	1	1	1	Cycle	
Clock Disable Time from CKE	I <sub>CKE</sub>	1	1	1	1	1	1	1	1	1	Cycle	
Data Output High Impedance Time from DQM	I <sub>DOZ</sub>	2	2	2	2	2	2	2	2	2	Cycle	
Data Input Mask Time from DQM	I <sub>DOD</sub>	0	0	0	0	0	0	0	0	0	Cycle	
Data Input Time from Write Command	I <sub>DWD</sub>	0	0	0	0	0	0	0	0	0	Cycle	
Data Output High Impedance Time from Precharge Command	I <sub>ROH</sub>	2	2	1	2	2	1	2	2	1	Cycle	
Active Command Input Time from Mode Register Set Command Input (Min.)	I <sub>MRD</sub>	3	3	3	3	3	3	3	3	3	Cycle	

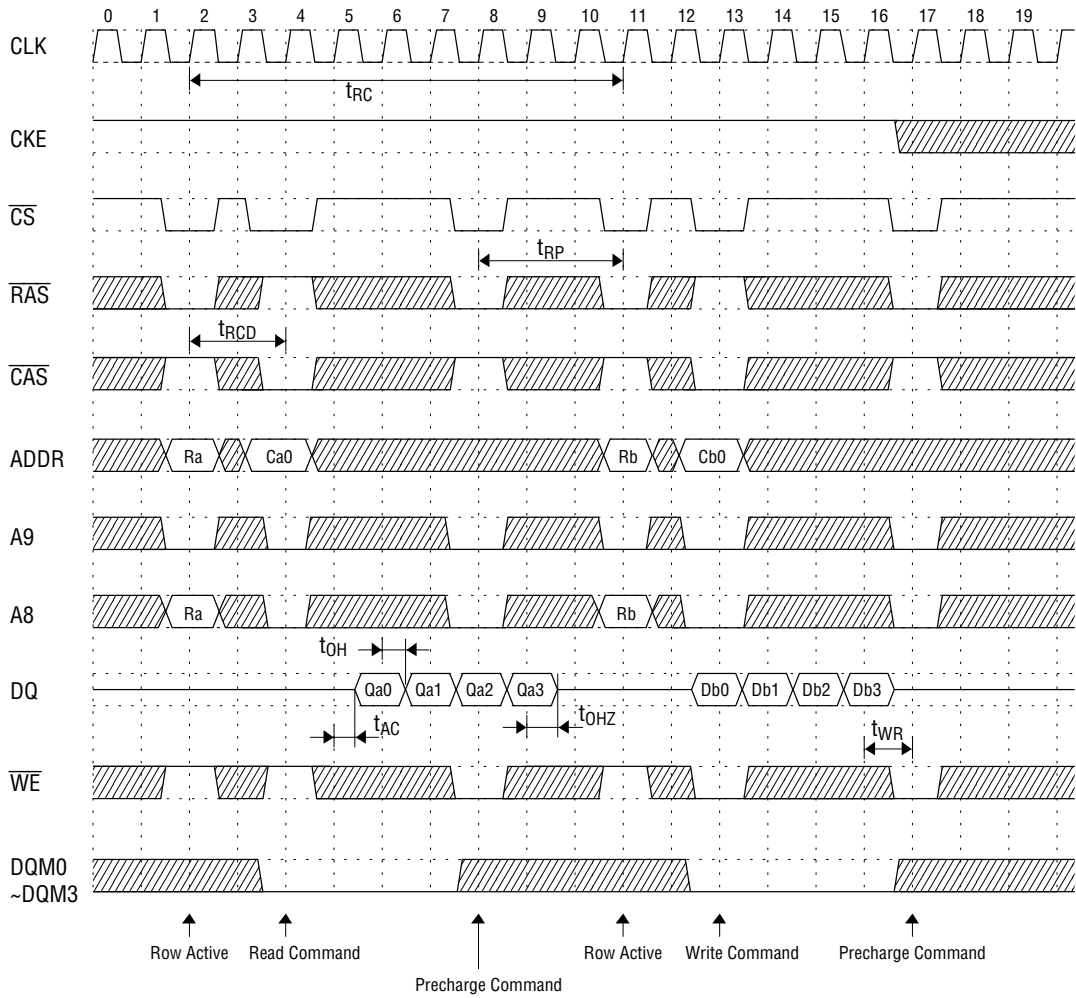
- Notes :
1. AC measurements assume  $t_T = 1$  ns.
  2. The reference level for timing of input signals is 1.4 V.
  3. Output load.



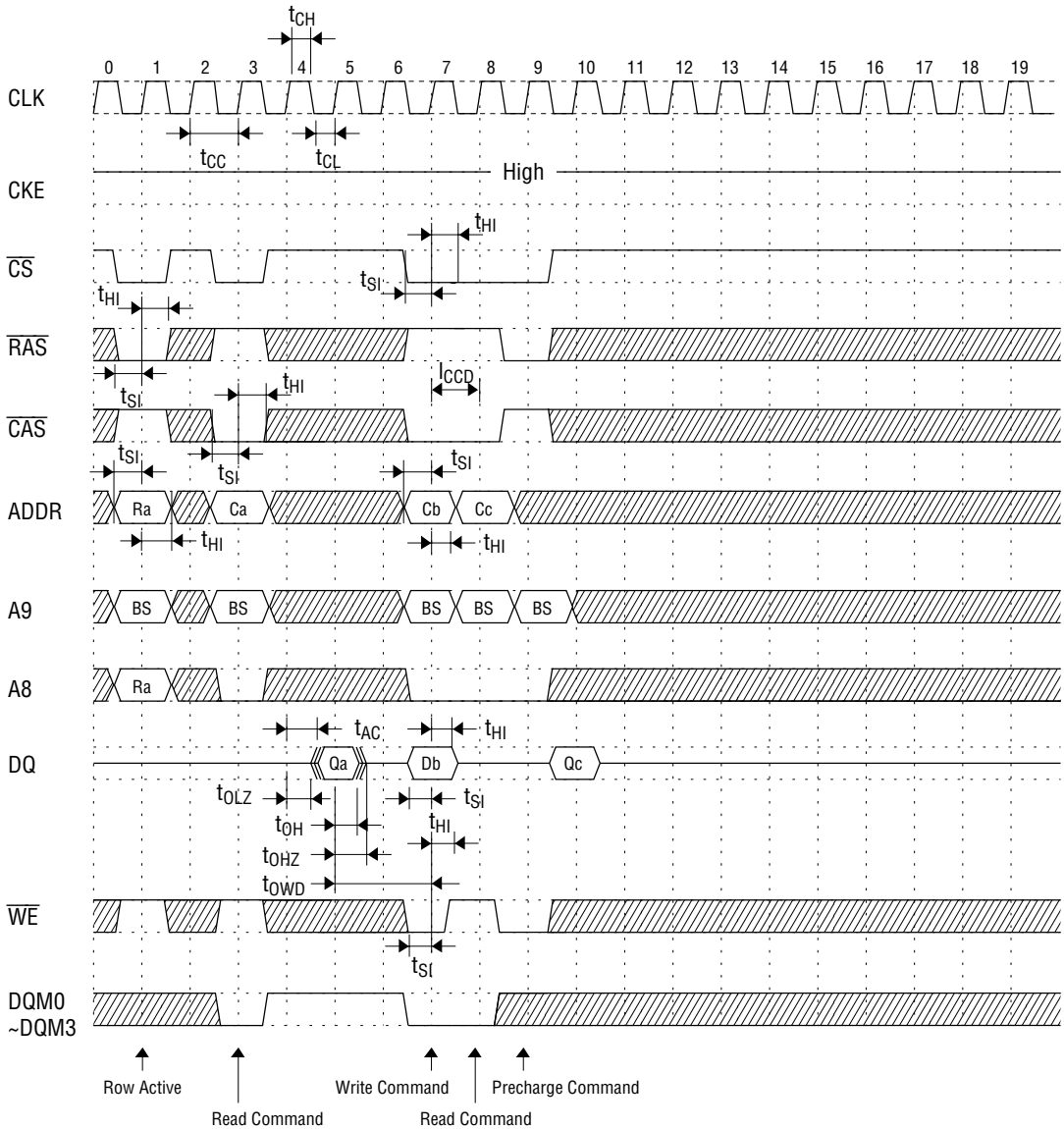
4. An access time is measured at 1.4 V.
5. If  $t_T$  is longer than 1ns, the reference level for timing of input signals is  $V_{IH}$  and  $V_{IL}$ .

**TIMING WAVEFORM**

**Read & Write Cycle (Same Bank) @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4**



Single Bit Read-Write-Read Cycle (Same Page) @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4



- \*Notes:**
1. When  $\overline{CS}$  is set "High" at a clock transition from "Low" to "High", all inputs except CKE and DQM0, DQM1, DQM2, DQM3 are invalid.
  2. When issuing an active, read or write command, the bank is selected by A9.

A9	Active, read or write
0	Bank A
1	Bank B

3. The auto precharge function is enabled or disabled by the A8 input when the read or write command is issued.

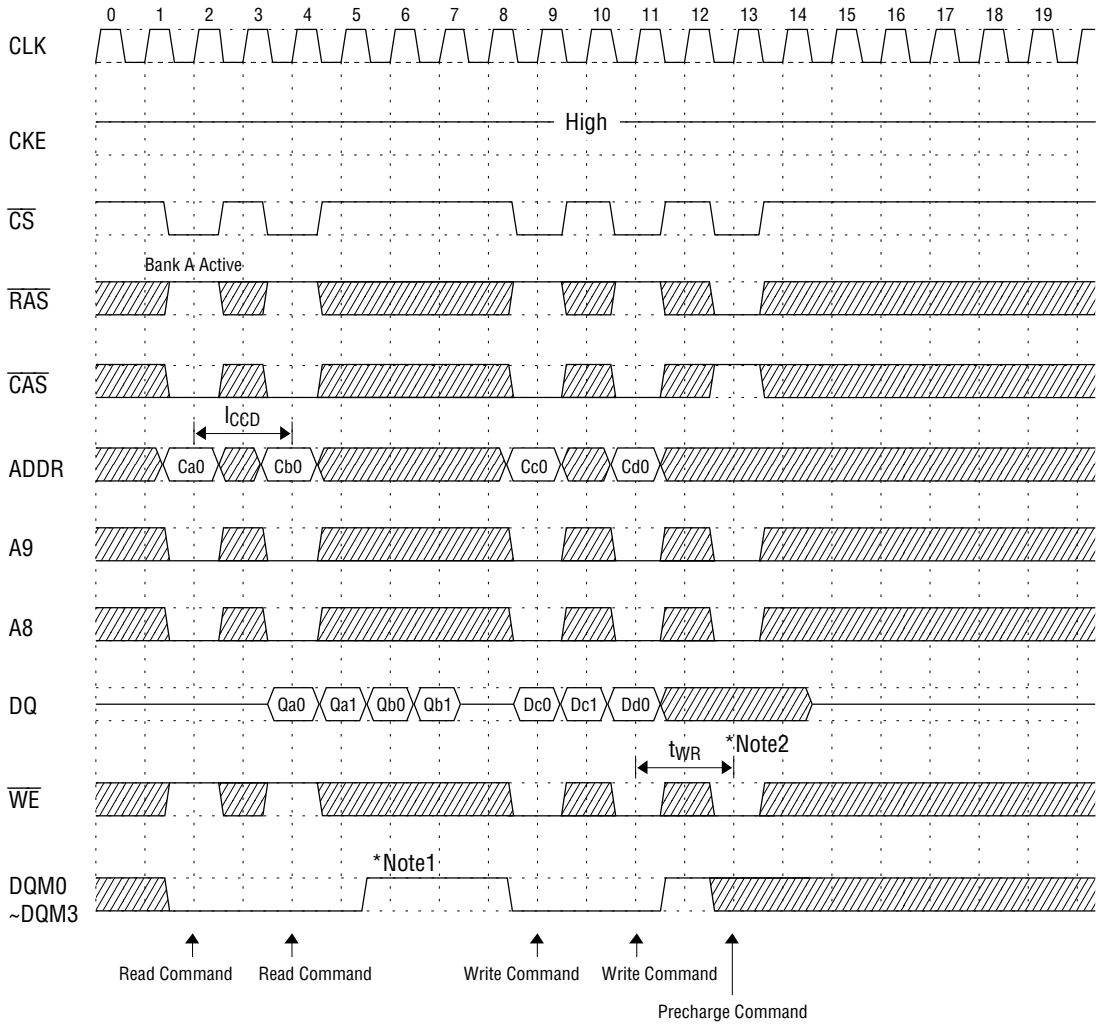
A8	A9	Operation
0	0	After the end of burst, bank A holds the active status.
1	0	After the end of burst, bank A is precharged automatically.
0	1	After the end of burst, bank B holds the active status.
1	1	After the end of burst, bank B is precharged automatically.

4. When issuing a precharge command, the bank to be precharged is selected by the A8 and A9 inputs.

A8	A9	Operation
0	0	Bank A is precharged.
0	1	Bank B is precharged.
1	X	Both banks A and B are precharged.

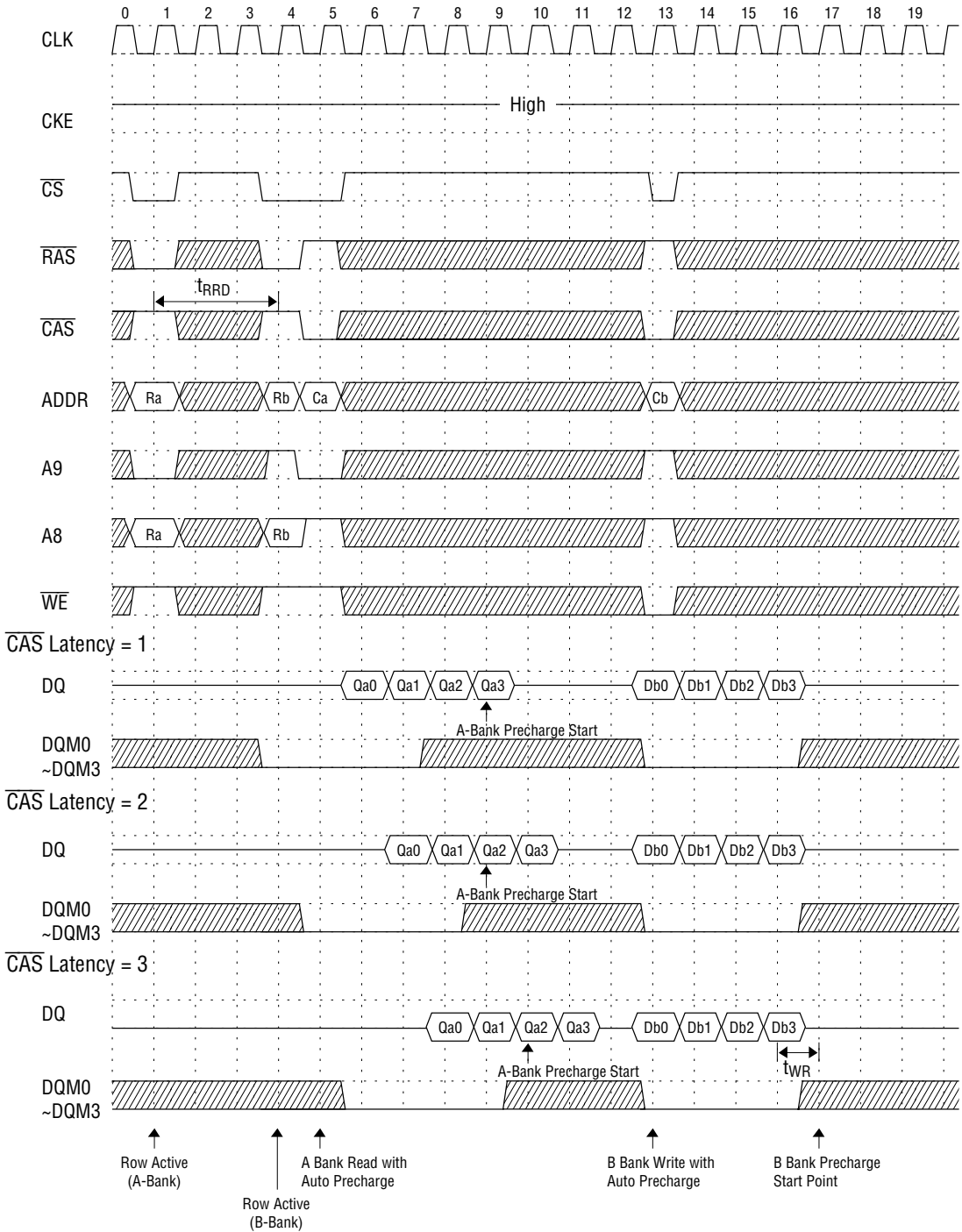
5. The input data and the write command are latched by the same clock (Write latency = 0).
6. The output is forced to high impedance by  $(1 \text{ CLK} + t_{0HZ})$  after DQM<sub>i</sub> entry.

Page Read & Write Cycle (Same Bank) @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4

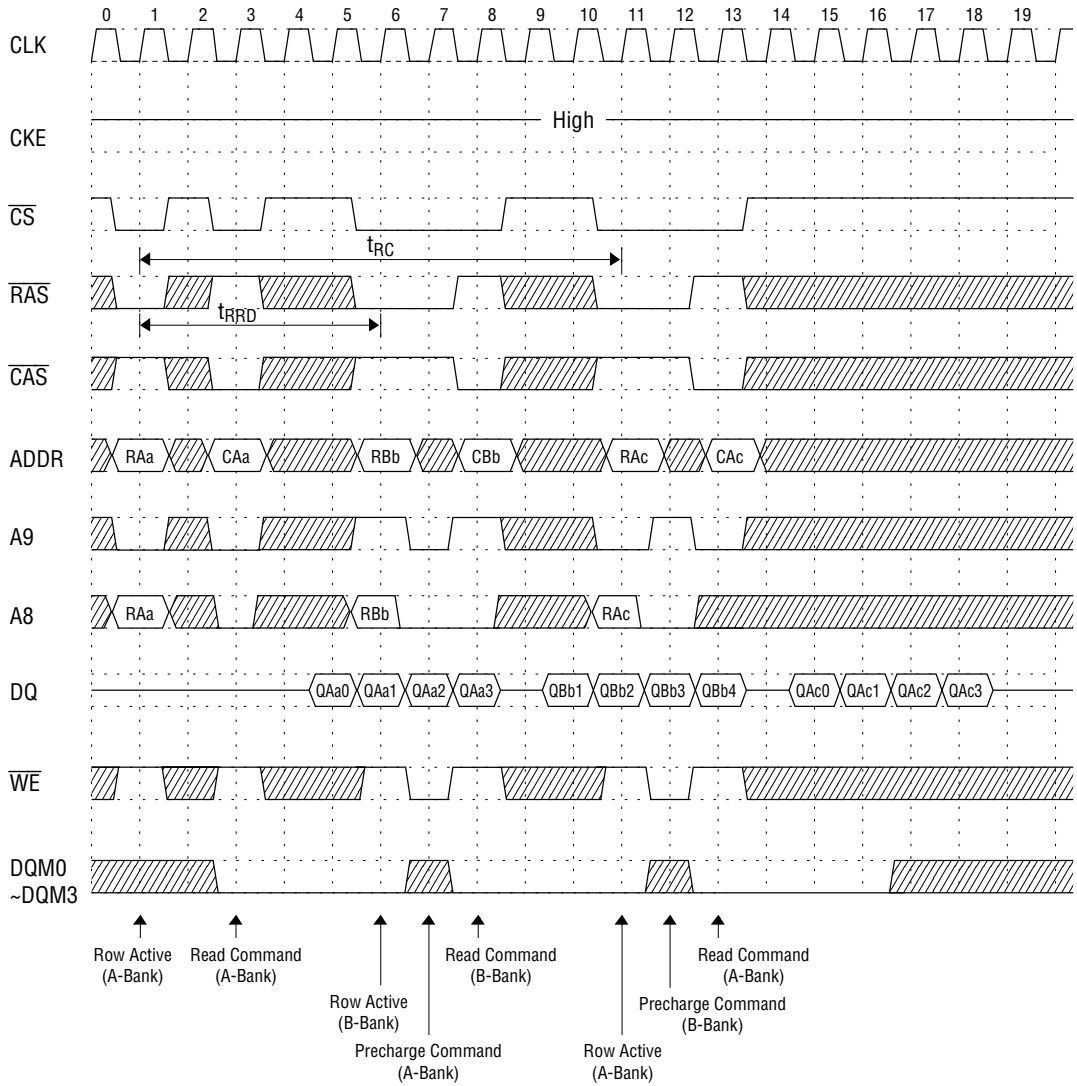


- \*Notes:**
1. To write data before a burst read ends, DQMi should be asserted three cycles prior to the write command, to avoid bus contention.
  2. To assert row precharge before a burst write ends, wait  $t_{\text{WR}}$  after the last write data input. Input data during the precharge input cycle will be masked internally.

Read & Write Cycle with Auto Precharge @ Burst Length = 4

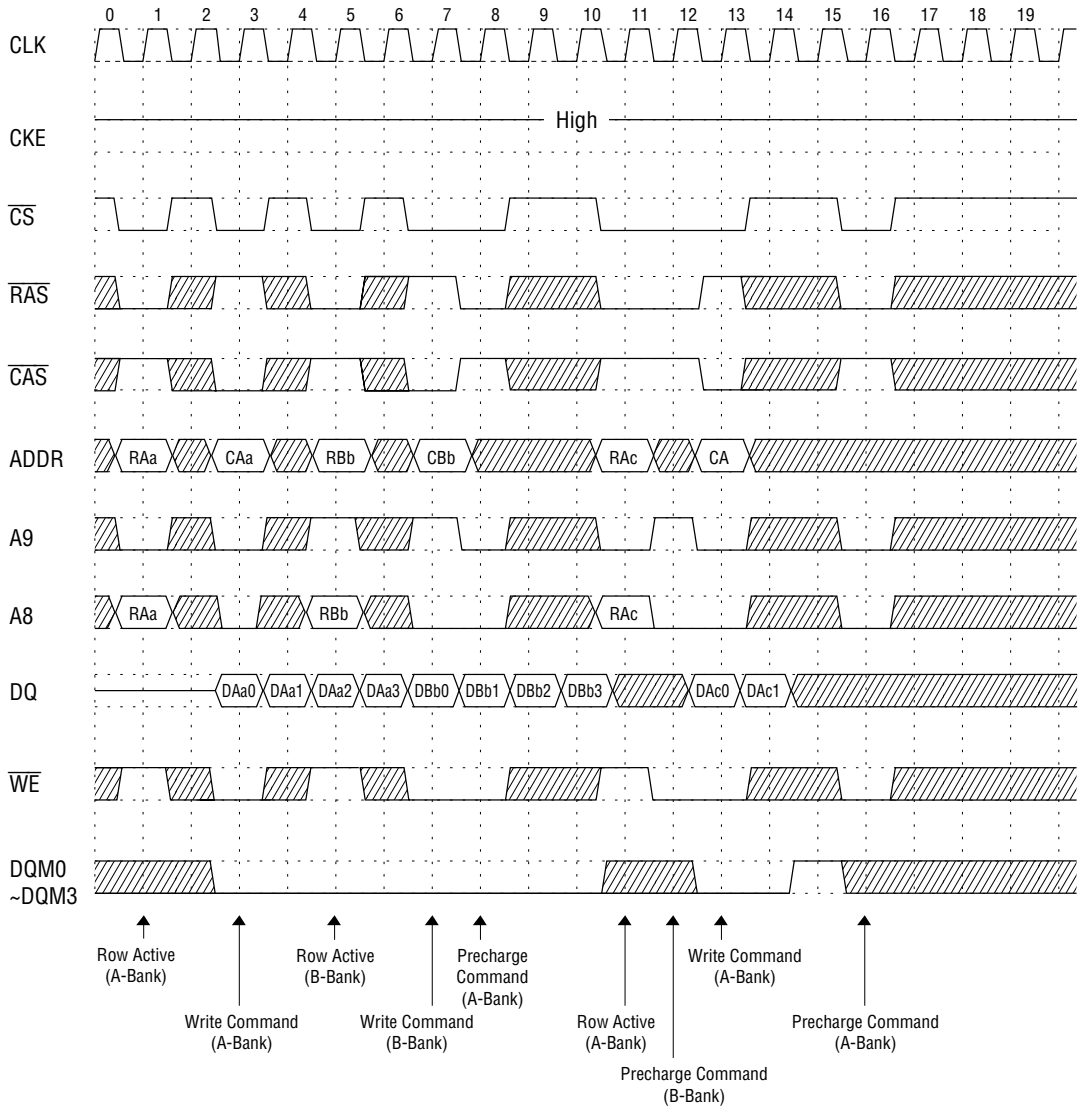


Bank Interleave Random Row Read Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4

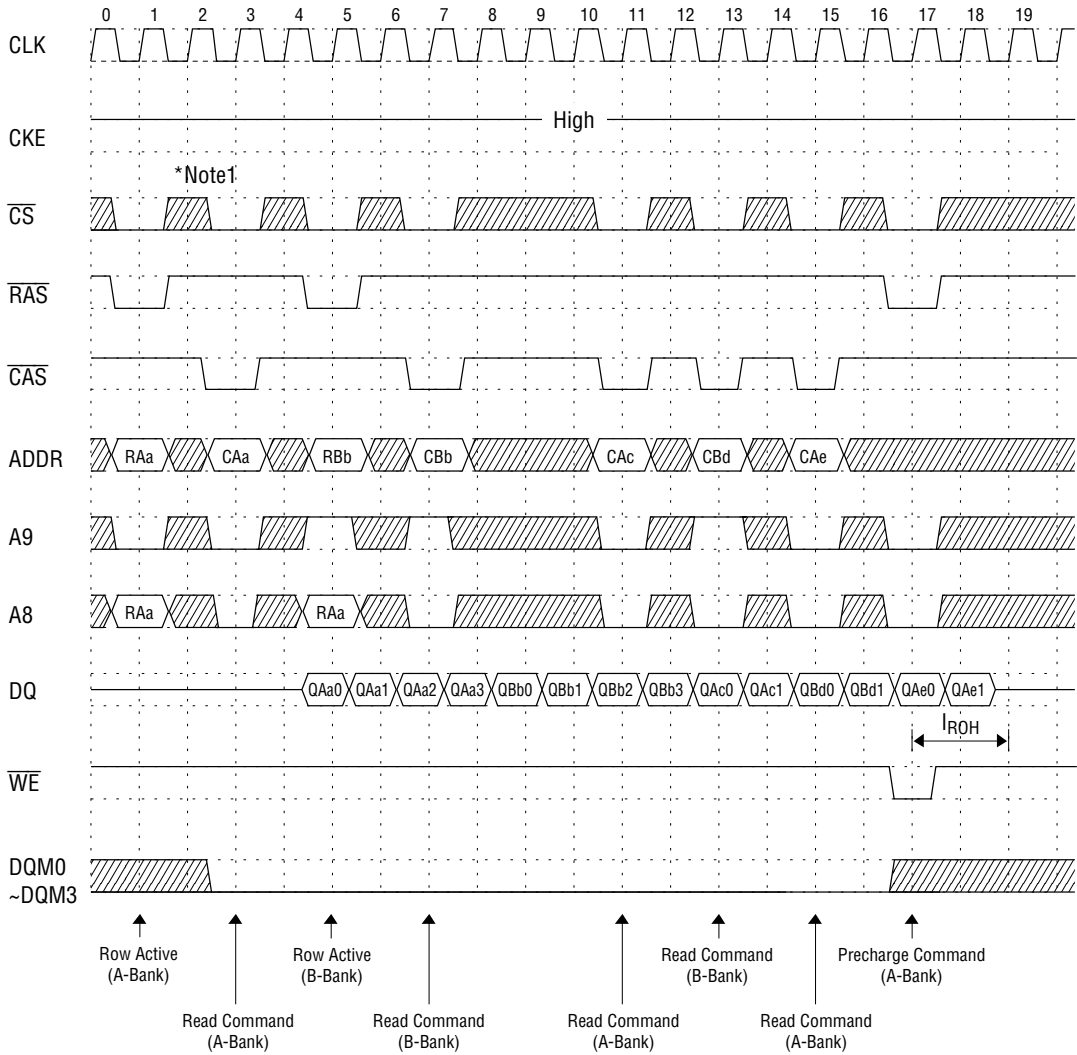




**Bank Interleave Random Row Write Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4**

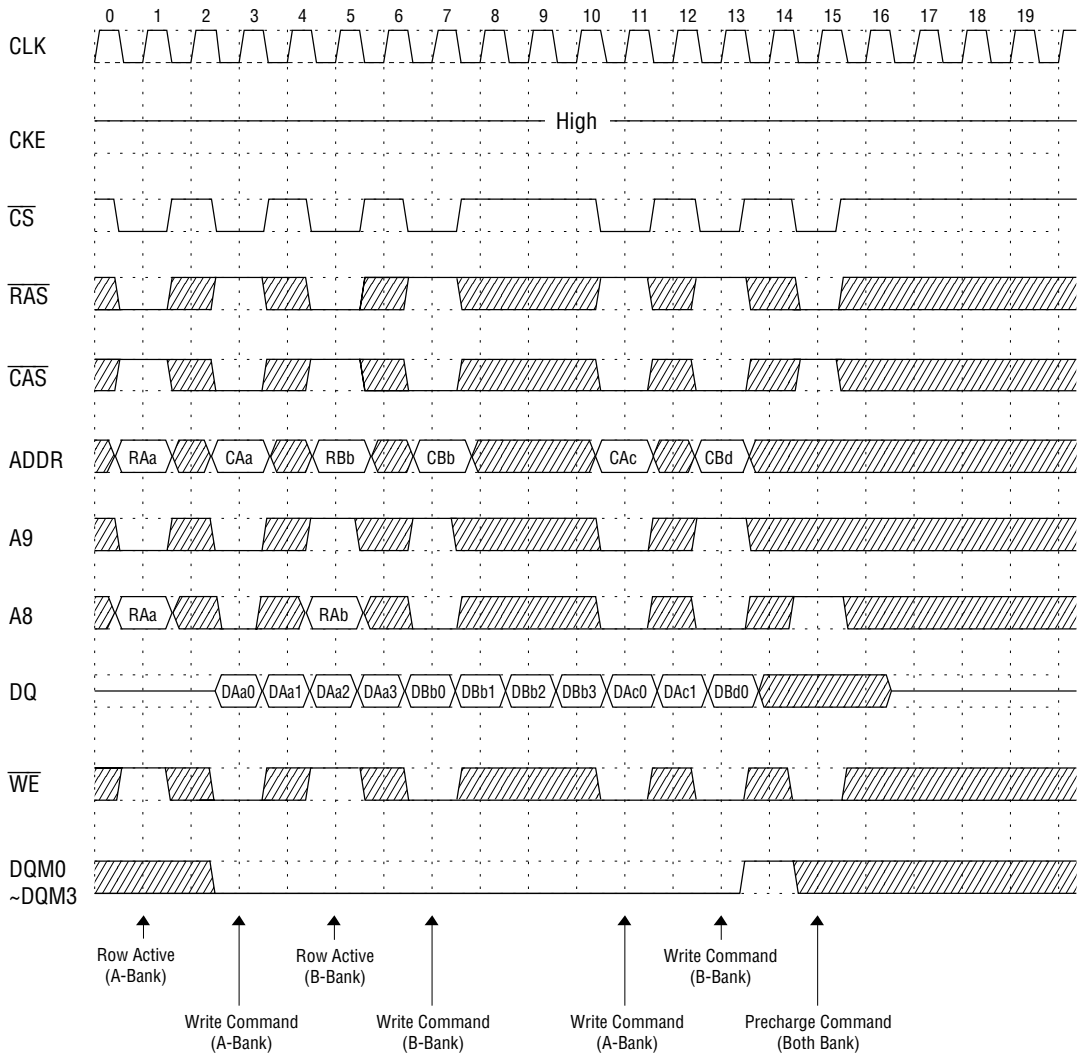


Bank Interleave Page Read Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4

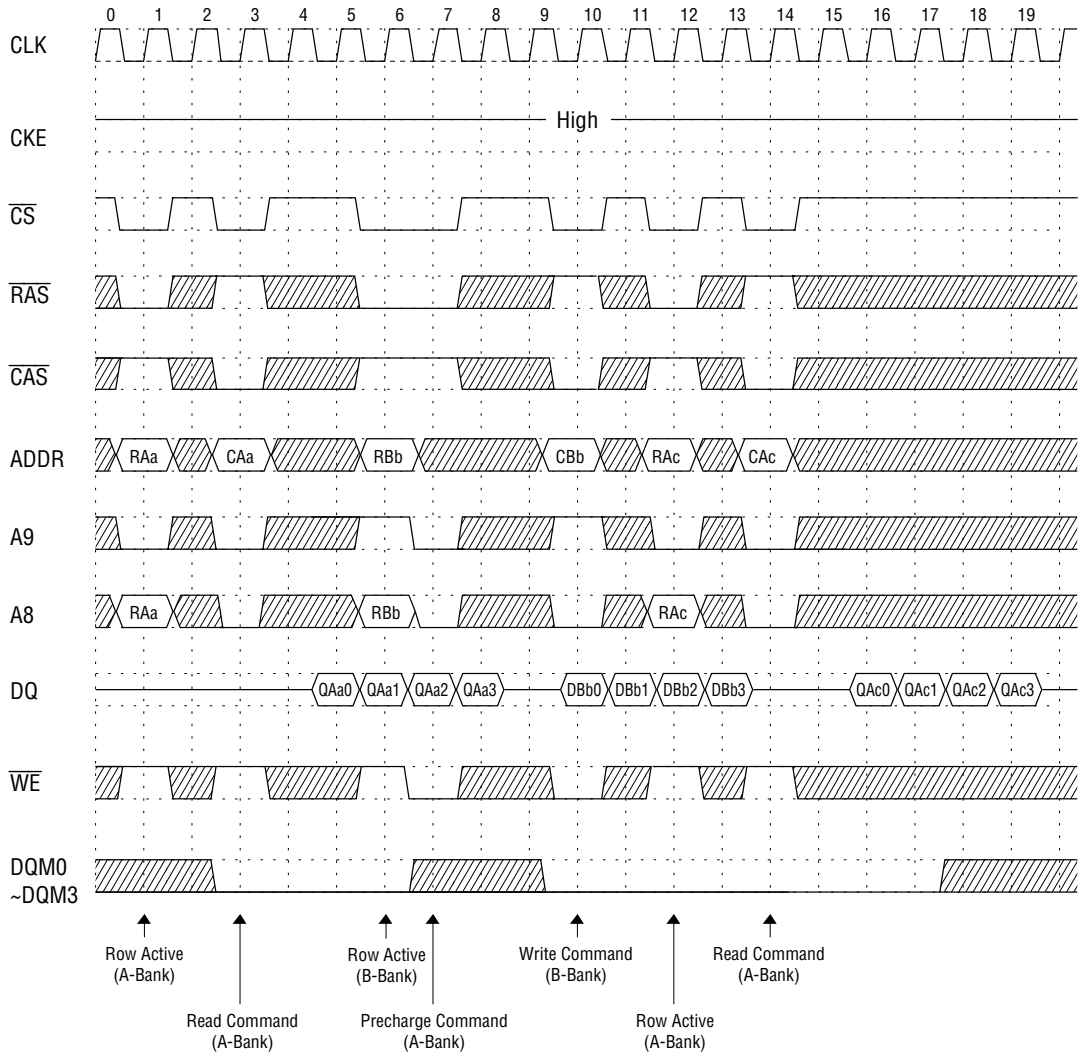


**\*Note:** 1.  $\overline{\text{CS}}$  is ignored when  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  and  $\overline{\text{WE}}$  are high at the same cycle.

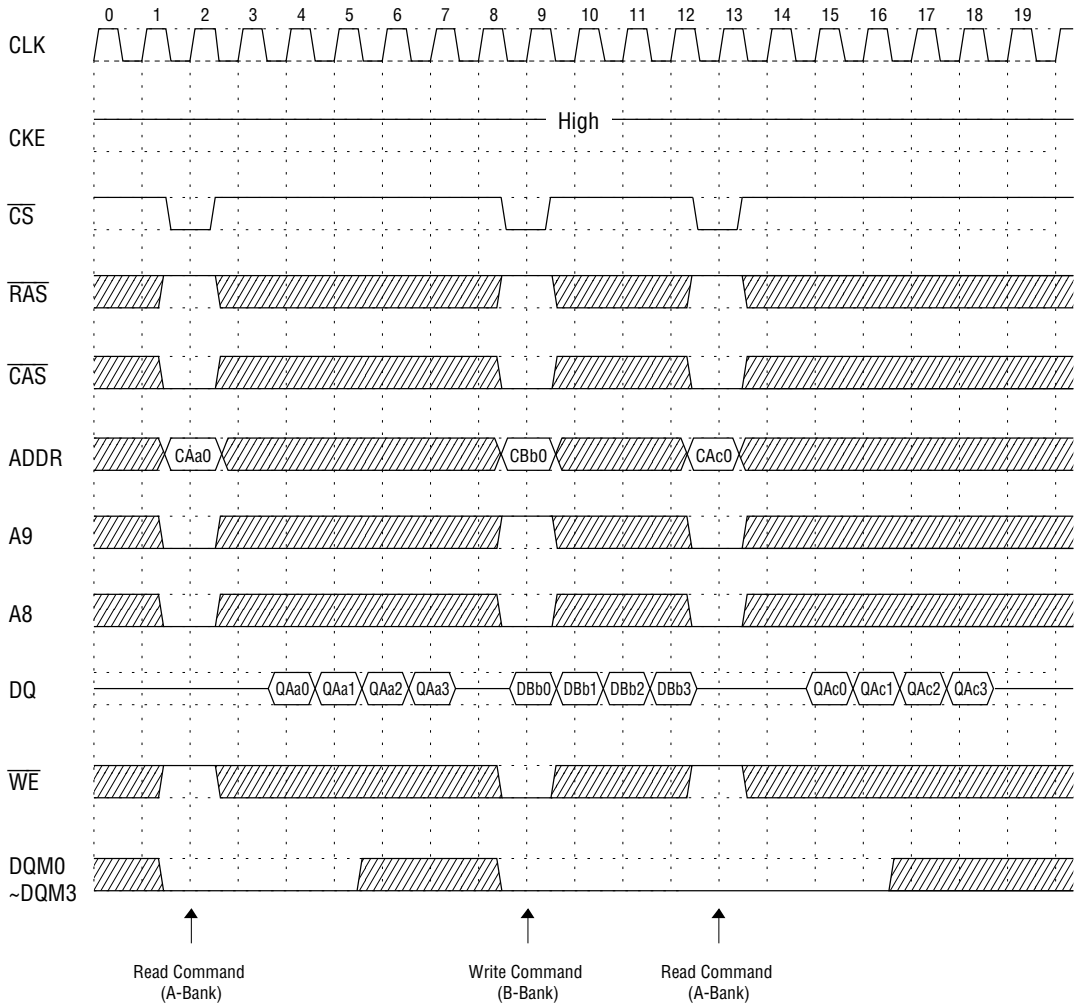
Bank Interleave Page Write Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4



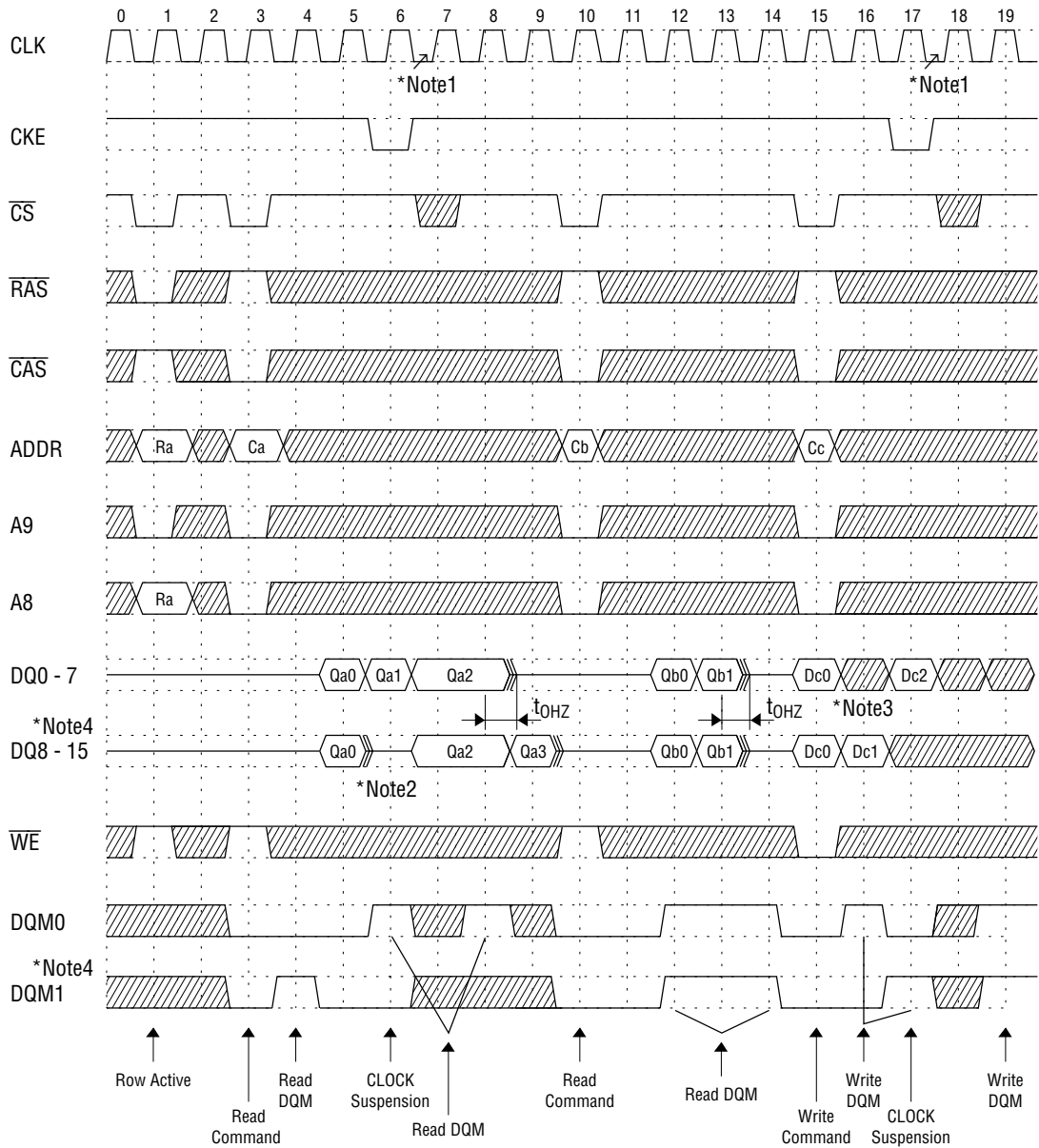
Bank Interleave Random Row Read/Write Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4



Bank Interleave Page Read/Write Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4

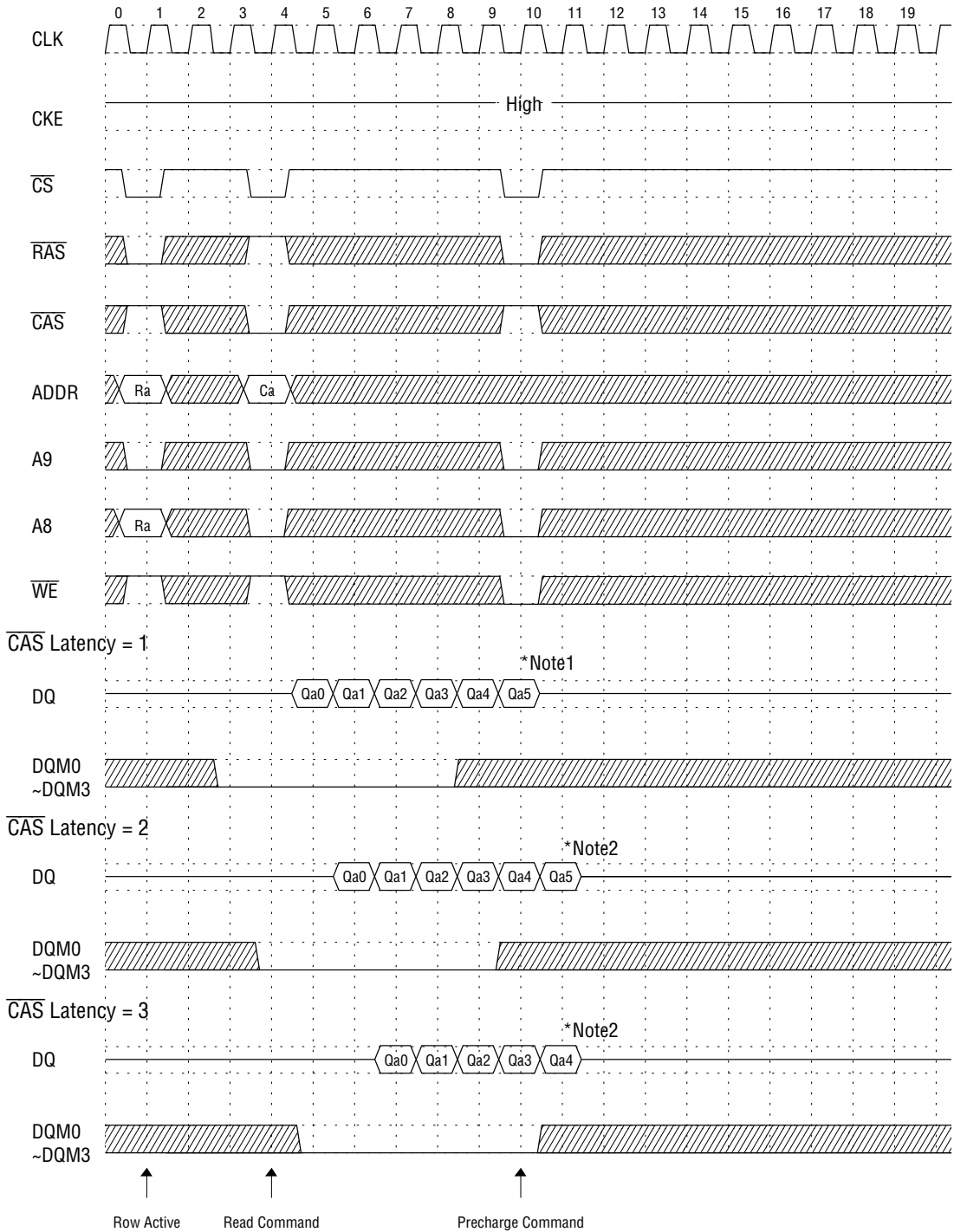


**Clock Suspension & DQM Operation Cycle @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4**



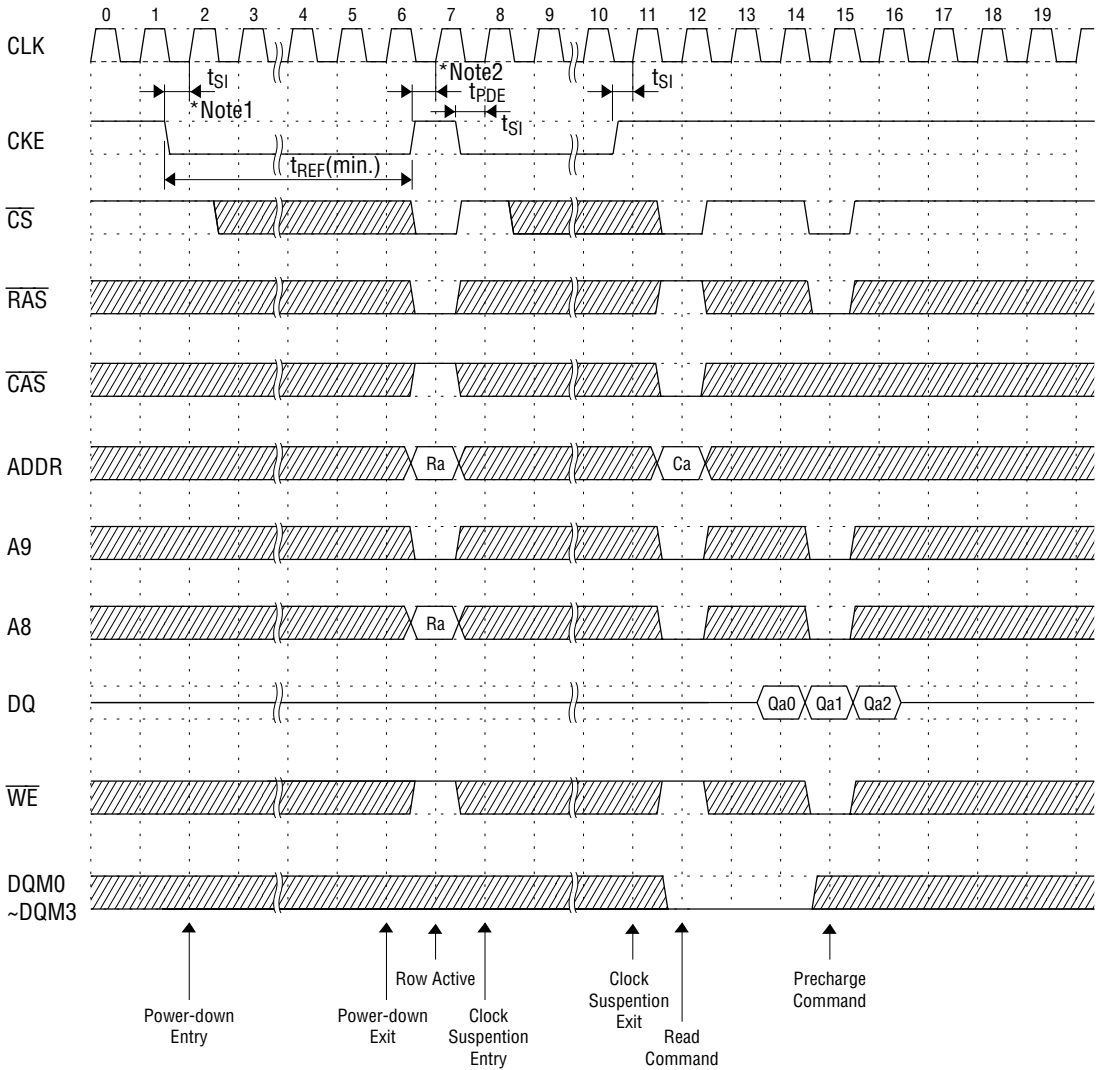
- \*Notes:**
1. When CKE is deactivated, the next clock cycle will be ignored.
  2. When DQMs are asserted, the read data after two clock cycles will be masked.
  3. When DQMs are asserted, the write data in the same clock cycle will be masked.
  4. When DQM0 is set High, the input/output data of DQ0 - DQ7 will be masked.  
 When DQM2 is set High, the input/output data of DQ8 - DQ15 will be masked.  
 When DQM3 is set High, the input/output data of DQ16 - DQ23 will be masked.  
 When DQM4 is set High, the input/output data of DQ24 - DQ31 will be masked.

Read Interruption by Precharge Command @ Burst Length = 8



- \*Notes:**
1. When  $\overline{\text{CAS}}$  latency = 1, and if row precharge is asserted before a burst read ends, then the read data will not output after the next clock cycle of precharge command.
  2. If row precharge is asserted before burst read ends when  $\overline{\text{CAS}}$  latency = 2 or 3, then the read data will not output after the second clock cycle of the precharge command.

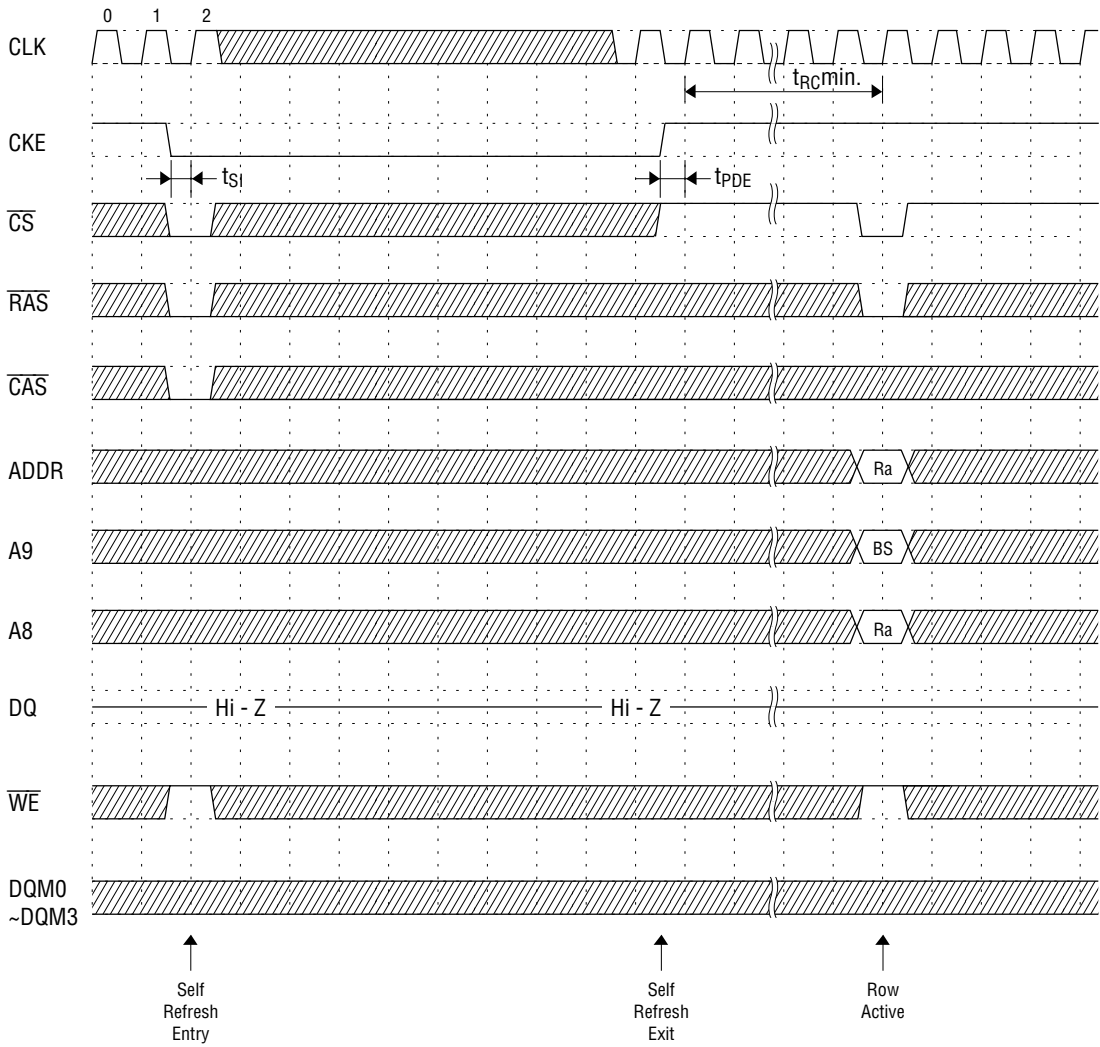
Power Down Mode @  $\overline{\text{CAS}}$  Latency = 2, Burst Length = 4



- \*Notes:**
1. When both banks are in precharge state, and if CKE is set low, then the MSM54V24632A enters power-down mode and maintains the mode while CKE is low.
  2. To release the circuit from power-down mode, set CKE high for longer than  $t_{PDE}$ , and the inputs will be set within the same cycle.

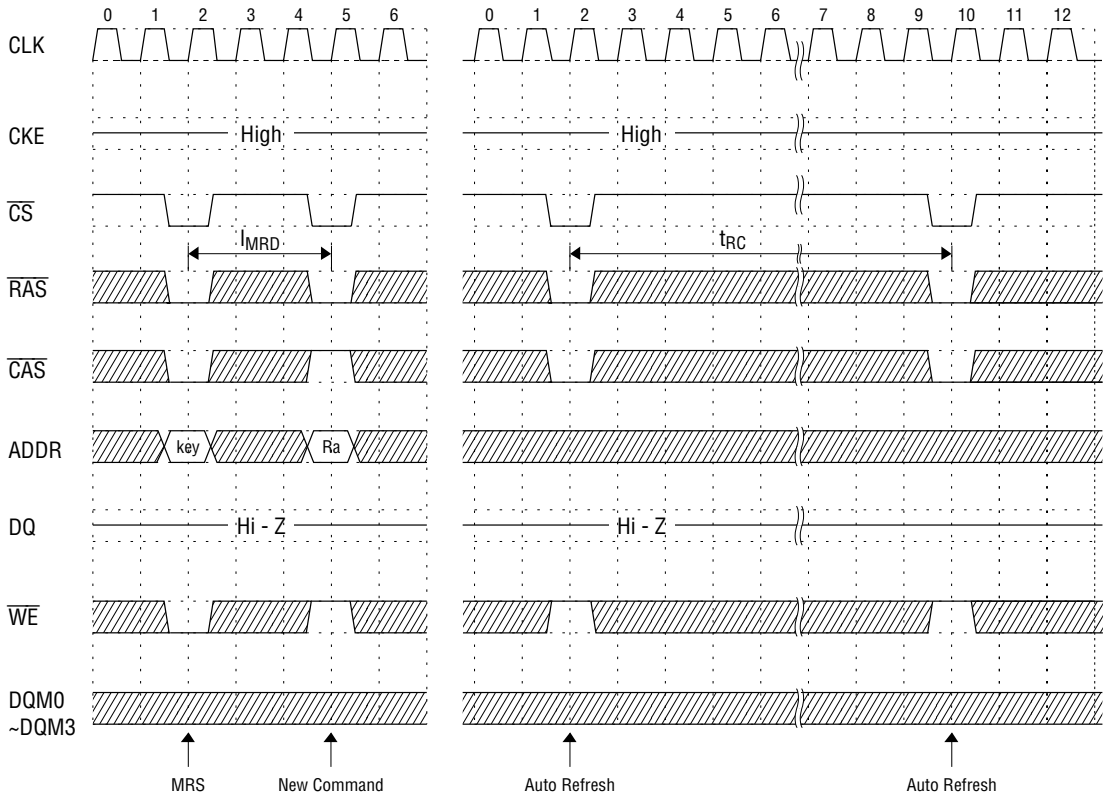


Self Refresh Cycle



Mode Register Set Cycle

Auto Refresh Cycle



**FUNCTION TRUTH TABLE (Table 1) (1/2)**

Current State <sup>1</sup>	CS	RAS	CAS	WE	BA	ADDR	Action
Idle	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	Row Active
	L	L	H	L	BA	A8	NOP <sup>4</sup>
	L	L	L	H	X	X	Auto-Refresh or Self-Refresh <sup>5</sup>
	L	L	L	L		OP Code	Mode Register write
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BA	CA, A8	Read
	L	H	L	L	BA	CA, A8	Write
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A8	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	Reserved
	L	H	L	H	BA	CA, A8	Term Burst, start new Burst Read
	L	H	L	L	BA	CA, A8	Term Burst, start new Burst Write
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A8	Term Burst, execute Row Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	Reserved (Term Burst) --> Row Active
	L	H	L	H	BA	CA, A8	Term Burst, Start new Burst Read
	L	H	L	L	BA	CA, A8	Term Burst, start new Burst write
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A8	Term Burst, execute Row Precharge
	L	L	L	X	X	X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	H	BA	CA, A8	ILLEGAL <sup>2</sup>
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A8	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	H	BA	CA, A8	ILLEGAL <sup>2</sup>
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A8	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL

## FUNCTION TRUTH TABLE (Table 1) (2/2)

Current State <sup>1</sup>	CS	RAS	CAS	WE	BA	ADDR	Action
Precharge	H	X	X	X	X	X	NOP --> Idle after $t_{RP}$
	L	H	H	H	X	X	NOP --> Idle after $t_{RP}$
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A8	NOP <sup>4</sup>
	L	L	L	X	X	X	ILLEGAL
Write Recovery	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A8	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Row Active	H	X	X	X	X	X	NOP --> Row Active after $t_{RCD}$
	L	H	H	H	X	X	NOP --> Row Active after $t_{RCD}$
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A8	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Refresh	H	X	X	X	X	X	NOP --> Idle after $t_{RC}$
	L	H	H	X	X	X	NOP --> Idle after $t_{RC}$
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Mode Register Access	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

## ABBREVIATIONS

RA = Row Address

BA = Bank Address

NOP = No Operation command

CA = Column Address

AP = Auto Precharge

- Notes:
1. All inputs will be enabled when CKE is set high for at least 1 cycle prior to the inputs.
  2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
  3. Satisfy the timing of  $t_{CCD}$  and  $t_{WR}$  to prevent bus contention.
  4. NOP to bank precharging or in idle state. Precharges activated bank by BA or A8.
  5. Illegal if any bank is not idle.

**FUNCTION TRUTH TABLE for CKE (Table 2)**

Current State (n)	CKEn-1	CKEn	$\overline{CS}$	RAS	CAS	$\overline{WE}$	ADDR	Action
Self Refresh <sup>6</sup>	H	x	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh --> ABI
	L	H	L	H	H	H	X	Exit Self Refresh --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)
Power Down <sup>6</sup>	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Power Down --> ABI
	L	H	L	H	H	H	X	Exit Power Down --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL <sup>7</sup>
	L	L	X	X	X	X	X	NOP (Continue power down mode)
All Banks Idle <sup>7</sup> (ABI)	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	L	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State Other than Listed Above	H	H	X	X	X	X	X	Refer to Operations in Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend Next Cycle
	L	H	X	X	X	X	X	Enaole Clock of Next Cycle
	L	L	X	X	X	X	X	Continue Clock Suspension

- Notes:
- 6. If a minimum set-up time  $t_{PDE}$  is satisfied when CKE transitions from "L" to "H", CKE operates asynchronously so that a command can be input in the same internal clock cycle.
  - 7. Power-down and self refresh can be entered only when all the banks are in an idle state.