SONY

CXA2074Q/S

US Audio Multiplexing Decoder

Description

The CXA2074Q/S is an IC designed as a decoder for the Zenith TV Multi-channel System and also corresponds with I²C BUS. Functions include stereo demodulation, SAP (Separate Audio Program) demodulation, dbx noise reduction and sound processor. Various kinds of filters are built in while adjustment, mode control and sound processor control are all executed through I²C BUS.

Features

- Audio multiplexing decoder, dbx noise reduction decoder and sound processor are all included in a single chip. Almost any sort of signal processing is possible through this IC.
- All adjustments are possible through I²C BUS to allow for automatic adjustment.
- Various built-in filter circuits greatly reduce external parts.
- There are three systems for inputs and two systems for outputs, and each mode control is possible.

Standard I/O Level

[( ) is the pin No. for the CXA2074S.]

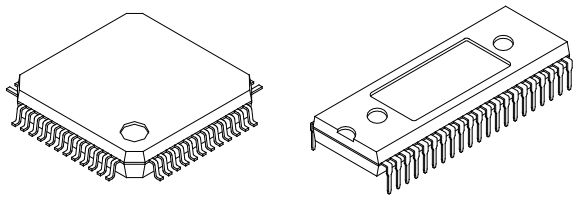
- Input level

COMPIN (Pin 17)	245mVrms
AUX1-L/R (Pins 36 and 35)	490mVrms
AUX2-L/R (Pins 38 and 37)	490mVrms

- Output level

LPOUT-L/R (Pins 40 and 39)	490mVrms
LSOUT-L/R (Pins 8 and 7)	490mVrms

CXA2074Q	CXA2074S
48 pin QFP (Plastic)	42 pin SDIP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	11	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation			
	P_D	0.6 (48 pin QFP)	W
		2.2 (42 pin SDIP)	W

Range of Operating Supply Voltage

9 ± 0.5 V

Applications

TV, VCR and other decoding systems for US audio multiplexing TV broadcasting

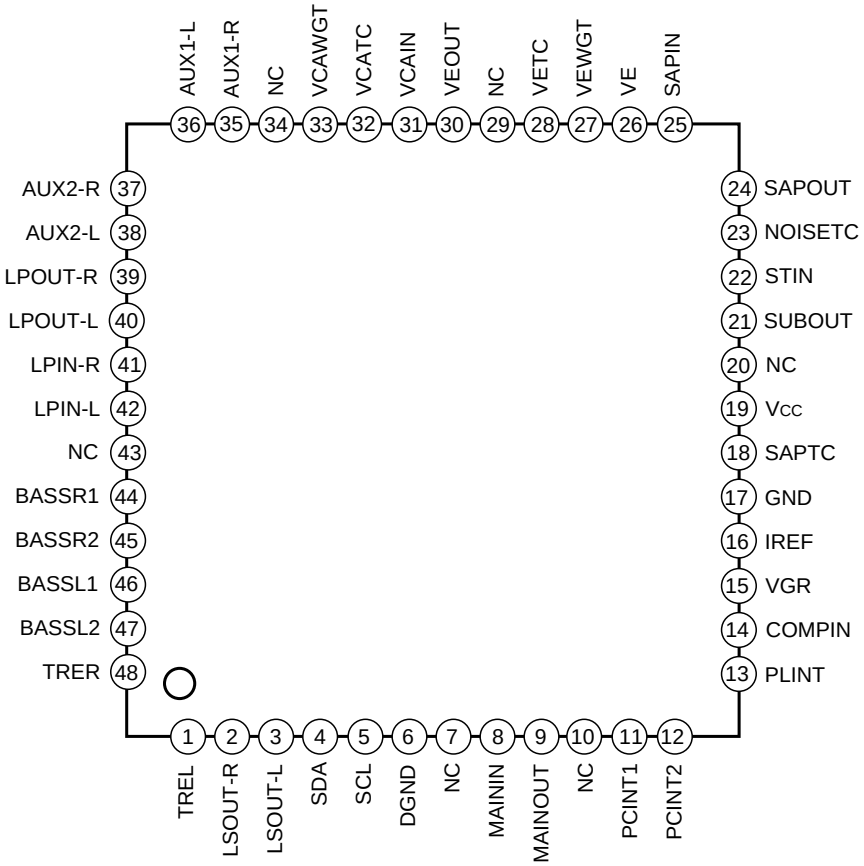
Structure

Bipolar silicon monolithic IC

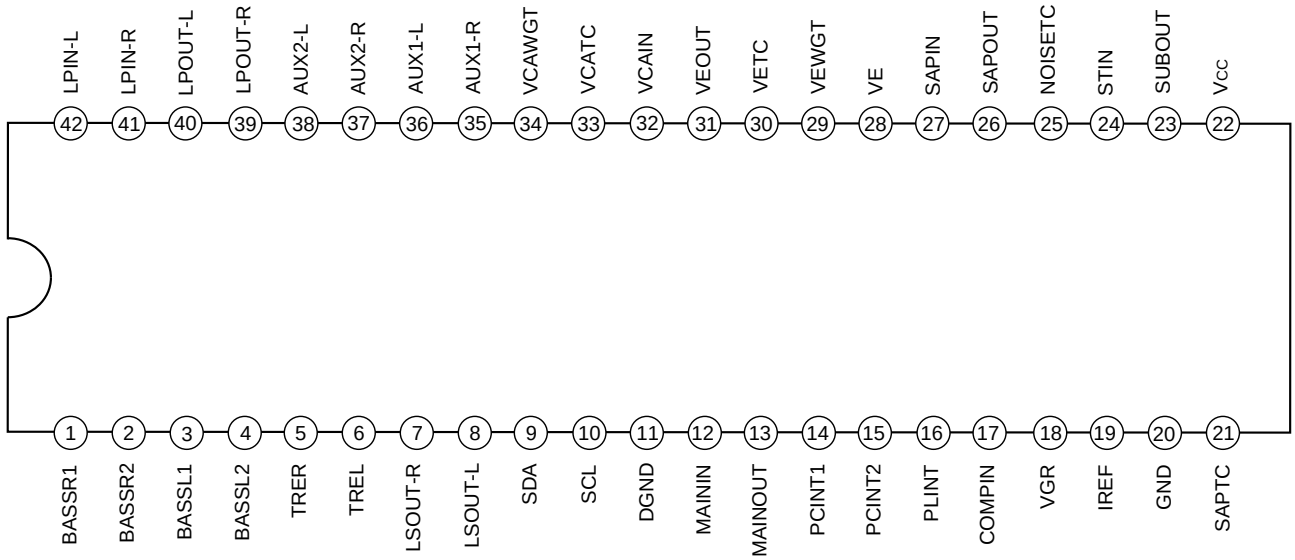
E96843A6Y-PS

Pin Configuration (Top View)

CXA2074Q

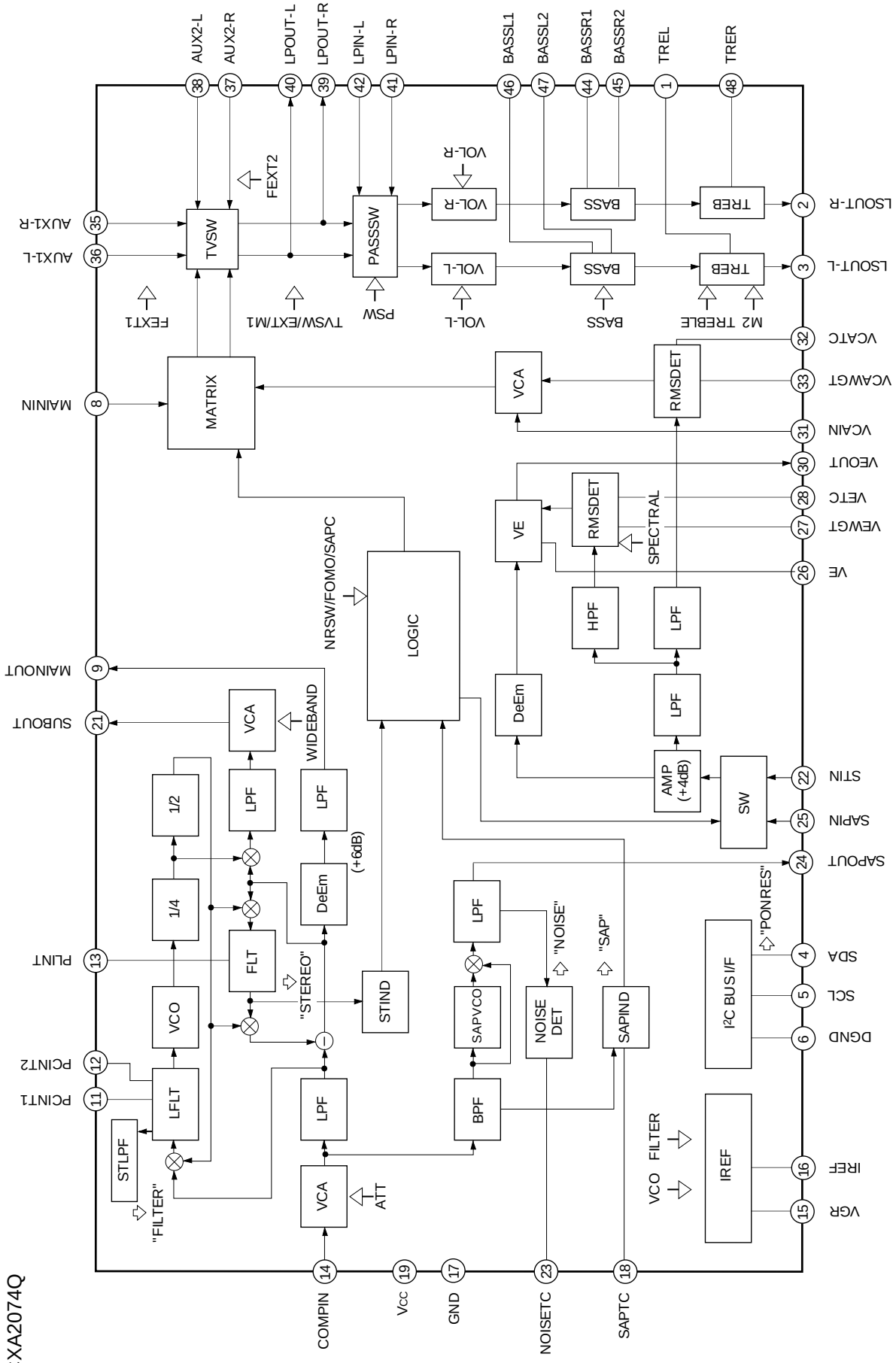


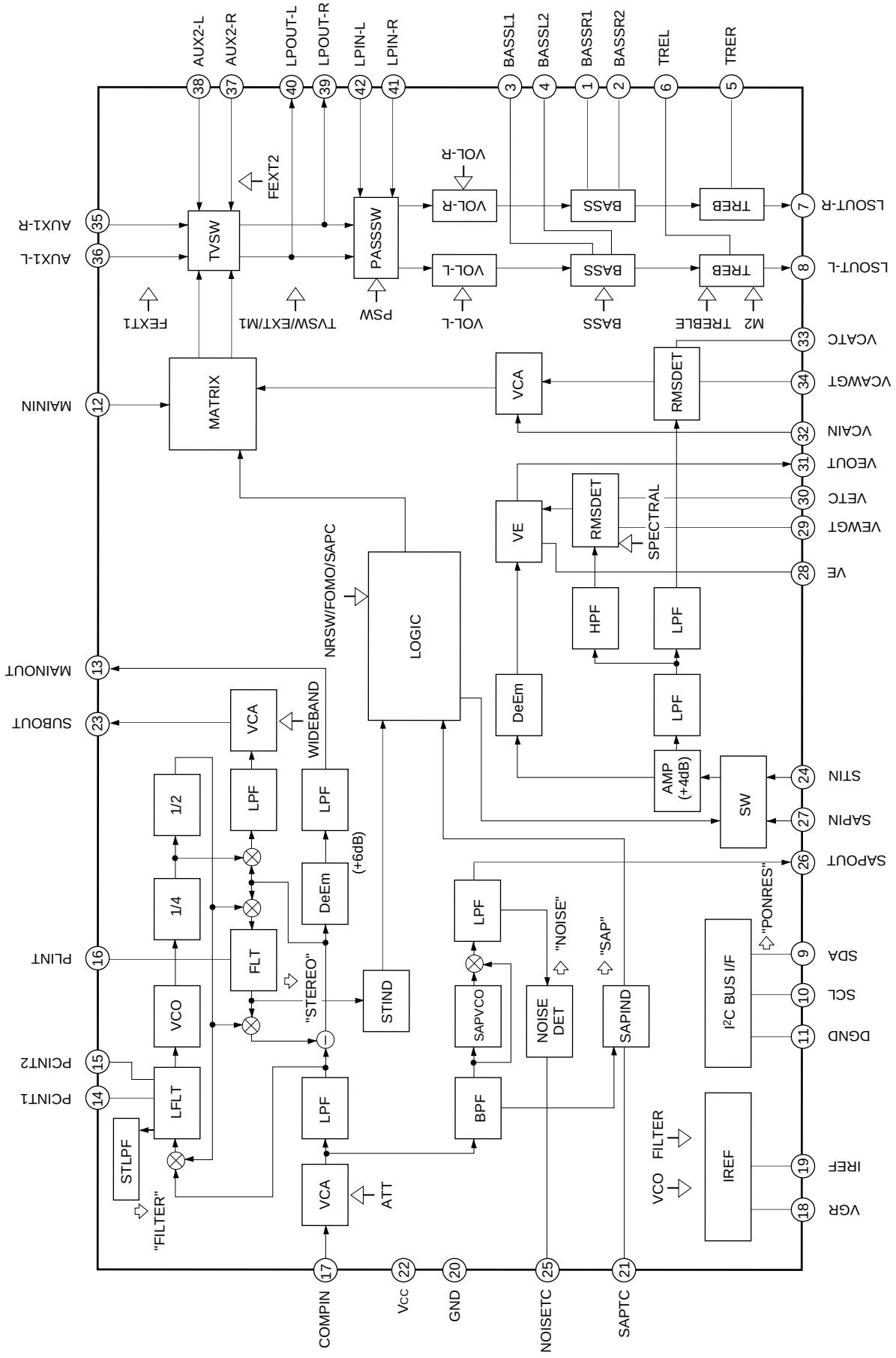
CXA2074S



Block Diagram

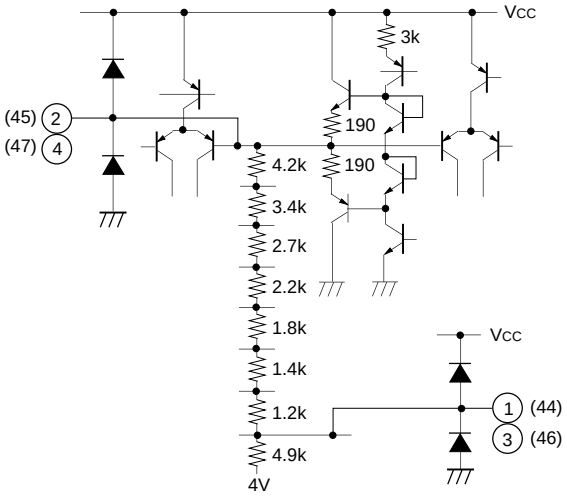
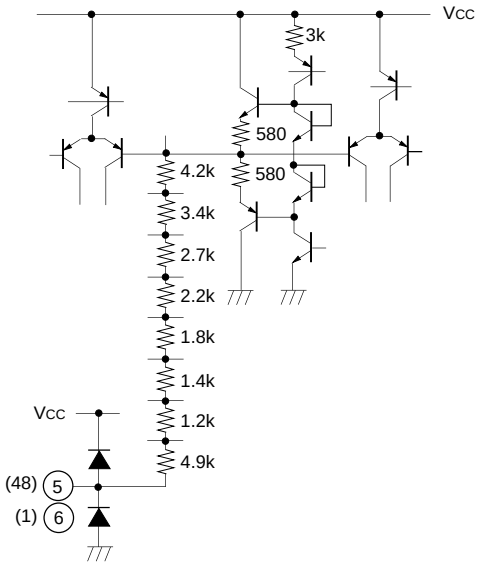
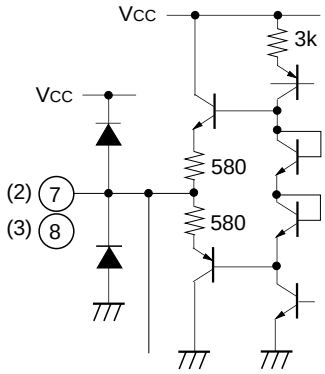
CXA2074Q

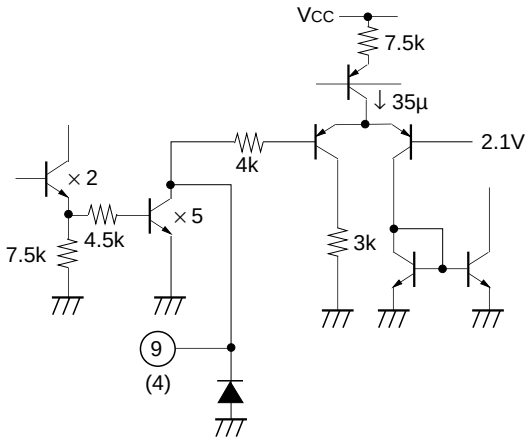
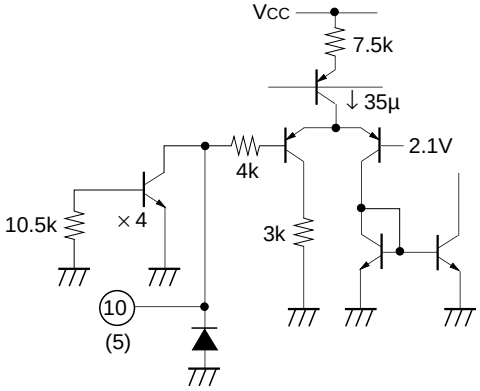
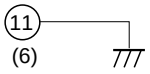
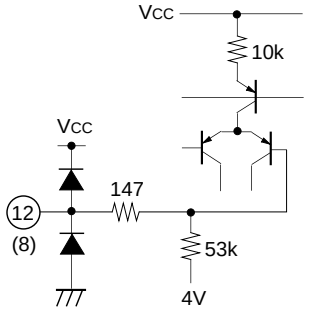
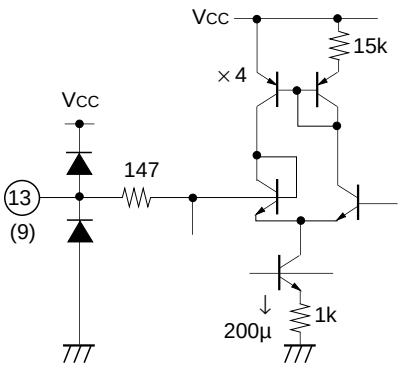


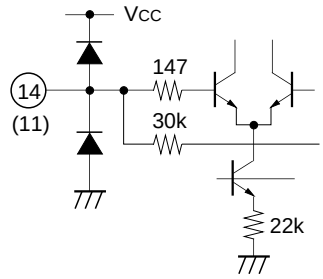
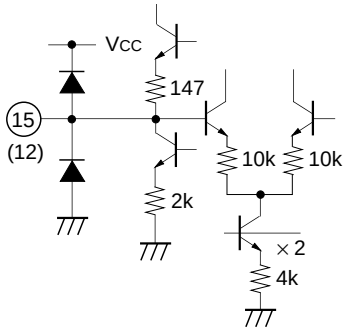
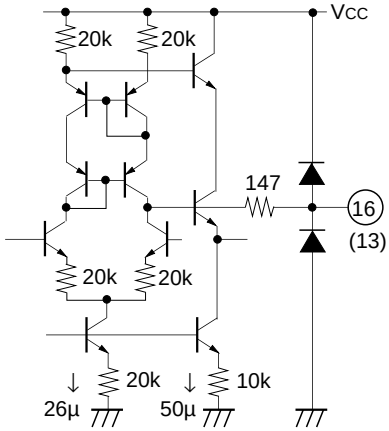
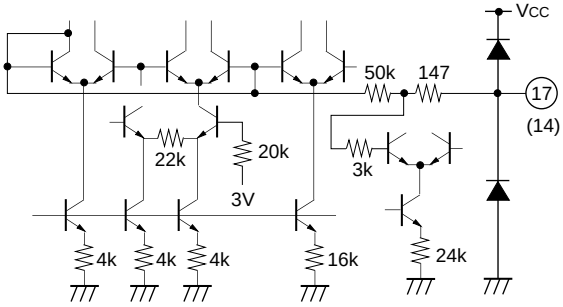

AUX2-L
AUX2-R
LPOUT-L
LPOUT-R
LPIN-L
LPIN-R
BASSL1
BASSL2
BASSR1
BASSR2
TREL
TRER
38
37
40
39
42
41
3
4
1
2
6
5
FEXT2
VOL-R
TVSW
PASSSW
VOL-R
BASS
TREB
LSOUT-R
7
AUX1-R
35
AUX1-L
36
LSOUT-L
8
FEXT1
TVSW/EXT/M1
PSW
VOL-L
BASS
TREBLE
M2
VCATC
33
MATRIX
VCA
RMSDET
VCAWGT
34
MAININ
12
VCAIN
32
VEOUT
31
VETC
30
VEWGT
29
VE
28
SPECTRAL
NRSW/FOMO/SAPC
LOGIC
HPF
LPF
MAINOUT
13
SUBOUT
23
WIDEBAND
DeEm
LPF
STIN
24
SAPIN
27
SAPOUT
26
1/2
1/4
(+6dB)
PLINT
16
FLT
"STEREO"
STIND
LPF
"NOISE"
"SAP"
"PONRES"
SDA
9
SCL
10
DGND
11
VCO
SAPVCO
NOISE DET
SAPIND
I2C BUS I/F
PCINT2
15
PCINT1
14
LFLT
BPF
STLPF
"FILTER"
ATT
FILTER
VCO
IREF
19
VGR
18
COMPIN
17
VCC
22
GND
20
NOISETC
25
SAPTC
21

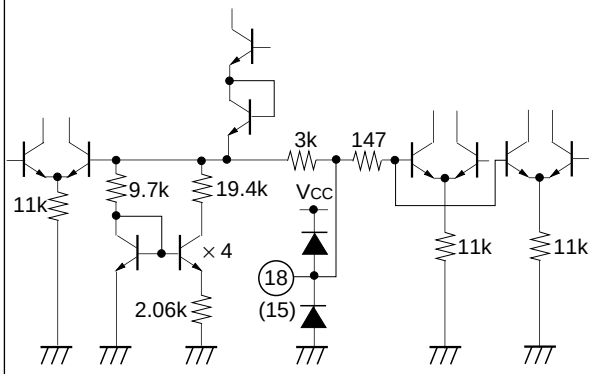
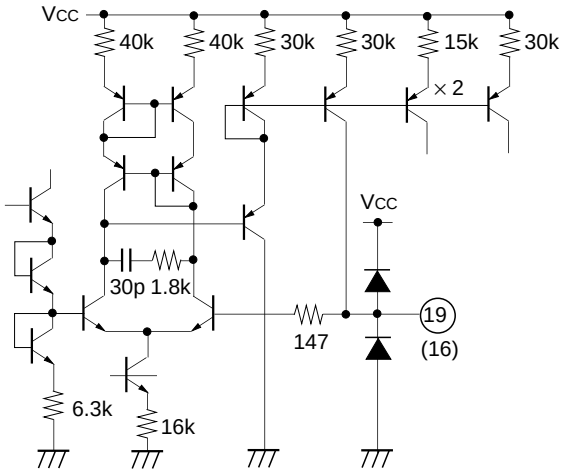
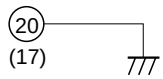
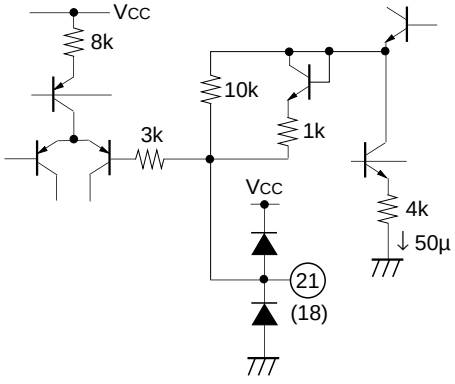
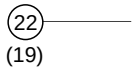
CXA2074S

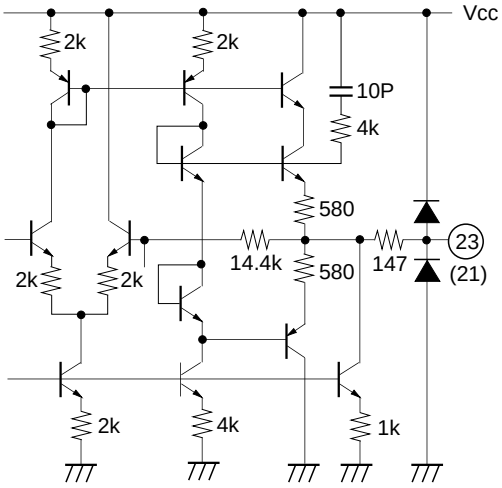
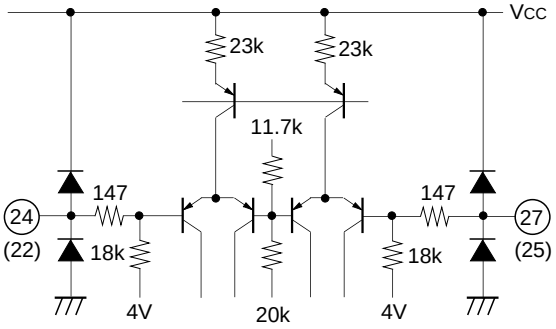
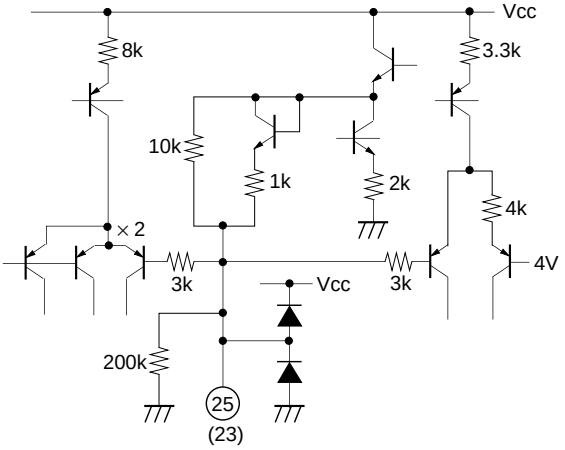
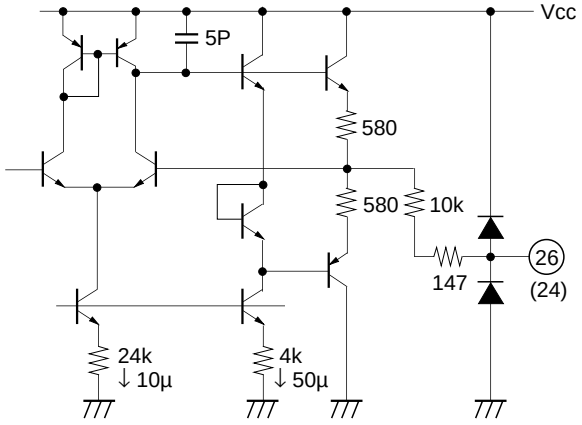
Pin Description

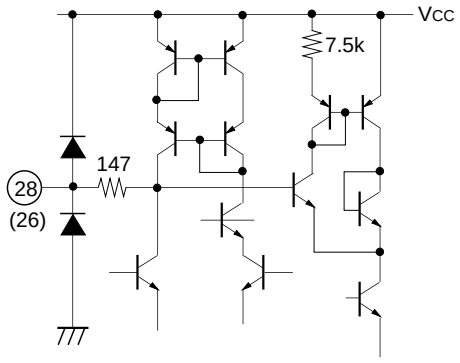
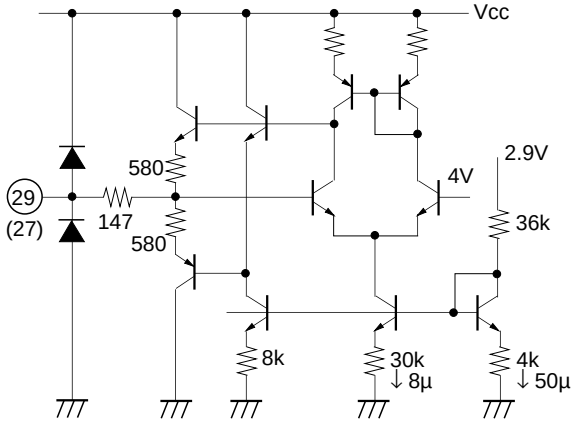
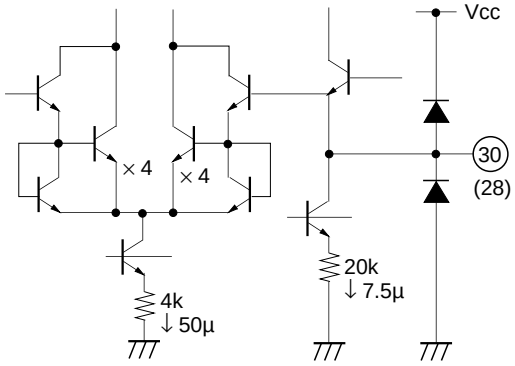
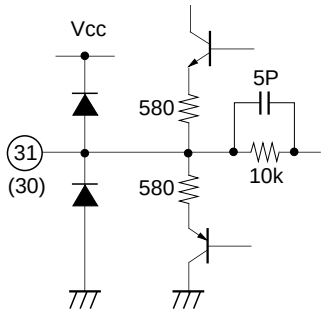
Pin No. QFP	Pin No. SDIP	Symbol	Pin voltage	Equivalent circuit	Description
44	1	BASSR1	4.0V		BASS filter pin. (Right channel) (Connect a 47nF capacitor between Pins 1 and 2 (44 and 45).) The cutoff frequency is determined by the built-in resistor and the external capacitance.
45	2	BASSR2	4.0V		
46	3	BASSL1	4.0V		BASS filter pin. (Left channel) (Connect a 47nF capacitor between Pins 3 and 4 (46 and 47).) The cutoff frequency is determined by the built-in resistor and the external capacitance.
47	4	BASSL2	4.0V		
48	5	TRER	4.0V		TREBLE filter pin. (Right channel) (Connect a 6.8nF capacitor between this pin and GND.)
1	6	TREL	4.0V		TREBLE filter pin. (Left channel) (Connect a 6.8nF capacitor between this pin and GND.)
2	7	LSOUT-R	4.0V		LSOUT right channel output pin.
3	8	LSOUT-L	4.0V		LSOUT left channel output pin.

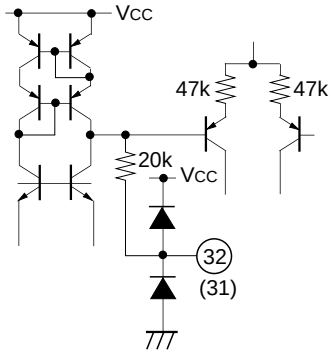
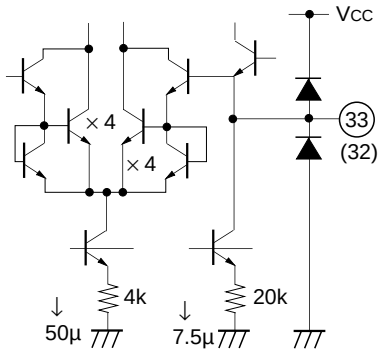
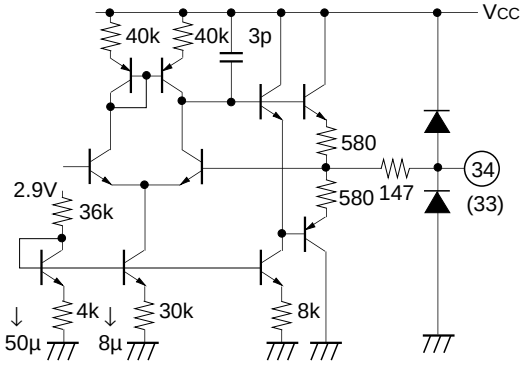
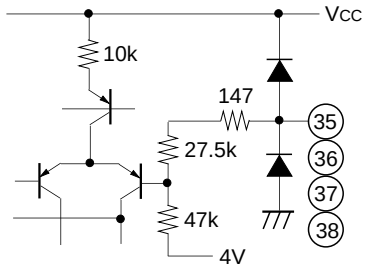
Pin No. QFP	Pin No. SDIP	Symbol	Pin voltage	Equivalent circuit	Description
4	9	SDA	—		Serial data I/O pin. V_{IH} > 0V V_{IL} < 1.5V
5	10	SCL	—		Serial clock input pin. V_{IH} > 3.0V V_{IL} < 1.5V
6	11	DGND	—		Digital block GND.
8	12	MAININ	4.0V		Input the (L + R) signal from MAINOUT (Pin 13 (9)).
9	13	MAINOUT	4.0V		(L + R) signal output pin.

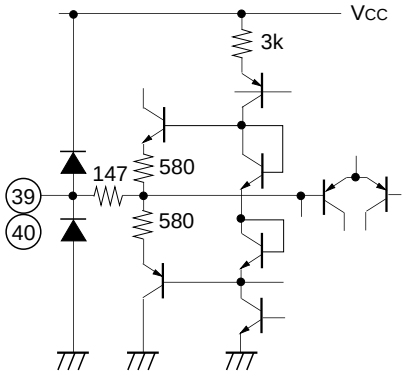
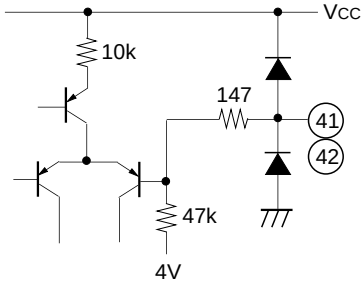
Pin No.		Symbol	Pin voltage	Equivalent circuit	Description
QFP	SDIP				
11	14	PCINT1	4.0V		Stereo block PLL loop filter integrating pin.
12	15	PCINT2	4.0V		
13	16	PLINT	5.1V		Pilot cancel circuit loop filter integrating pin. (Connect a 1µF capacitor between this pin and GND.)
14	17	COMPIN	4.0V		Audio multiplexing signal input pin.

Pin No. QFP	Pin No. SDIP	Symbol	Pin voltage	Equivalent circuit	Description
15	18	VGR	1.3V		Band gap reference output pin. (Connect a 10µF capacitor between this pin and GND.)
16	19	IREF	1.3V		Set the filter and VCO reference current. The reference current is adjusted with the BUS DATA based on the current which flows to this pin. (Connect a 62kΩ (±1%) resistor between this pin and GND.)
17	20	GND	—		Analog block GND.
18	21	SAPTC	4.5V		Set the time constant for the SAP carrier detection circuit. (Connect a 4.7µF capacitor between this pin and GND.)
19	22	Vcc	—		Supply voltage pin.

Pin No. QFP	Pin No. SDIP	Symbol	Pin voltage	Equivalent circuit	Description
21	23	SUBOUT	4.0V		(L – R) signal output pin.
22	24	STIN	4.0V		Input the (L – R) signal from SUBOUT (Pin 23 (21)).
25	27	SAPIN	4.0V		Input the (SAP) signal from SAPOUT (Pin 26 (24)).
23	25	NOISETC	3.0V		Set the time constant for the noise detection circuit. (Connect a 4.7µF capacitor between this pin and GND.)
24	26	SAPOUT	4.0V		SAP FM detector output pin.

Pin No. QFP	Pin No. SDIP	Symbol	Pin voltage	Equivalent circuit	Description
26	28	VE	4.0V		Variable de-emphasis integrating pin. (Connect a 2700pF capacitor and a 3.3kΩ resistor in series between this pin and GND.)
27	29	VEWGT	4.0V		Weight the variable de-emphasis control effective value detection circuit. (Connect a 0.047µF capacitor and a 3kΩ resistor in series between this pin and GND.)
28	30	VETC	1.7V		Determine the restoration time constant of the variable de-emphasis control effective value detection circuit. (The specified restoration time constant can be obtained by connecting a 3.3µF capacitor between this pin and GND.)
30	31	VEOUT	4.0V		Variable de-emphasis output pin. (Connect a 4.7µF non-polar capacitor between Pins 31 (30) and 32 (31).)

Pin No. QFP	Pin No. SDIP	Symbol	Pin voltage	Equivalent circuit	Description
31	32	VCAIN	4.0V		VCA input pin. Input the variable de-emphasis output signal from Pin 31 (30) via a coupling capacitor.
32	33	VCATC	1.7V		Determine the restoration time constant of the VCA control effective value detection circuit. (The specified restoration time constant can be obtained by connecting a 10µF capacitor between this pin and GND.)
33	34	VCAWGT	4.0V		Weight the VCA control effective value detection circuit. (Connect a 1µF capacitor and a 3.9kΩ resistor in series between this pin and GND.)
35	35	AUX1-R	4.0V		Right channel external input 1 pin.
36	36	AUX1-L	4.0V		Left channel external input 1 pin.
37	37	AUX2-R	4.0V		Right channel external input 2 pin.
38	38	AUX2-L	4.0V		Left channel external input 2 pin.

Pin No.		Symbol	Pin voltage	Equivalent circuit	Description
QFP	SDIP				
39	39	LPOUT-R	4.0V		LPOUT right channel output pin.
40	40	LPOUT-L	4.0V		LPOUT left channel output pin.
41	41	LPIN-R	4.0V		Right channel loop input pin.
42	42	LPIN-L	4.0V		Left channel loop input pin.
7	—	NC	—	(7)	
10	—	NC	—	(10)	
20	—	NC	—	(20)	
29	—	NC	—	(29)	
34	—	NC	—	(34)	
43	—	NC	—	(43)	

Electrical Characteristics

COMPIN input level
(100% modulation level)

Main (L + R) (Pre-Emphasis: OFF) = 245mVrms
SUB (L – R) (dbx-TV: OFF) = 490mVrms
Pilot = 49mVrms
SAP Carrier = 147mVrms
f_H = 15.734kHz

The pin numbers in parenthesis are for the CXA2074Q.

(Ta = 25°C, V_{CC} = 9V)

No.	Item	Signal	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
1	Current consumption	Icc		17 (14)	No signal				30	40	50	mA
2	Main output level	Vmain	MONO	17 (14)	Mono 1kHz 100% mod. Pre-em. ON			39/40	440	490	540	mVrms
3	Main de-emphasis frequency characteristic	FCdeem	MONO	17 (14)	Mono 5kHz 30% mod. Pre-em. ON	20 log ('5k'/'1k')		39/40	–1.2	0	1.0	dB
4	Main LPF frequency characteristic	FCmain	MONO	17 (14)	Mono 12kHz 30% mod. Pre-em. ON	20 log ('12k'/'1k')		39/40	–3.0	–1.0	1.0	dB
5	Main distortion	THDm	MONO	17 (14)	Mono 1kHz 100% mod. Pre-em. ON		15kLPF	39/40	–	0.1	0.5	%
6	Main overload distortion	THDmmax	MONO	17 (14)	Mono 1kHz 200% mod. Pre-em. OFF		15kLPF	39/40	–	0.15	0.5	%
7	Main S/N	SNmain	MONO	17 (14)	Mono 1kHz, Pre-em. ON	20 log ('100%'/'0%')	15kLPF	39/40	61	69	–	dB
8	Sub output level	Vsub	ST	17 (14)	SUB (L-R), 1kHz, 100% mod., NR OFF			23 (21)	150	190	230	mVrms
9	Sub LPF frequency characteristic	FCsub	ST	17 (14)	SUB (L-R) 12kHz, 30% mod., NR OFF	20 log ('12k'/'1k')		23 (21)	–3.0	–0.5	1.0	dB
10	Sub distortion	THDsub	ST	17 (14)	SUB (L-R) 1kHz, 100% mod., NR OFF		15kLPF	23 (21)	–	0.1	1.0	%
11	Sub overload distortion	THDsmax	ST	17 (14)	SUB (L-R), 1kHz, 200% mod., NR OFF		15kLPF	23 (21)	–	0.2	2.0	%
12	Sub S/N	SNsub	ST	17 (14)	SUB (L-R) 1kHz, NR OFF	20 log ('100%'/'0%')	15kLPF	23 (21)	56	64	–	dB
13	ST → SAP Crosstalk	CTst	SAP	17 (14)	SUB (L-R), 1kHz, 100% mod., NR ON, SAP Carrier (5f_H)	20 log ('NRSW = 0'/ 'NRSW = 1')	1kBPF	40	60	70	–	dB
14	Sub pilot leak	PCsub	ST	17 (14)	PILOT (f_H) 0dB	0dB = 49mVrms	f_H BPF	23 (21)	–	–35	–27	dB
15	Stereo ON level	THst	ST	17 (14)	Change PILOT (f_H) Level	0dB = 49mVrms		BUS RETURN	–9.0	–6.0	–3.0	dB
16	Stereo ON/OFF hysteresis	HYst				20 log ('on level'/'off level')			3.5	6.0	8.5	dB

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
17	SAP output level	Vsap	SAP	17 (14)	SAP 1kHz 100% mod. NR OFF			26 (24)	150	190	230	mVrms
18	SAP LPF frequency characteristic	FCsap	SAP	17 (14)	SAP 10kHz, 30% mod. NR OFF	20 log ('10k'/'1k')		26 (24)	–3.0	0	2.5	dB
19	SAP distortion	THDsap	SAP	17 (14)	SAP 1kHz 100% mod. NR OFF		15kLPF	26 (24)	–	2.5	6.0	%
20	SAP S/N	SNsap	SAP	17 (14)	SAP 1kHz, NR OFF	20 log ('100%'/'0%')	15kLPF	26 (24)	46	55	–	dB
21	SAP → ST Cross talk	CTsap	ST	17 (14)	SAP 1kHz 100% mod. NR ON, Pilot (f_H)	20 log ('NRSW = 1'/'NRSW = 0')	1kBPF	40	60	70	–	dB
22	SAP ON level	THsap	SAP	17 (14)	Change SAP Carrier ($5f_H$) Level	0dB = 147mVrms		BUS RETURN	–12.0	–9.0	–6.5	dB
23	SAP ON/OFF hysteresis	HYsap				20 log ('on level'/'off level')			2.0	4.0	6.0	dB
24	ST separation 1 L → R	STLsep1	ST	17 (14)	ST-L 300Hz 30% mod. NR ON		15kLPF	39/40	23	35	–	dB
25	ST separation 1 R → L	STRsep1	ST	17 (14)	ST-R 300Hz 30% mod. NR ON		15kLPF	39/40	23	35	–	dB
26	ST separation 2 L → R	STLsep2	ST	17 (14)	ST-L 3kHz 30% mod. NR ON		15kLPF	39/40	23	35	–	dB
27	ST separation 2 R → L	STRsep2	ST	17 (14)	ST-R 3kHz 30% mod. NR ON		15kLPF	39/40	23	35	–	dB
28	LPOUT output level	Vtp	EXT	35/36 37/38	Sine wave 1kHz, 490mVrms	0dB = 490mVrms		39/40	–0.5	0	0.5	dB
29	LPOUT muted amount	MUlp1	INT	17 (14)	MONO 1kHz, 100%, Pre-em. on	20 log (M1 = "0"/M1 = "1")	1kBPF	39/40	–	–85	–70	dB
30		MUlp2	EXT	35/36 37/38	Sine wave 1kHz, 490mVrms	20 log (M1 = "0"/M1 = "1")			–	–90	–75	dB
31	LSOUT output level	Vls	INT	17 (14)	MONO 1kHz 100%, Pre-em. on	0dB = 490mVrms		7/8 (2/3)	–0.9	0	0.9	dB
			EXT	35/36 37/38	Sine wave 1kHz, 490mVrms	0dB = 490mVrms						
32	LSOUT cross talk	CTls	INT	35/36 37/38	Sine wave 1kHz, 490mVrms	0dB = 490mVrms EXT → INT	1kBPF	7/8 (2/3)	–	–75	–60	dB
			EXT	17 (14)	MONO 1kHz 100%, Pre-em. on	0dB=490mVrms INT → EXT	1kBPF	7/8 (2/3)	–	–90	–80	dB
33	LSOUT muted amount	MUls	EXT	35/36 37/38	Sine wave 1kHz, 490mVrms	20 log (M2 = "0"/M2 = "1")	1kBPF	7/8 (2/3)	–	–90	–75	dB

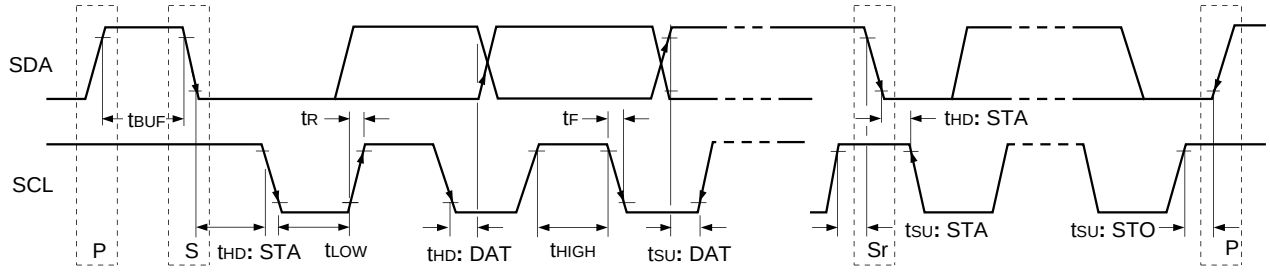
No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
34	LSOUT DC offset	OSls	INT EXT	—	No signal	Mute (M2 = 0)/ DC difference when there is no signal		7/8 (2/3)	–25	0	25	mV
35	LSOUT distortion	THDls	EXT	35/36 37/38	Sine wave 1kHz, 490mVrms		15kLPF	7/8 (2/3)	–	0.01	0.5	%
36	LSOUT S/N	SNls	EXT	35/36 37/38	Sine wave 1kHz, 490mVrms	20 log ('490mVrms'/ 'No signal')	15kLPF	7/8 (2/3)	75	88	–	dB
37	LSOUT overload distortion	THDlsmax	EXT	35/36 37/38	Sine wave 1kHz, 2Vrms		15kLPF	7/8 (2/3)	–	0.1	1.0	%
38	BASS maximum value	TBmax	EXT	35/36 37/38	Sine wave 100Hz, 245mVrms	BASS = "F" 0dB = 245mVrms		7/8 (2/3)	11	12	13	dB
39	BASS minimum value	TBmin	EXT	35/36 37/38	Sine wave 100Hz, 245mVrms	BASS = "0" 0dB = 245mVrms		7/8 (2/3)	–13	–12	–11	dB
40	TREBLE maximum value	TTmax	EXT	35/36 37/38	Sine wave 10kHz, 245mVrms	TREBLE = "F" 0dB = 245mVrms		7/8 (2/3)	11	12	13	dB
41	TREBLE minimum value	TTmin	EXT	35/36 37/38	Sine wave 10kHz, 245mVrms	TREBLE = "0" 0dB = 245mVrms		7/8 (2/3)	–13	–12	–11	dB
42	Volume minimum value	VOLmin	EXT	35/36 37/38	Sine wave 1kHz, 490mVrms	VOL-L = "0", VOL-R = "0" 0dB = 490mVrms	1kBPF	7/8 (2/3)	–	–90	–75	dB

I²C BUS block items (SDA, SCL)

No.	Item	Symbol	Min.	Typ.	Max.	Unit
1	High level input voltage	V_{IH}	3.0	—	5.0	V
2	Low level input voltage	V_{IL}	0	—	1.5	
3	High level input current	I_{IH}	—	—	10	µA
4	Low level input current	I_{IL}	—	—	10	
5	Low level output voltage SDA (Pin 9) during 3mA inflow	V_{OL}	0	—	0.4	V
6	Maximum inflow current	I_{OL}	3	—	—	mA
7	Input capacitance	C_I	—	—	10	pF
8	Maximum clock frequency	f_{SCL}	0	—	100	kHz
9	Minimum waiting time for data change	t_{BUF}	4.7	—	—	µs
10	Minimum waiting time for start of data transfer	t_{HD}: STA	4.0	—	—	
11	Low level clock pulse width	t_{LOW}	4.7	—	—	
12	High level clock pulse width	t_{HIGH}	4.0	—	—	
13	Minimum waiting time for start preparation	t_{SU}: STA	4.7	—	—	
14	Minimum data hold time	t_{HD}: DAT	0	—	—	
15	Minimum data preparation time	t_{SU}: DAT	250	—	—	ns
16	Rise time	t_R	—	—	1	µs
17	Fall time	t_F	—	—	300	ns
18	Minimum waiting time for stop preparation	t_{SU}: STO	4.7	—	—	µs

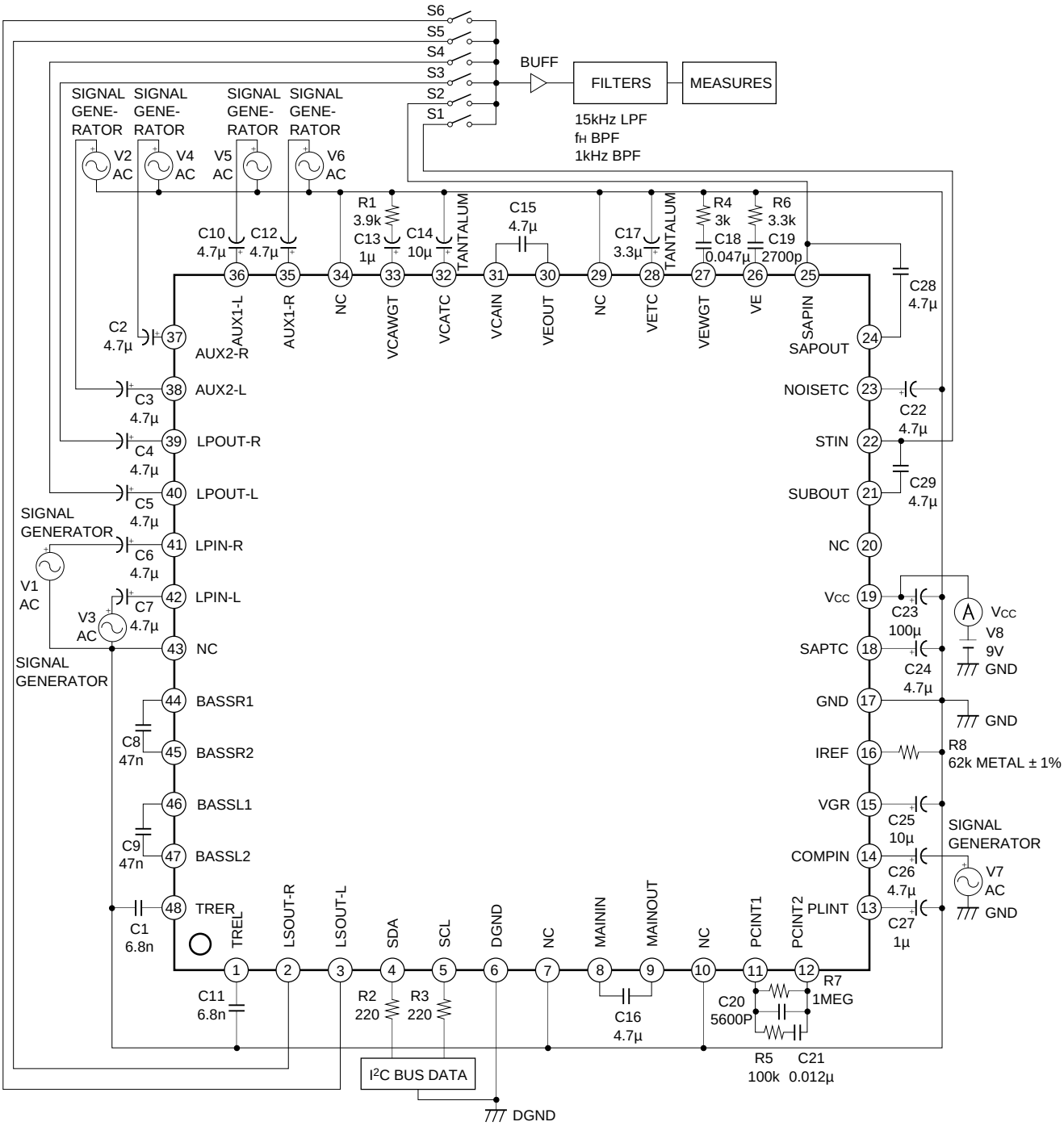
I²C BUS load conditions: Pull-up resistor 4kΩ (Connect to +5V)
Load capacity 200pF (Connect to GND)

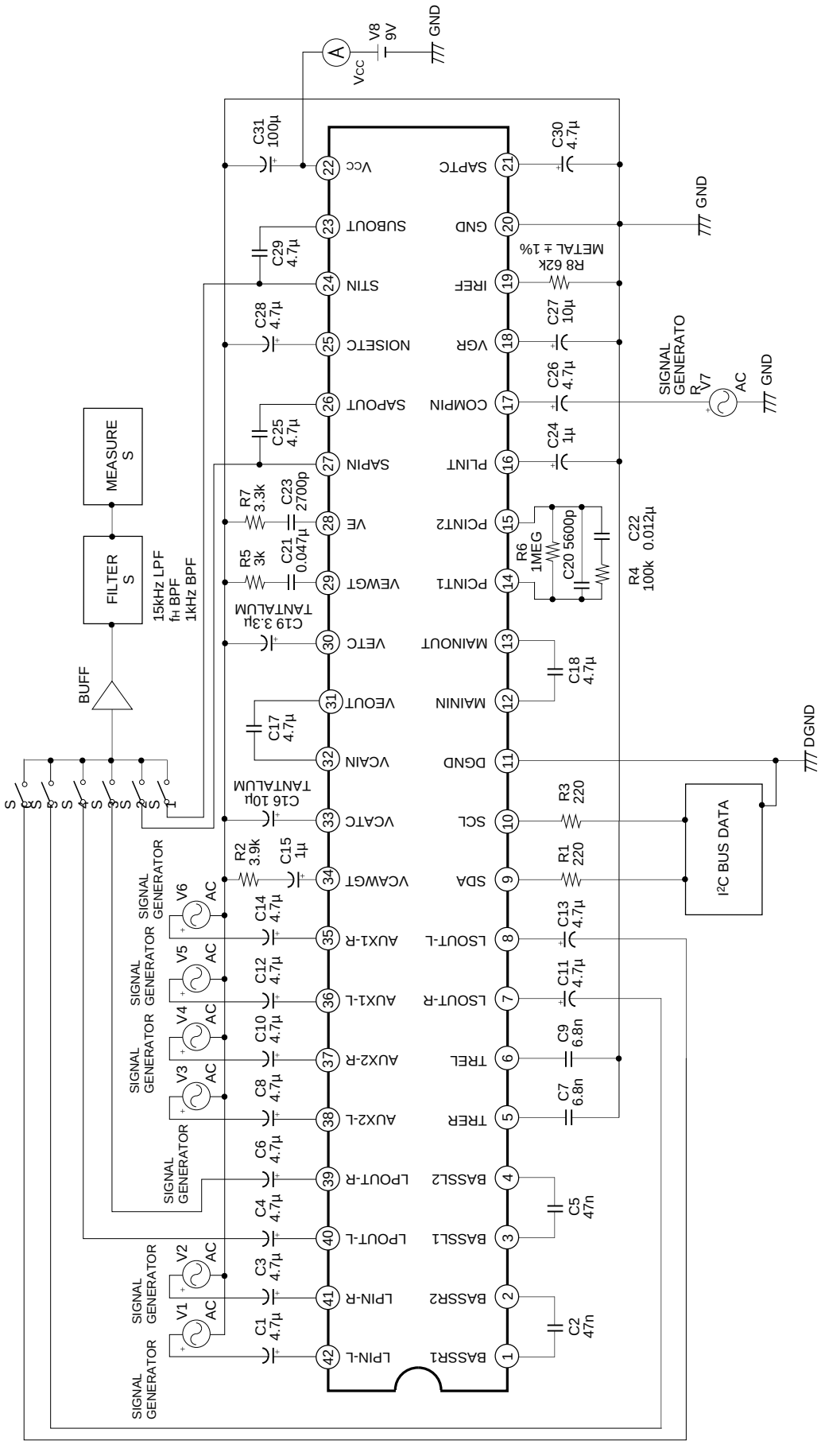
I²C BUS Control Signal



Electrical Characteristics Measurement Circuit

CXA2074Q




CXA2074S
SIGNAL GENERATOR
V1 AC
V2 AC
V3 AC
V4 AC
V5 AC
V6 AC
V7 AC
V8 9V
GND
DGND
BUFF
FILTER S
MEASURE S
15kHz LPF
fH BPF
1kHz BPF
I2C BUS DATA
SCL
SDA
R1 220
R2 3.9k
R3 220
R4 100k
R5 3k
R6 1MEG
R7 3.3k
R8 62k METAL ± 1%
C1 4.7µ
C2 47n
C3 4.7µ
C4 4.7µ
C5 47n
C6 4.7µ
C7 6.8n
C8 4.7µ
C9 6.8n
C10 4.7µ
C11 4.7µ
C12 4.7µ
C13 4.7µ
C14 4.7µ
C15 1µ
C16 10µ TANTALUM
C17 4.7µ
C18 4.7µ
C19 3.3µ TANTALUM
C20 5600p
C21 0.047µ
C22 0.012µ
C23 2700p
C24 1µ
C25 4.7µ
C26 4.7µ
C27 10µ
C28 4.7µ
C29 4.7µ
C30 4.7µ
C31 100µ
1 BASSR1
2 BASSR2
3 BASSL1
4 BASSL2
5 TREB
6 TREL
7 LSOUT-R
8 LSOUT-L
9 SDA
10 SCL
11 DGND
12 MAININ
13 MAINOUT
14 PCINT1
15 PCINT2
16 PLINT
17 COMPIN
18 VGR
19 IREF
20 GND
21 SAPTC
22 VCC
23 SUBOUT
24 STIN
25 NOISETC
26 SAPOUT
27 SAPIN
28 VE
29 VEWGT
30 VETC
31 VEOUT
32 VCAIN
33 VCATC
34 VCAWGT
35 AUX1-R
36 AUX1-L
37 AUX2-R
38 AUX2-L
39 LPOUT-R
40 LPOUT-L
41 LPIN-R
42 LPIN-L

I²C BUS Register Data Standard Setting Values

Register	Number of bits	Classification	Standard setting	Contents	Setting value when electrical characteristics are measured
ATT	4	A	9	Center point	Adjustment point
VCO	6	A	1F		
FILTER	6	A	1F		
SPECTRAL	6	A	1F		
WIDEBAND	6	A	1F		
TEST-DA	1	T	0	Normal mode	Standard setting value
TEST1	1	T	0		
FST	1	T	0	Normal mode	FST = 0
VOL-L	6	U	3F	3F = 0dB	
VOL-R	6	U	3F	3F = 0dB	
BASS	4	U	8	7 or 8 = 0dB	
TREBLE	4	U	8	7 or 8 = 0dB	
NRSW	1	U	—	According to the mode control table	
FOMO	1	U	—		
TVSW	1	U	0	TV decoder output selection	Standard setting value
EXT	1	U	0		
FEXT1	1	U	0	External input 1 forced MONO	Standard setting value
FEXT2	1	U	0	External input 2 forced MONO	Standard setting value
PSW	1	U	0	TVSW output selection	Standard setting value
M1	1	U	1	Mute OFF	
M2	1	U	1		
ATTSW	1	S	—	Fixed by the set specifications	
SAPC	1	S	—		

Classification A: Adjustment
U: User control
S: Proper to set
T: Test

List of Adjustment Contents

The pin numbers in parenthesis are for the CXA2074Q.

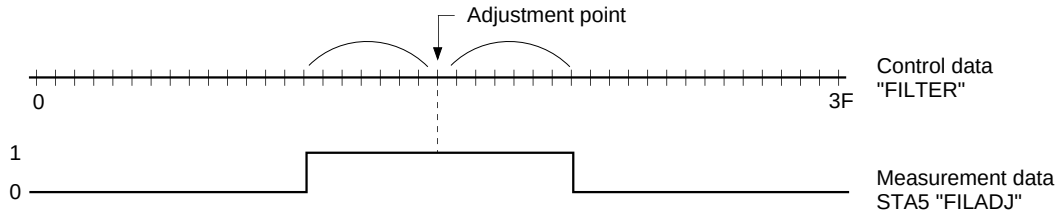
	Adjustment item	Adjustment data	Input pin	Input signal data	Measurement	Adjustment contents	Test mode setting
1	MAIN VCA	ATT	COMPIN Pin 17 (Pin 14)	100Hz 245mVrms	LPOUT-L output level	Adjust as close to 490mVrms as possible	
2	ST & SAP VCO	VCO	None	None	LPOUT-R output frequency	Adjust as close to 62.936kHz as possible	TEST-DA = 1
3	ST & SAP & dbx FILTER	FILTER	COMPIN Pin 17 (Pin 14)	9.4kHz 600mVrms	STA5 (FILADJ)	Adjust to the center of the FILADJ = 1 condition	TEST1 = 1
4	Low frequency ST separation	WIDEBAND	COMPIN Pin 17 (Pin 14)	ST-L 30% 300Hz	LPOUT-R output level	Minimize the output level	
	High frequency ST separation	SPECTRAL	COMPIN Pin 17 (Pin 14)	ST-L 30% 3kHz	LPOUT-R output level	Minimize the output level	

Adjustment Method

1. ATT adjustment
   1) TEST BIT is set to “TEST1 = 0” and “TEST-DA = 0”.
   2) Input a 100Hz, 245mVrms sine wave signal to COMPIN and monitor the LPOUT-L output level. Then, adjust the “ATT” data for ATT adjustment so that the LPOUT-L output goes to the standard value.
   3) Adjustment range: ±30%
      Adjustment bits: 4 bits

2. Stereo, SAPVCO adjustment
   1) TEST BIT is set to “TEST1 = 0” and “TEST-DA = 1”.
   2) Monitor the LPOUT-R output ($4f_H$ free running) frequency in a no input state, and adjust “VCO” adjustment data so that this frequency is as close to $4f_H$ (62.936kHz) as possible.
   3) Adjustment range: ±20%
      Adjustment bits: 6 bits

3. Stereo, SAP block, dbx filter adjustment
   1) TEST BIT is set to “TEST1 = 1” and “TEST-DA = 0”.
   2) Input a 9.4kHz, 600mVrms sine wave signal to COMPIN. While monitoring the STATUS FLAG (STA5) condition, adjust the “FILTER” adjustment data.
   3) Adjustment range: ±20%
      Adjustment bits: 6 bits
      Align “FILTER” with the center of the STA5 = 1 (adjustment OK) condition range.



4. Separation adjustment
   1) TEST BIT is set to “TEST1 = 0” and “TEST-DA = 0”.
   2) Set the unit to stereo mode and input the left channel only signal (modulation factor 30%, frequency 300Hz NR-ON) to COMPIN. At this time, adjust the “WIDEBAND” adjustment data to reduce LPOUT-R output to the minimum.
   3) Next, set the frequency only of the input signal to 3kHz and adjust the “SPECTRAL” adjustment data to reduce LPOUT-R output to the minimum.
   4) The adjustments in 2 and 3 above are performed to optimize the separation.
   5) “WIDEBAND” “SPECTRAL”
      Adjustment range: ±30% Adjustment range: ±15%
      Adjustment bits: 6 bits Adjustment bits: 6 bits

Description of Operation [The pin numbers in parenthesis are for the CXA2074Q.]

The US audio multiplexing system possesses the base band spectrum shown in Fig. 1.

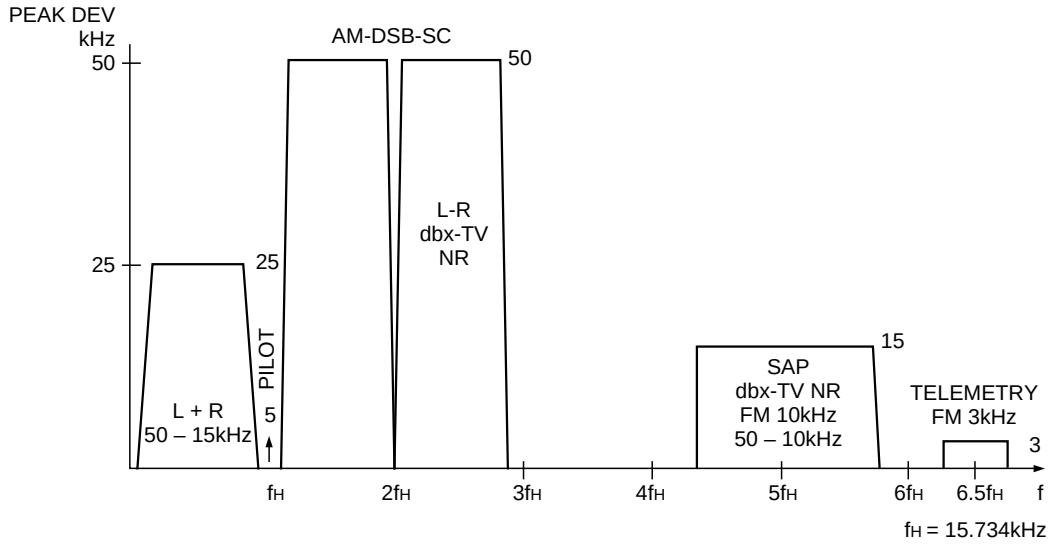


Fig. 1. Base band spectrum

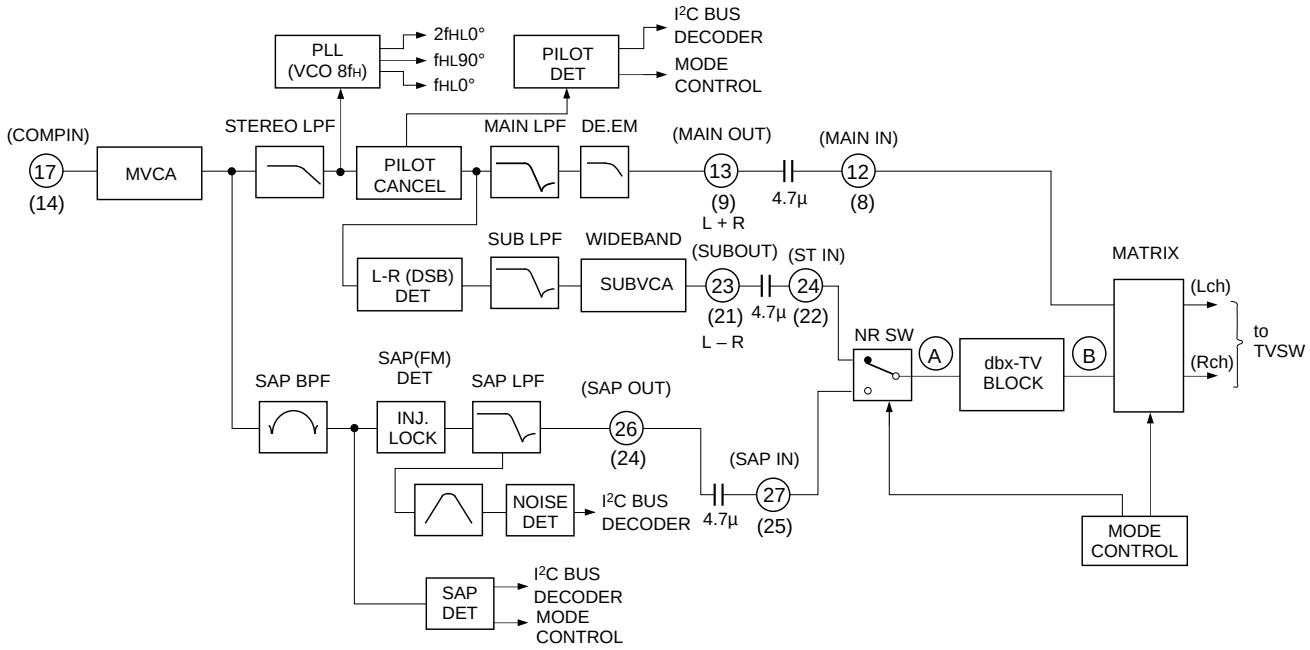


Fig. 2. Overall block diagram (See Fig. 3 for the dbx-TV block)

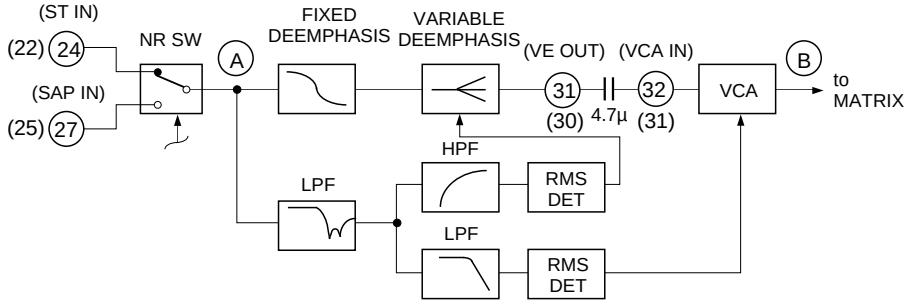


Fig 3. dbx-TV block

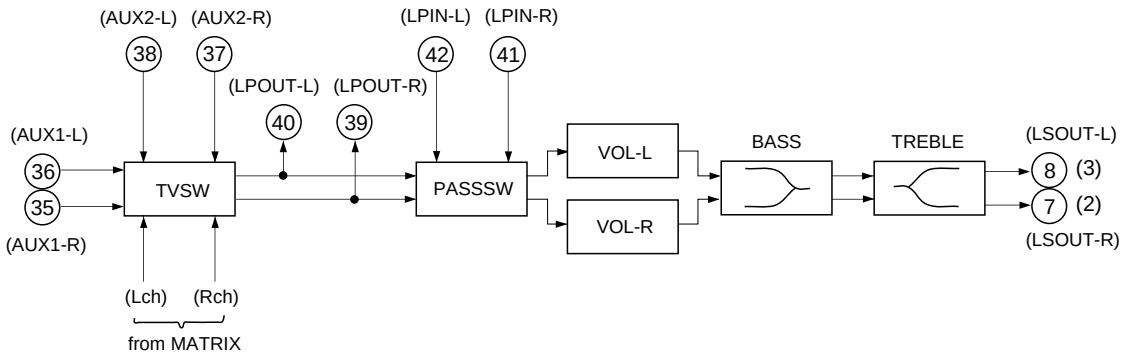


Fig. 4. Sound processor block

(1) L + R (MAIN)

After the audio multiplexing signal input from COMPIN (Pin 17 (Pin 14)) passes through MVCA, the SAP signal and telemetry signal are suppressed by STEREO LPF. Next, the pilot signals are canceled. Finally, the L – R signal and SAP signal are removed by MAIN LPF, and frequency characteristics are flattened (de-emphasized) and input to the matrix.

(2) L – R (SUB)

The L – R signal follows the same course as L + R before the pilot signal is canceled. L – R has no carrier signal, as it is a suppressed-carrier double-sideband amplitude modulated signal (DSB-AM modulated). For this reason, the pilot signal is used to regenerate the carrier signal (quasi-sine wave) to be used for the demodulation of the L – R signal. In the last stage, the residual high frequency components are removed by SUB LPF and the L – R signal is input to the dbx-TV block via the NRSW circuit after passing through SUBVCA.

(3) SAP

SAP is an FM signal using $5f_H$ as a carrier as shown in the Fig. 1. First, the SAP signal only is extracted using SAP BPF. Then, this is subjected to FM detection. Finally, residual high frequency components are removed and frequency characteristics flattened using SAP LPF, and the SAP signal is input to the dbx-TV block via the NRSW circuit. When there is no SAP signal, the Pin 26 output is soft muted.

(4) Mode discrimination

Stereo discrimination is performed by detecting the pilot signal amplitude. SAP discrimination is performed by detecting the $5f_H$ carrier amplitude. NOISE discrimination is performed by detecting the noise near 25kHz after FM detection of SAP signal.

(5) dbx-TV block

Either the L – R signal or SAP signal input respectively from ST IN (Pin 24 (Pin 22)) or SAP IN (Pin 27 (Pin 25)) is selected by the mode control and input to the dbx-TV block.

The input signal then passes through the fixed de-emphasis circuit and is applied to the variable de-emphasis circuit. The signal output from the variable de-emphasis circuit passes through an external capacitor and is applied to VCA (voltage control amplifier). Finally, the VCA output is converted from a current to a voltage using an operational amplifier and then input to the matrix.

The variable de-emphasis circuit transmittance and VCA gain are respectively controlled by Each of effective value detection circuits. Each of the effective value detection circuits passes the input signal through a predetermined filter for weighting before the effective value of the weighted signal is detected to provide the control signal.

(6) Matrix, TVSW, PASSSW

The signals (L + R, L – R, SAP) input to "MATRIX" become the outputs for the ST-L, ST-R, MONO and SAP signals according to the BUS data and whether there is ST / SAP discrimination.

"TVSW" switches the "MATRIX" output signal, external input signal (input to AUX1-L, R), external input signal (input to AUX2-L, R) and external forced MONO.

"PASSSW" switches the "TVSW" output signal and external input signal (input to LPIN-L, R).

(7) Sound processor block

The sound processor block contains, "BASS/TREBLE" tone control functions, and "VOLUME".

BASS: ±12dB (±1.7dB/STEP at 100Hz)
TREBLE: ±12dB (±1.7dB/STEP at 10kHz)
VOLUME: 0 to –80dB (–1.25dB/STEP)

(8) Others

"MVCA" is a VCA which adjusts the input signal level to the standard level of this IC.

"Bias" supplies the reference voltage and reference current to the other blocks. The current flowing to the resistor connecting IREF (Pin 19 (Pin 16)) with GND become the reference current.

Standard input and output levels

Input pin	Pin No.	Input level	LPOUT output level	LSOUT output level*3
COMPIN	17 (14)	245mVrms*1	490mVrms*2	490mVrms*2
AUX1-L/AUX1-R	36/35	490mVrms	490mVrms	490mVrms
AUX2-L/AUX2-R	38/37	490mVrms	490mVrms	490mVrms
LPIN-L/LPIN-R	42/41	490mVrms	—	490mVrms

*1 MONO, 25kHz Deviation, Pre-Em. off

*2 MONO, 25kHz Deviation, Pre-Em. on

*3 VOLUME MAX, BASS & TREBLE CENTER

Register Specifications

Slave address

SLAVE RECEIVER	SLAVE TRANSMITTER
80H (1000 0000)	81H (1000 0001)

Register table

SUB ADDRESS	DATA							
MSB LSB	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
****0000	*		TEST-DA	TEST1	ATT (4)			
****0001	*		VCO (6)					
****0010	*		FILTER (6)					
****0011	*		SPECTRAL (6)					
****0100	*		WIDEBAND (6)					
****0101	*		ATTSW	FST	NRSW	FOMO	SAPC	M1
****0110	*		PSW	FEXT1	FEXT2	TVSW	EXT	M2
****0111	*		VOL-L (6)					
****1000	*		VOL-R (6)					
****1001	*				BASS (4)			
****1010	*				TREBLE (4)			

* : Don't Care

Status Registers

when TEST1 = 0

STA1	STA2	STA3	STA4	STA5	STA6	STA7	STA8
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
POWER ON RESET	STEREO	SAP	NOISE	—	—	—	—

when TEST1 = 1

STA1	STA2	STA3	STA4	STA5	STA6	STA7	STA8
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
POWER ON RESET	STEREO	SAP	NOISE	FILADJ	—	—	—

Description of Registers

Control registers

Register	Number of bits	Classification*1	Contents
ATT	4	A	Input level adjustment
VCO	6	A	STEREO VCO & SAP VCO free running frequency adjustment
FILTER	6	A	STEREO and SAP and dbx filter adjustment
SPECTRAL	6	A	Adjustment of stereo separation (3kHz)
WIDEBAND	6	A	Adjustment of stereo separation (300Hz)
TEST-DA	1	T	Turn to DAC test mode and VCO adjustment mode by means of TEST-DA = 1.
TEST1	1	T	Turn to test mode by means of TEST = 1. (Adjustment of FILTER)
FST	1	T	Turn to forced stereo by means of FST = 1.
VOL-L	6	U	LSOUT-L output signal level control
VOL-R	6	U	LSOUT-R output signal level control
BASS	4	U	LSOUT output bass control
TREBLE	4	U	LSOUT output treble control
NRSW	1	U	Selection of the output signal (Stereo mode, SAP mode)
FOMO	1	U	Turn to forced MONO by means of FOMO = 1. (Left channel only is MONO during SAP output.)
TVSW	1	U	Selection of TV mode or external input mode for LPOUT output
EXT	1	U	Selection of external input 1 mode or external input 2 mode for LPOUT output. (TVSW = 1)
FEXT1	1	U	External input 1 forced MONO (1: forced MONO ON)
FEXT2	1	U	External input 2 forced MONO (1: forced MONO ON)
PSW	1	U	Selection of internal mode or LPIN mode for LSOUT output.
M1	1	U	Selection of LPOUT mute ON/OFF (0: mute ON, 1: mute OFF)
M2	1	U	Selection of LSOUT mute ON/OFF (0: mute ON, 1: mute OFF)
ATTSW	1	S	Turn the input stage MVCA off when ATTSW = 1.
SAPC	1	S	Selection of SAP mode or L + R mode according to the presence of SAP broadcasting

*1 Classification U: User control
A: Adjustment
S: Proper to set
T: Test

Status registers

Register	Number of bits	Contents	
PONRES	1	POWER ON RESET detection;	1: RESET
STEREO	1	Stereo discrimination of the COMPIN input signal;	1: Stereo
SAP	1	SAP discrimination of the COMPIN input signal;	1: SAP
NOISE	1	Noise level discrimination of the SAP signal;	1: Noise
FILADJ	1	Status of FILTER adjustment;	1: OK range

Description of Control Registers

ATT (4): Adjust the signal level input to COMPIN (Pin 17 (Pin 14)) to the standard input level (245mVrms).
Variable range of the input signal: 245mVrms –5.0dB to +3.0dB
0 = Level min.
F = Level max.

VCO (6): Adjust STEREO & SAP VCO free running frequency (fo).
Variable range: fo ±20%
0 = Free running frequency min.
3F = Free running frequency max.

FILTER (6): Adjust the filter fo of the ST, SAP and dbx blocks.
Variable range: fo ±20%
0 = Frequency min.
3F= Frequency max.

SPECTRAL (6): Perform high frequency (fs = 3kHz) separation adjustment.
0 = Level max.
3F = Level min.

WIDEBAND (6): Perform low frequency (fs = 300Hz) separation adjustment.
0 = Level min.
3F = Level max.

TEST-DA (1): Set DAC output test mode and VCO adjustment mode.
0 = Normal mode
1 = DAC output test mode and VCO adjustment mode
In addition, the following outputs are present at Pins 40 and 39.
LPOUT-L (Pin 40): DA control DC level
LPOUT-R (Pin 39): STEREO VCO oscillation frequency ($4f_H$)

TEST1 (1): Set filter adjustment mode.
0 = Normal mode
1 = FILTER (STA5) adjustment mode
In addition, the following outputs are present at Pins 40 and 39.
LPOUT-L (Pin 40): SAP BPF OUT
LPOUT-R (Pin 39): NR BPF OUT

FST (1): Select forced STEREO mode
0 = Normal mode
1 = Forced stereo mode

VOL-L (6): LSOUT-L output signal level control
0 = Volume Min. (–80dB)
3F= Volume Max. (0dB)
–1.25 dB/STEP

VOL-R (6): LSOUT-R output signal level control
0 = Volume Min. (–80dB)
3F= Volume Max. (0dB)
–1.25 dB/STEP

BASS (4): LSOUT output bass control
0 = Bass Min.
7 & 8 = Bass Center (0dB)
F = Bass Max.

TREBLE (4): LSOUT output treble control
0 = Treble Min.
7 & 8 = Treble Center (0dB)
F = Treble Max.

NRSW (1): Select stereo mode or SAP mode
0 = Stereo mode
1 = SAP mode

FOMO (1): Select forced MONO mode
0 = Normal mode
1 = Forced MONO mode

TVSW (1): Select TV mode or external input mode for LPOUT output.
0 = TV mode
1 = External input mode

EXT (1): Select external input [1] mode or external input [2] mode for LPOUT output. (TVSW = 1)
0 = External input [1] mode
1 = External input [2] mode

FEXT1 (1): Turn external input [1] to forced MONO.
0 = Normal mode
1 = External input [1] is forced MONO.
Input the same signal to both AUX1-L and AUX1-R.

FEXT2 (1): Turn external input [2] to forced MONO
0 = Normal mode
1 = External input [2] is forced MONO
Input the same signal to both AUX2-L and AUX2-R.

PSW (1) Select INT mode or LPIN mode for LSOUT output.
0 = INT mode
1 = LPIN mode

M1 (1): Mute the LPOUT-L and LPOUT-R output.
0 = Mute ON
1 = Mute OFF

M2 (1): Mute the LSOUT-L and LSOUT-R output.
0 = Mute ON
1 = Mute OFF

ATTSW (1) Select BYPASS SW of MVCA
0 = Normal mode
1 = MVCA is passed

SAPC (1): Select the SAP signal output mode
When there is no SAP signal, the conditions for selecting SAP output are selected by SAPC.
0 = L + R output is selected
1 = SAP output is selected

Description of Mode Control

Priority ranking: M1/M2 > TVSW/EXT > TEST-DA > TEST1 > (NRSW & FOMO & SAPC)

<table>
<tr><th>Mode control</th><th>SAPC = 0</th><th>SAPC = 1</th></tr>
<tr><td>NRSW</td><td>“Select dbx input and TV decoder output”
Conditions: FOMO = 0
NRSW = 0 (MONO or ST output)
• During ST input: left channel: L,
right channel: R
• During other input: left channel: L + R,
right channel: L + R

NRSW = 1 (SAP output)
• When there is “SAP” during SAP discrimination
– left channel: SAP, right channel: SAP
• When there is “No SAP”, output is the same as when NRSW = 0.</td><td>“Select dbx input and TV decoder output”
Conditions: FOMO = 0
NRSW = 0 (MONO or ST output)
As on the left

NRSW = 1 (SAP output)
• Regardless of the presence of SAP discrimination,
dbx input: “SAP”
left channel: SAP, right channel: SAP
However, when there is no SAP, SAPOUT output is soft muted (–7dB)</td></tr>
<tr><td>FOMO</td><td colspan="2">“Forced MONO”
FOMO = 1
• During SAP output: left channel: L + R, right channel: SAP
• During ST or MONO output: left channel: L + R, right channel: L + R</td></tr>
<tr><td>SAPC</td><td colspan="2">Change the selection conditions for “MONO or ST output” and “SAP output”.
SAPC = 0: Switch to SAP output when there is SAP discrimination.
Do not switch to SAP output when there is no SAP discrimination.
SAPC = 1: Switch to SAP output regardless of whether there is SAP discrimination.</td></tr>
<tr><td>M1/M2</td><td colspan="2">“MUTE”
M1 = 0: LPOUT output is muted.
M2 = 0: LSOUT output is muted.</td></tr>
<tr><td>TVSW/EXT</td><td colspan="2">“TV mode/external input mode selection”
TVSW = 0: Set LPOUT output to TV mode.
TVSW = 1: Set LPOUT output to external input mode.
EXT = 0: Set LPOUT output to external input [1] mode. (TVSW = 1)
EXT = 1: Set LPOUT output to external input [2] mode. (TVSW = 1)</td></tr>
<tr><td>TEST1</td><td colspan="2">“TEST1”
TEST1 = 1
Return adjustment data with STATUS REGISTER as an adjustment mode.
In addition, outputs are as follows.
left channel: SAP BPF OUT
right channel: NR BPF OUT</td></tr>
<tr><td>TEST-DA</td><td colspan="2">“TEST-DA”
TEST-DA = 1
Used to adjust the D/A TEST and VCO.
left channel: D/A output
right channel: STVCO oscillation frequency (4f_H)</td></tr>
</table>

Decoder Output and Mode Control Table 1 (SAPC = 1)

Input signal mode	Mode detection			Mode control			dbx input	Output	
	ST	SAP	NOISE	NRSW	FOMO	SAPC		Lch	Rch
MONO *1	0	0	0	0	*	1	MUTE	L + R	L + R
	0	0	0	1	0	1	SAP	SAP	SAP
	0	0	0	1	1	1	SAP	L + R	SAP
	0	*	1	0	*	1	MUTE	L + R	L + R
	0	*	1	1	0	1	(SAP)	(SAP)	(SAP)
	0	*	1	1	1	1	(SAP)	L + R	(SAP)
STEREO *1	1	0	*	0	0	1	L – R	L	R
	1	0	*	0	1	1	MUTE	L + R	L + R
	1	1	1	0	0	1	L – R	L	R
	1	1	1	0	1	1	MUTE	L + R	L + R
	1	0	0	1	0	1	SAP	SAP	SAP
	1	0	0	1	1	1	SAP	L + R	SAP
	1	*	1	1	0	1	(SAP)	(SAP)	(SAP)
	1	*	1	1	1	1	(SAP)	L + R	(SAP)
MONO & SAP	0	1	*	0	0	1	MUTE	L + R	L + R
	0	1	*	0	1	1	MUTE	L + R	L + R
	0	1	0	1	0	1	SAP	SAP	SAP
	0	1	0	1	1	1	SAP	L + R	SAP
	0	1	1	1	0	1	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	1	(SAP)	L + R	(SAP)
STEREO & SAP	1	1	*	0	0	1	L – R	L	R
	1	1	*	0	1	1	MUTE	L + R	L + R
	1	1	0	1	0	1	SAP	SAP	SAP
	1	1	0	1	1	1	SAP	L + R	SAP
	1	1	1	1	0	1	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	1	(SAP)	L + R	(SAP)

Note

(SAP) : The SAPOUT output signal is soft muted (approximately –7dB).
The signal is soft muted when NOISE = 1.

* : Don't care.

*1 SAP or NOISE discrimination may be made during MONO or STEREO input when the noise is inputted in the weak electric field.
"NOISE" status rises earlier than "SAP" status when the amount of noise is increased to COMPIN.

Decoder Output and Mode Control Table 2 (SAPC = 0)

Input signal mode	Mode detection			Mode control			dbx input	Output	
	ST	SAP	NOISE	NRSW	FOMO	SAPC		Lch	Rch
MONO *1	0	0	*	*	*	0	MUTE	L + R	L + R
	0	1	1	0	0	0	MUTE	L + R	L + R
	0	1	1	0	1	0	MUTE	L + R	L + R
	0	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	0	(SAP)	L + R	(SAP)
STEREO *1	1	0	*	0	0	0	L – R	L	R
	1	0	*	0	1	0	MUTE	L + R	L + R
	1	0	*	1	0	0	L – R	L	R
	1	0	*	1	1	0	MUTE	L + R	L + R
	1	1	1	0	0	0	L – R	L	R
	1	1	1	0	1	0	MUTE	L + R	L + R
	1	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	0	(SAP)	L + R	(SAP)
MONO & SAP	0	1	0	0	0	0	MUTE	L + R	L + R
	0	1	0	0	1	0	MUTE	L + R	L + R
	0	1	0	1	0	0	SAP	SAP	SAP
	0	1	0	1	1	0	SAP	L + R	SAP
	0	1	1	0	0	0	MUTE	L + R	L + R
	0	1	1	0	1	0	MUTE	L + R	L + R
	0	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	0	(SAP)	L + R	(SAP)
STEREO & SAP	1	1	0	0	0	0	L – R	L	R
	1	1	0	0	1	0	MUTE	L + R	L + R
	1	1	0	1	0	0	SAP	SAP	SAP
	1	1	0	1	1	0	SAP	L + R	SAP
	1	1	1	0	0	0	L – R	L	R
	1	1	1	0	1	0	MUTE	L + R	L + R
	1	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	0	(SAP)	L + R	(SAP)

Note

(SAP) : The SAPOUT output signal is soft muted (approximately –7dB).
The signal is soft muted when NOISE = 1.

* : Don't care.

*1 SAP or NOISE discrimination may be made during MONO or STEREO input when the noise is inputted in the weak electric field.
"NOISE" status rises earlier than "SAP" status when the amount of noise is increased to COMPIN.

Mode Control Table 3

	M1	TVSW	EXT	FEXT1	FEXT2	LPOUT-L	LPOUT-R
1	0	–	–	–	–	MUTE	MUTE
2	1	0	–	–	–	TV (L)	TV (R)
3	1	1	0	0	–	AUX1-L	AUX1-R
4	1	1	0	1	–	AUX1-L	AUX1-L
5	1	1	1	–	0	AUX2-L	AUX2-R
6	1	1	1	–	1	AUX2-L	AUX2-L

TV (L) / TV (R) are selected in MATRIX

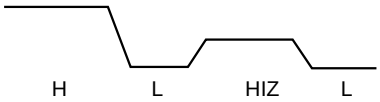
TV (L): MONO, ST-L, SAP, (SAPBPFout, D/Aout)

TV (R): MONO, ST-R, SAP, (NRBPFout, STVCO freerun ($4f_H$))

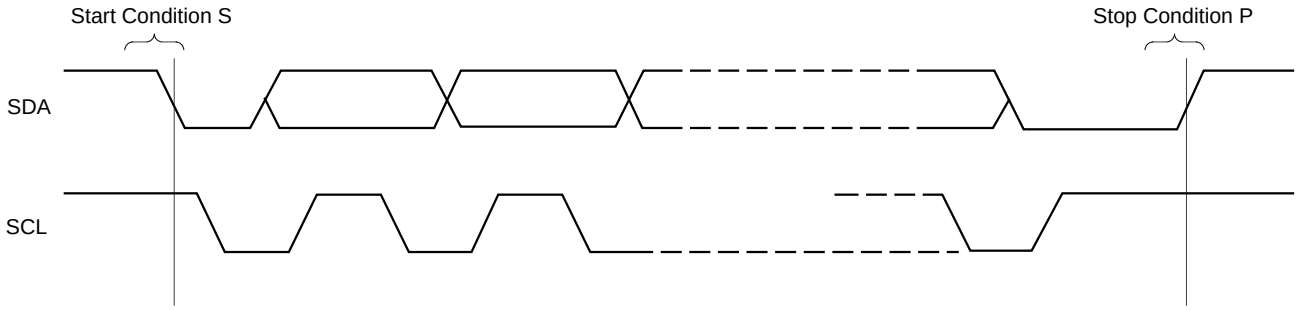
I^2C BUS Signal

There are two I^2C signals, SDA (Serial DATA) and SCL (Serial CLOCK) signals. SDA is a bidirectional signal.

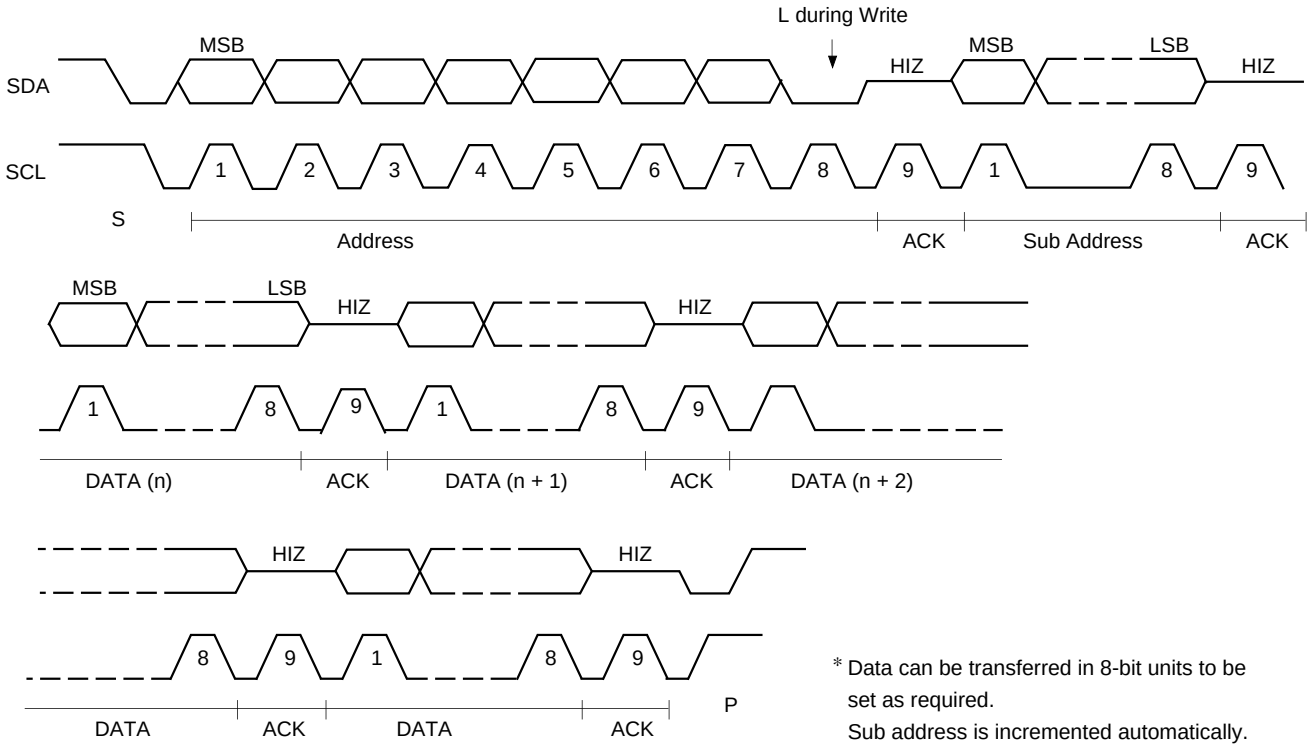
• Accordingly there are 3 values outputs, H, L and HIZ.



• I^2C transfer begins with Start Condition and ends with Stop Condition.

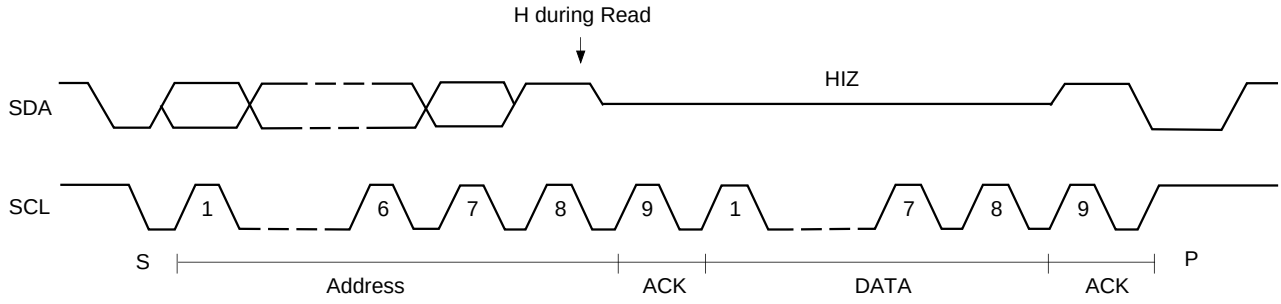


• **I²C data Write (Write from I²C controller to the IC)**

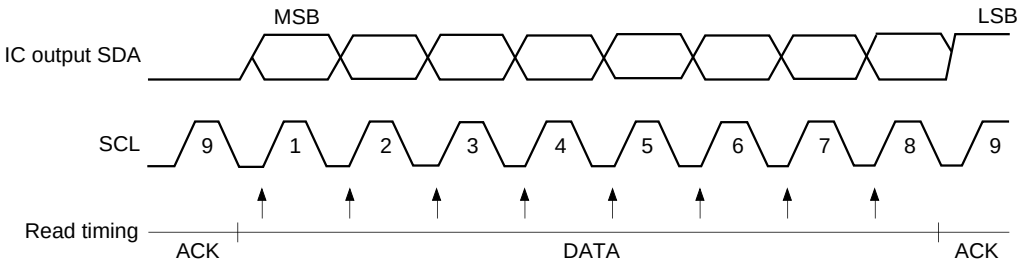


* Data can be transferred in 8-bit units to be set as required.
Sub address is incremented automatically.

• **I²C data Read (Read from the IC to I²C controller)**

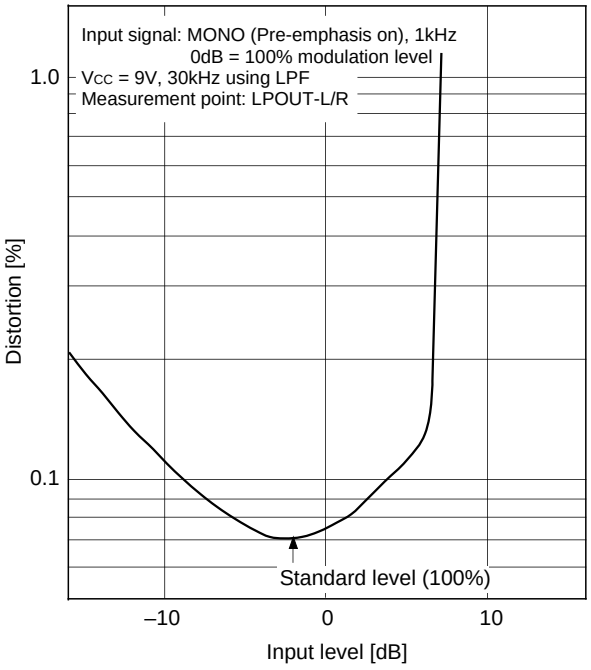


• Read timing

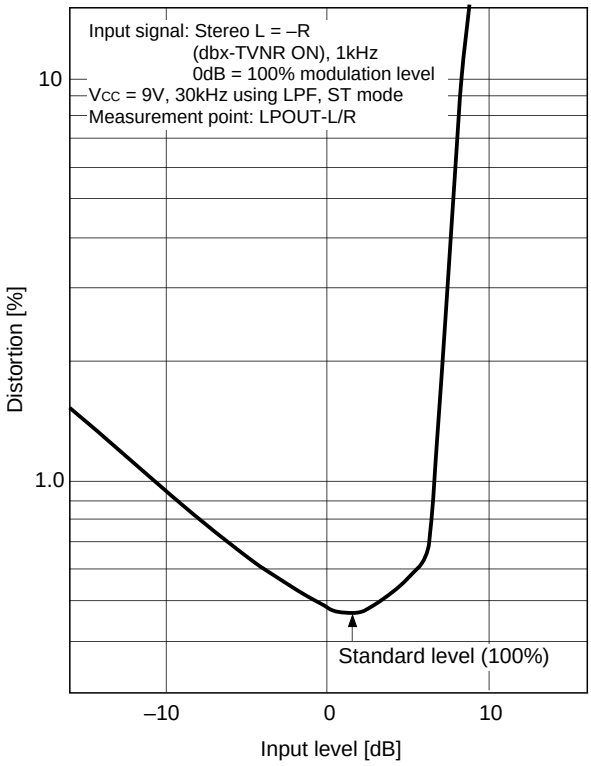


* Data Read is performed during SCL rise.

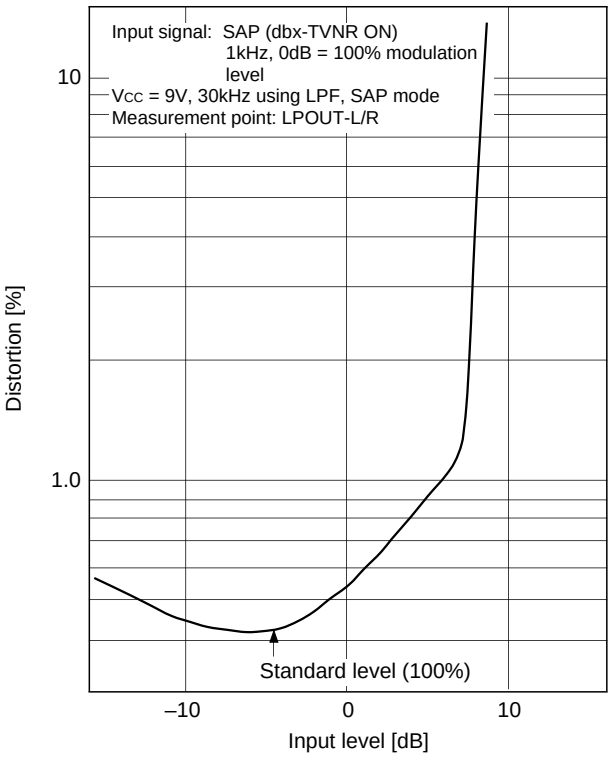
Input level vs. Distortion characteristics 1 (MONO)



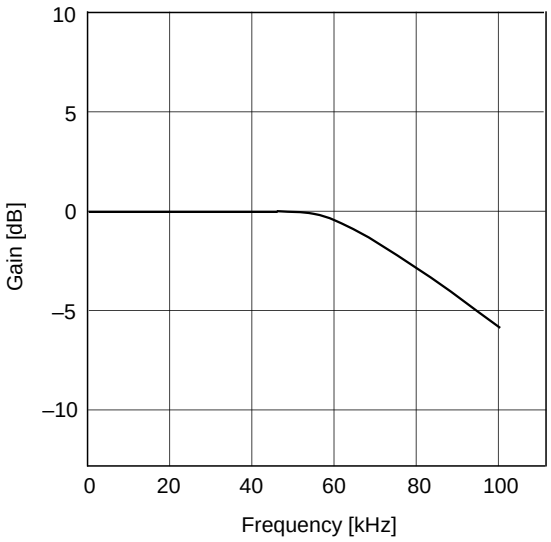
Input level vs. Distortion characteristics 2 (Stereo)



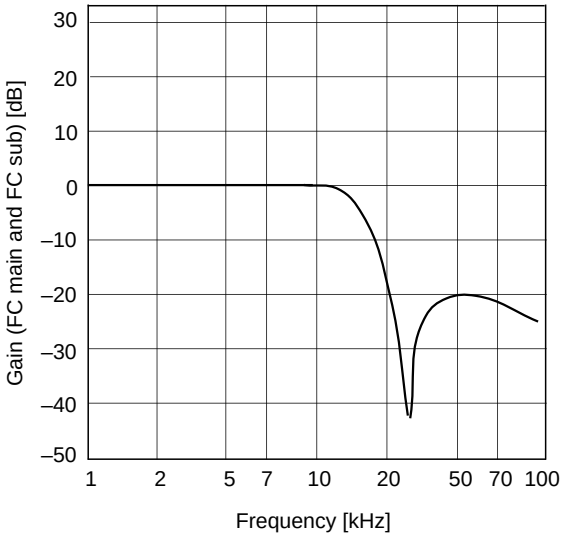
Input level vs. Distortion characteristics 3 (SAP)



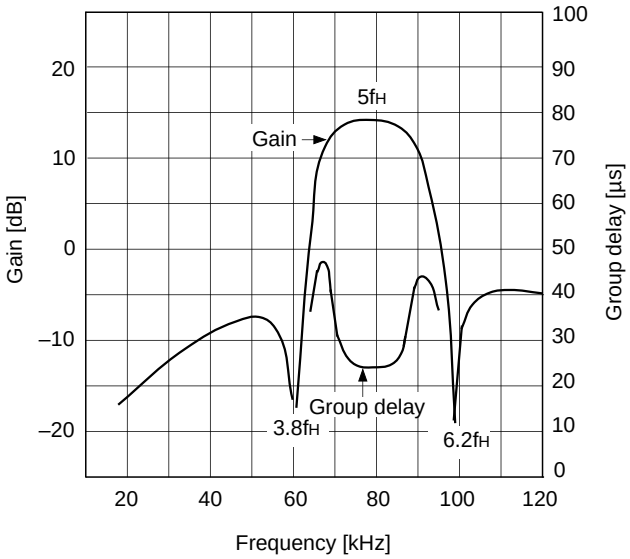
Stereo LPF frequency characteristics



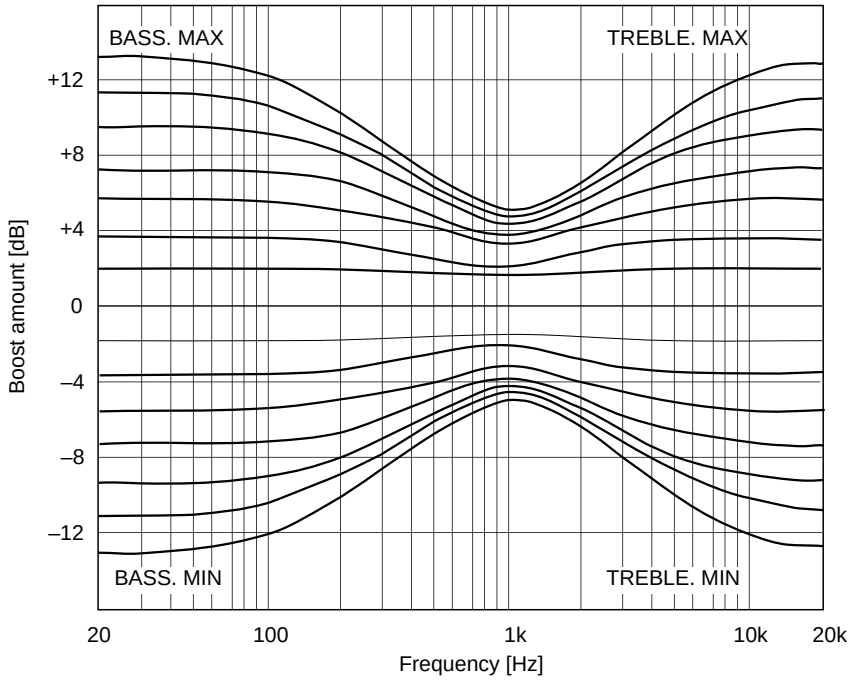
Main LPF and Sub LPF frequency characteristics



SAP frequency characteristics and group delay

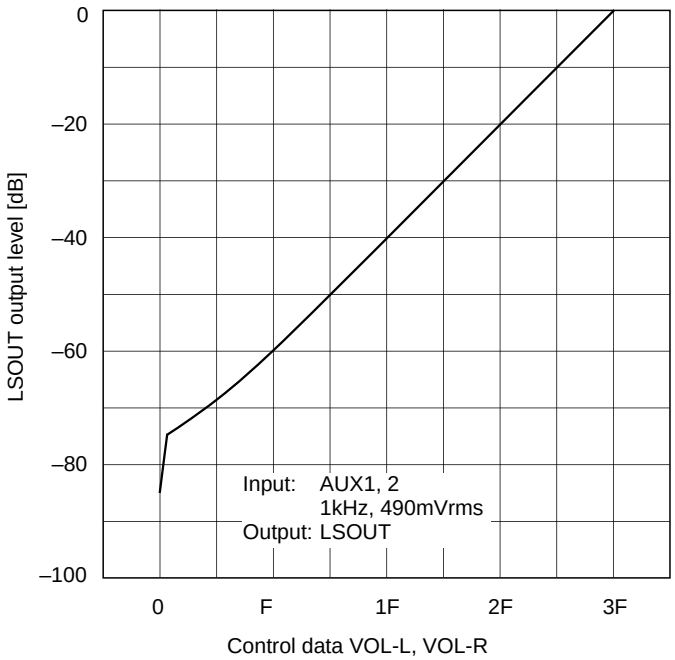


BASS-TREBLE characteristics



Input: AUX1, 2
245mVrms
Output: LSOUT

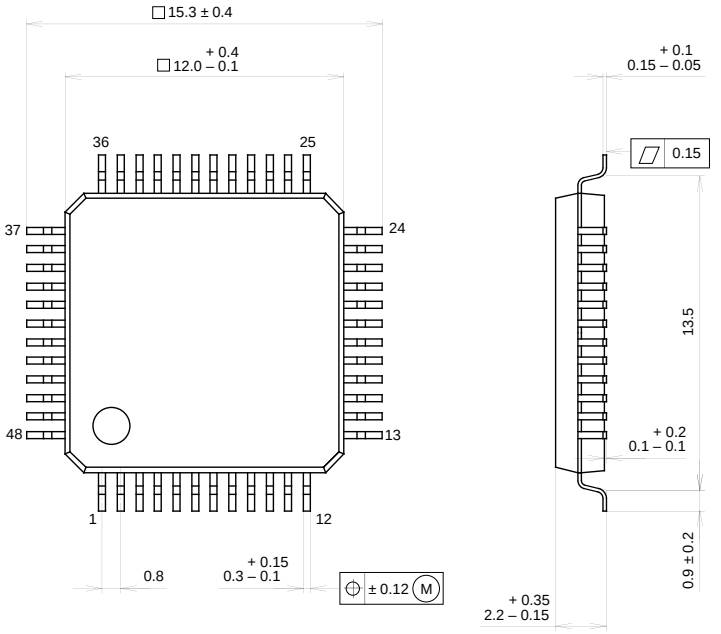
Volume characteristics



Package Outline Unit: mm

CXA2074Q

48PIN QFP (PLASTIC)



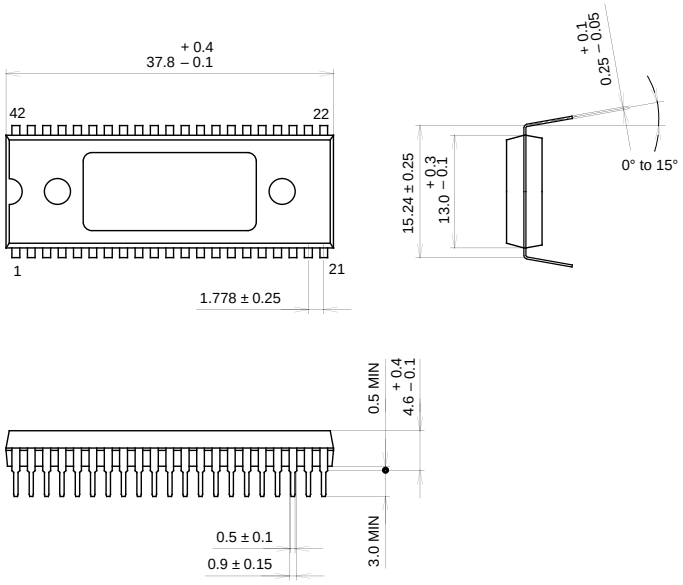
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	

CXA2074S

42PIN SDIP (PLASTIC) 600mil



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	4.4g

SONY CODE	SDIP-42P-02
EIAJ CODE	SDIP042-P-0600-A
JEDEC CODE	