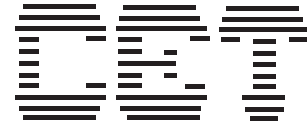


CED6060R/CEU6060R



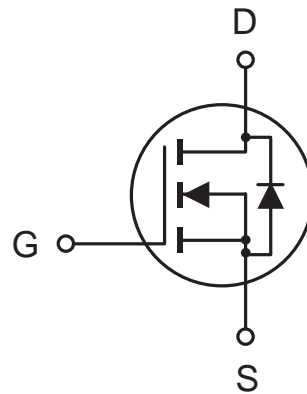
Feb. 2003

N-Channel Logic Level Enhancement Mode Field Effect Transistor

FEATURES

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- 60V , 30A , $R_{DS(ON)}=25m\Omega$ @ $V_{GS}=10V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-251 & TO-252 package.



ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous @ $T_J=125^\circ\text{C}$ -Pulsed	I_D	30	A
	I_{DM}	120	A
Drain-Source Diode Forward Current	I_S	30	A
Maximum Power Dissipation @ $T_c=25^\circ\text{C}$ Derate above 25°C	P_D	50	W
		0.3	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$

CED6060R/CEU6060R

ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE AVALANCHE RATING^a						
Single Pulse Drain-Source Avalanche Energy	E _{AS}	V _{DD} =25V, L=25μH R _G =25Ω		200		mJ
Maximum Drain-Source Avalanche Current	I _{AS}			30		A
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V			25	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS^a						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2		4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =24A			25	mΩ
On-State Drain Current	I _{D(ON)}	V _{GS} =10V, V _{DS} =10V	60			A
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =24A		20		S
SWITCHING CHARACTERISTICS^b						
Turn-On Delay Time	t _{D(ON)}	V _{DD} =30V, I _D =30A, V _{GS} =10V, R _{GEN} =7.5Ω		15	20	ns
Rise Time	t _r			250	300	ns
Turn-Off Delay Time	t _{D(OFF)}			45	60	ns
Fall Time	t _f			130	150	ns
Total Gate Charge	Q _g	V _{DS} =48V, I _D =30A, V _{GS} =10V		36	43	nC
Gate-Source Charge	Q _{gs}			9		nC
Gate-Drain Charge	Q _{gd}			19		nC

CED6060R/CEU6060R

ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS^b						
Input Capacitance	C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0\text{V}$ $f=1.0\text{MHz}$		1178		pF
Output Capacitance	C_{oss}			428		pF
Reverse Transfer Capacitance	C_{rss}			95		pF
DRAIN-SOURCE DIODE CHARACTERISTICS^b						
Diode Forward Voltage	V_{SD}	$V_{GS}=0\text{V}, I_S=24\text{A}$		0.9	1.3	V

Notes

a. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

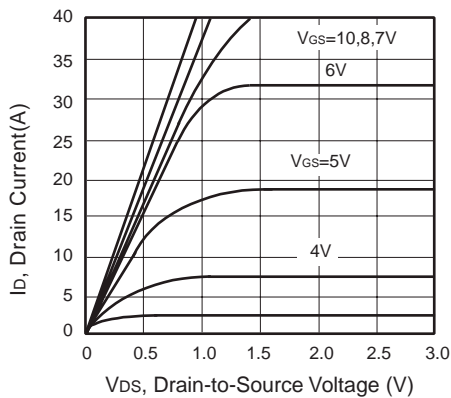


Figure 1. Output Characteristics

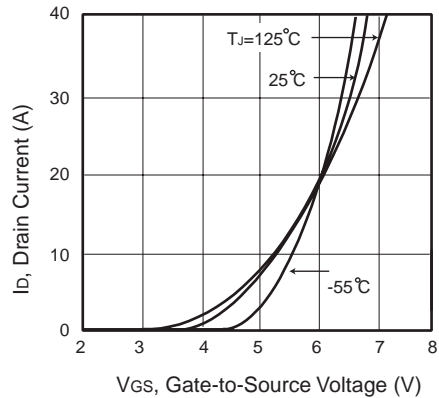


Figure 2. Transfer Characteristics

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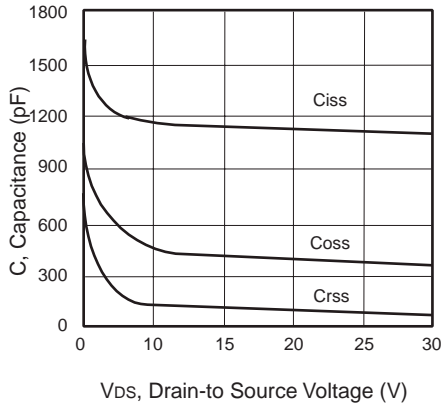


Figure 3. Capacitance

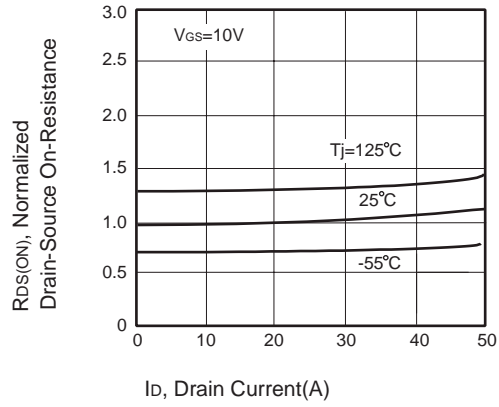


Figure 4. On-Resistance Variation with Drain Current and Temperature

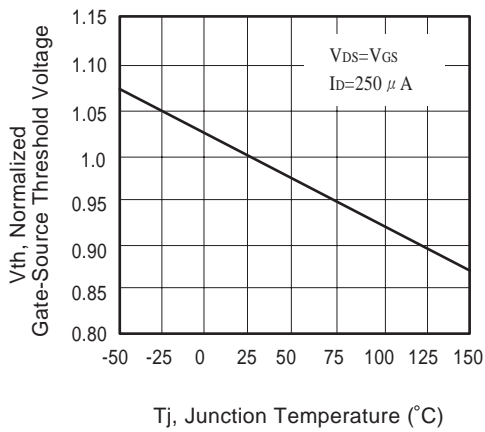


Figure 5. Gate Threshold Variation with Temperature

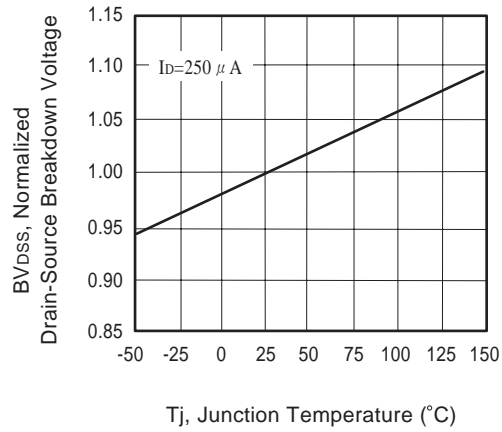


Figure 6. Breakdown Voltage Variation with Temperature

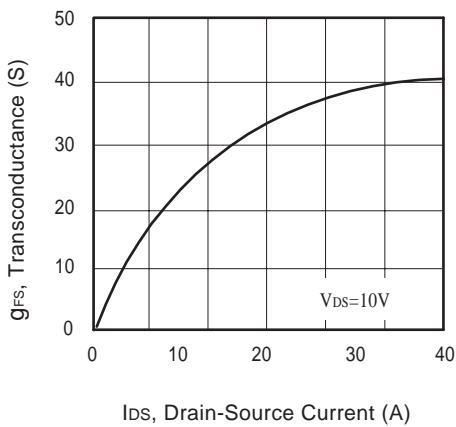


Figure 7. Transconductance Variation with Drain Current

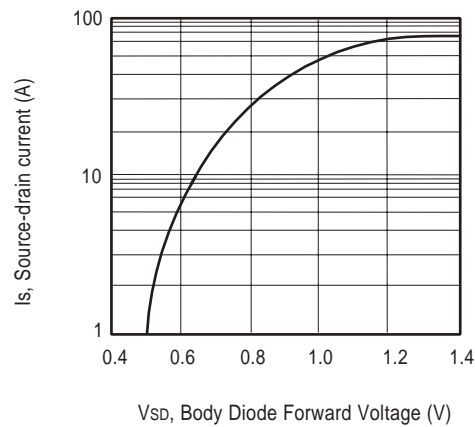


Figure 8. Body Diode Forward Voltage Variation with Source Current

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CED6060R/CEU6060R

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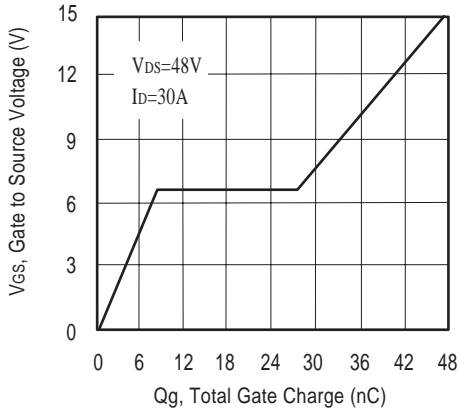


Figure 9. Gate Charge

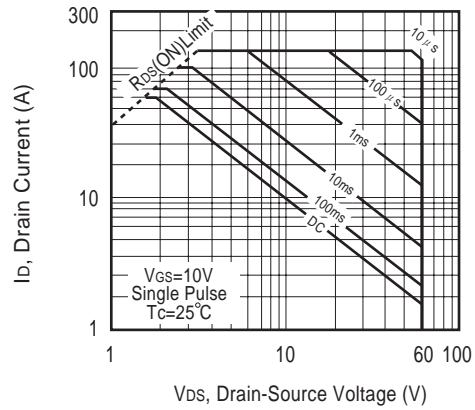


Figure 10. Maximum Safe Operating Area

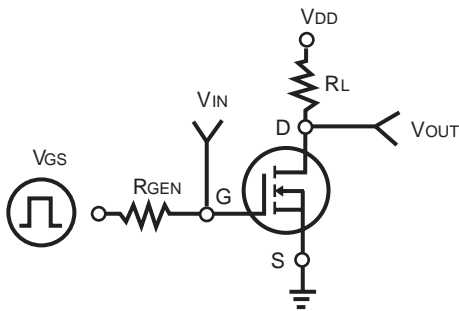


Figure 11. Switching Test Circuit

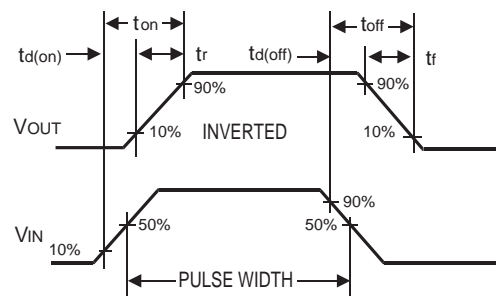


Figure 12. Switching Waveforms

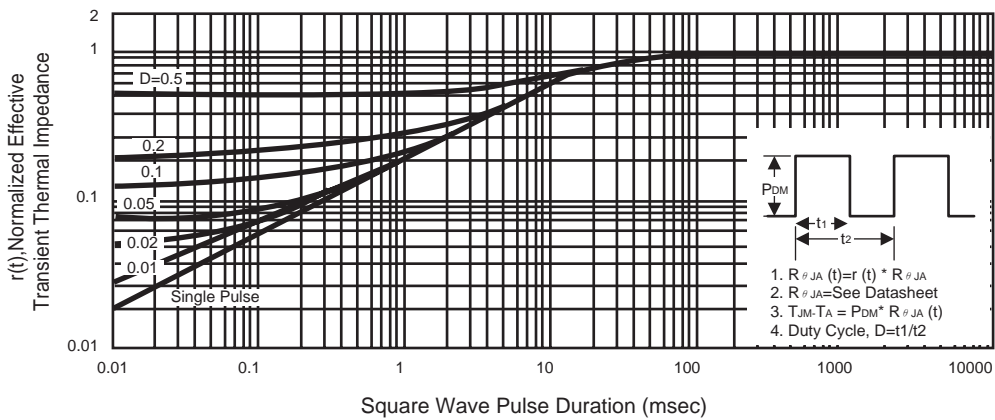


Figure 13. Normalized Thermal Transient Impedance Curve