

Structure Silicon monolithic integrated circuit

Product Name Sound Generator for cellular phone

Product No. **BU8899GU**

Features 64 polyphonic tones, 128 sounds plus 47 drum set sounds, 15 electric drum set sounds
Up to 8 user customized sound can be used to create original sounds.

○Absolute Maximum Ratings(unless otherwise noted, Ta = 25°C)

Parameter	Symbol	Rating	Unit	Remarks
Maximum I/O supply voltage	VDDIO	-0.3 ~ 4.5	V	DVDD_IO, AVDD
Maximum CORE supply voltage	VDDCO	-0.3 ~ 3.5	V	DVDD_CORE
Voltage applied to pin	VIN	DVSS-0.3 ~ VDDIO+0.3	V	
Input current	IIN	-1 ~ +1	uA	
Allowable dissipation	Pd	1600 (*1)	mW	
Storage temperature range	Tstg	-50 ~ 125	°C	
Operating temperature range	Topr	-30 ~ 85	°C	

(*1) Note: Reduce to 5.0mW/°C when Ta = 25°C or above

○Recommended Operating Power Supply Voltage Range(Unless otherwise noted, Ta = 25°C)

Parameter	Symbol	rating			Unit	Remarks
		Min	Typ	Max		
I/O Power supply voltage	VDDIO	2.7	3.0	3.3	V	DVDD_IO, AVDD
CORE Power supply voltage	VDDCO	2.25	2.5	2.75	V	DVDD_CORE
Ambient temperature	Ta	-30	25	85	°C	
MCLK input frequency	FMCLK	2.688	-	20	MHz	
SCLK input frequency	FSCLK	-	-	20	MHz	Internal operation frequency / 2 or less
MCLK duty	DMCLK	40	50	60	%	
Analog pin's load resistance	ZAN	10	-	-	kΩ	

This chip is not designed to protect itself against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

Application example

The product described in this specification is designed to be used with ordinary electronic equipment or devices(such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).

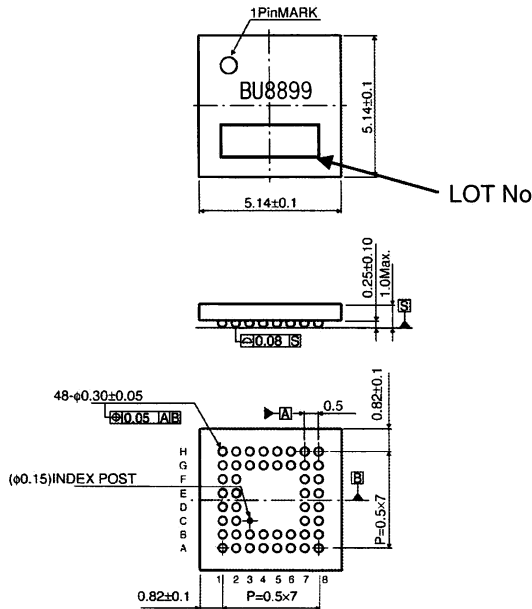
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○Electrical Characteristics

(Unless otherwise noted, Ta = 25°C)

Parameter	Symbol	rating			Unit	Conditions
		Min	Typ	Max		
Digital DC characteristics						
High-level input voltage	VIH	DVDD_ IO-0.5	-	-	V	
Low-level input voltage	VIL	-	-	DVSS +0.5	V	
High-level input voltage	IIH	-	-	1	μA	VIH=VDDIO
Low-level input voltage	IIL	-1	-	-	μA	VIL=DVSS
High-level output voltage	VOH	DVDD_ IO-0.3	-	-	V	IOH=-0.8mA
Low-level output voltage	VOL	-	-	DVSS+ 0.3	V	IOL=0.8mA
Analog DC characteristics						
VREF pin voltage	VAGND	0.475 AVDD	0.5AVD D	0.525 AVDD	V	IOUT=0A(no load)
Analog pin voltage	VOUT	0.47 AVDD	0.5AVD D	0.53 AVDD	V	IOUT=0A(no load) Not playing
General characteristics						
VREF pin rise time	TRVR	-	15	25	mS	When CVREF = 1uF, NRST=L→H
Analog pin characteristics						
Analog amplitude	VMAX	-	0.6 AVDD	-	Vp-p	Theoretical value for dynamic range
Power consumption DVDD_CORE=2.5[V], DVDD_IO=3.0[V], AVDD=3.0[V], internal operation frequency SYS_CLK=50[MHz]						
Analog Idd1	AIDD1	-	1.5	2.5	mA	Playing
Digital Idd10	DIDD10	-	28	35	mA	Not playing MIDI CLK control="101"
Digital Idd11 (DVDD_CORE)	DIDD11	-	56	65	mA	Playing 64POLY
Digital Idd12 (DVDD_IO)	DIDD12	-	0.4	1	mA	Playing
Analog Idd2	AIDD2	-	-	1	μA	Standby mode
Digital Idd20 (DVDD_CORE)	DIDD20	-	-	10	μA	Standby mode

○ External measure and View

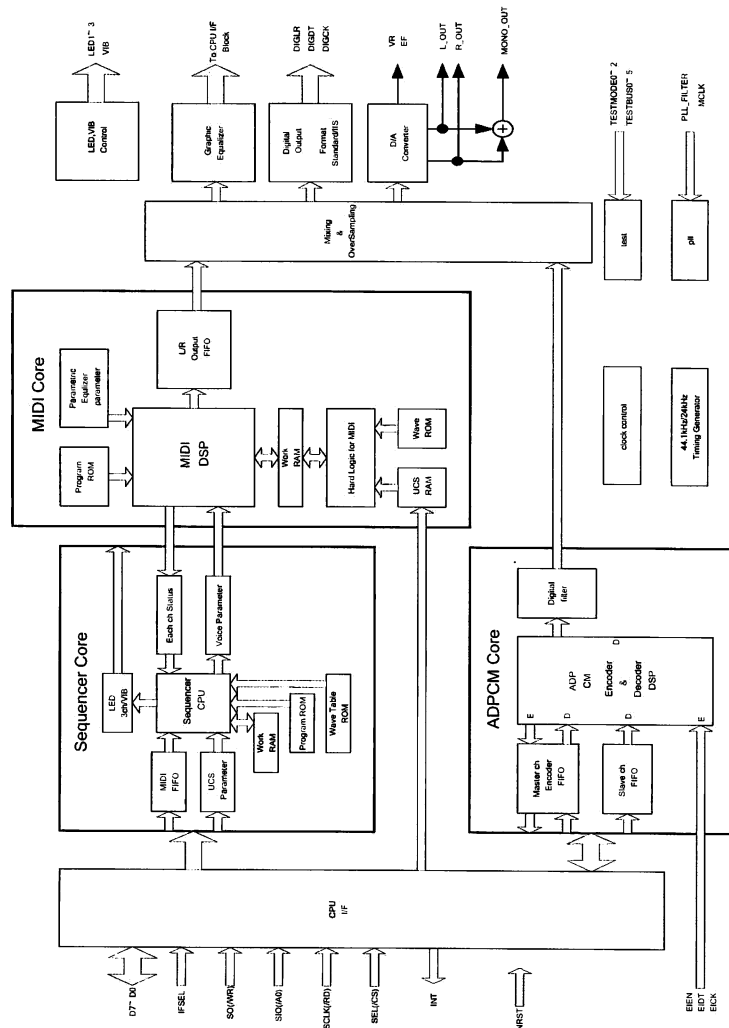


VCSP85H5 (48Pin) (Unit: mm)

○ Pin layout diagram

Pin NO.	Pin name	Pin NO.	Pin name	Pin NO.	Pin name
A2	VIB	H3	DVSS	F2	DIGDT
A3	INT	D8	TMODE2	G2	DIGCK
B3	LED1	E8	TMODE1	G6	TESTBUS0
A4	LED2	E7	TMODE0	H6	TESTBUS1
B4	LED3	A7	DVDD_IO	H5	TESTBUS2
D7	D7	H1	DVDD_IO	G5	TESTBUS3
C8	D6	F8	R_OUT	H4	TESTBUS4
C7	D5	F7	VREF	G4	TESTBUS5
B8	D4	G8	L_OUT	G3	PLL_FILTER
B6	D3	G7	AVSS	G1	MCLK
A6	D2	H8	AVDD	E2	IFSEL
B5	D1	H7	MONO_OUT	E1	SO(/WR)
A5	D0	B2	EIEN	D1	SIQ(/AO)
B7	DVDD_CORE	A1	EIDT	D2	SCLK(/RD)
H2	DVDD_CORE	B1	EICK	C1	SEL(/CS)
A8	DVSS	F1	DIGLR	C2	NRST

○ Block diagram



- Cautions on use
 - (1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.
 - (2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.
 - (3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.
 - (4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies have the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.
 - (5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.
 - (6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.
 - (7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.
 - (8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.
 - (9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.
 - (10) Ground wiring pattern

If small-signal GND and large-current GND are provided, it will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.
 - (11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.
 - (12) Others

In case of use this LSI, please peruse some other detail documents, we called , Technical note, Functional description, Application note.

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