PM8316
PM8611

TEMUX-84/SBS-LITE

OC-12 LINE CARD REFERENCE DESIGN

PRELIMINARY

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1 INTRODUCTION

The OC-12 Line Card Reference Design is a sample application of several PMC-Sierra devices including:

- PM5313 SPECTRA-622
- PM8316 TEMUX-84
- PM8611 SBI Bus Serializer (SBS-Lite)

1.1 Purpose

The OC-12 Line Card Reference Design is intended to assist engineers in designing their products using PMC-Sierra's devices. The purpose of this document is to provide a detailed hardware specification for the OC-12 Line Card. The specification detailed here is sufficient to allow design implementation and verification.

1.2 Scope

This document describes the design for the OC-12 Line Card. A general description of the card is given, along with a block diagram for the design. A description for each of the functional blocks of the design is given followed by a detailed account of design issues, including physical and mechanical descriptions, timing, simulations and implementation descriptions.

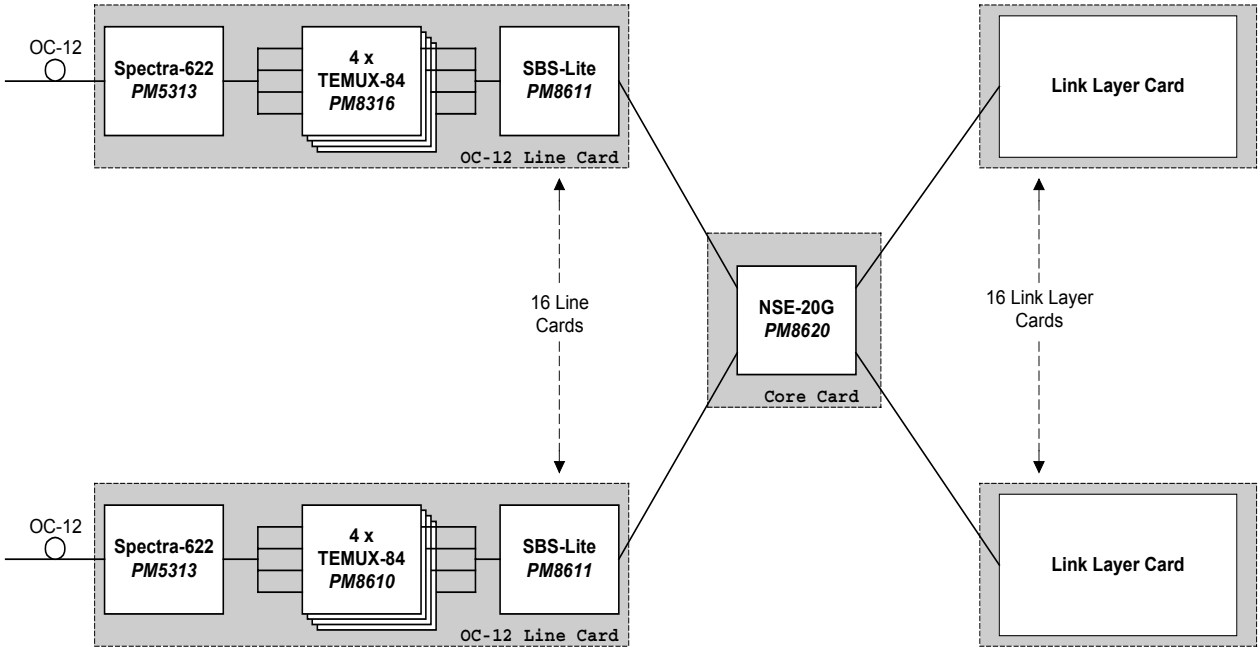
The OC-12 Line Card is fully capable of handling either SONET or SDH formats, but for simplicity of explanation, the SONET standard will be dealt with exclusively throughout this document. Please refer to each device datasheet for SDH configuration information.

1.3 Application

The OC-12 Line Card is designed to be one of many line cards in a larger switching system. Each line card receives and decodes an OC-12 SONET stream, with the ability to switch any DS0 within the OC-12 frame. The data is then sent over an LVDS serial backplane to the working and protection core cards, which perform switching of the traffic. The core card, using a PM8620 Narrowband Switch Element (NSE-20G), can switch any DS0 from any of the 32 input ports on the core card, to any of the 32 output ports; therefore having the capacity to support a maximum of 16 line cards and 16 link layer cards.

When an NSE is placed between the framers of the line cards and link layer devices of the service cards, it allows the construction of an NxDS0 switch of up to 20 Gb/s. Figure 1 demonstrates how up to 16 OC-12 Line Cards can connect to a Core Card to create a switching system with a bandwidth of ~20 Gb/s.

Figure 1 – Switching System Architecture



The line card is a specific application that demonstrates certain features of the SPECTRA-622, TEMUX-84 and SBS-Lite. Please refer to the individual product datasheets for the full listing of possible applications.

2 FEATURES

This Reference Design provides the following features:

Implements an OC-12 Line Card using the following PMC-Sierra devices:

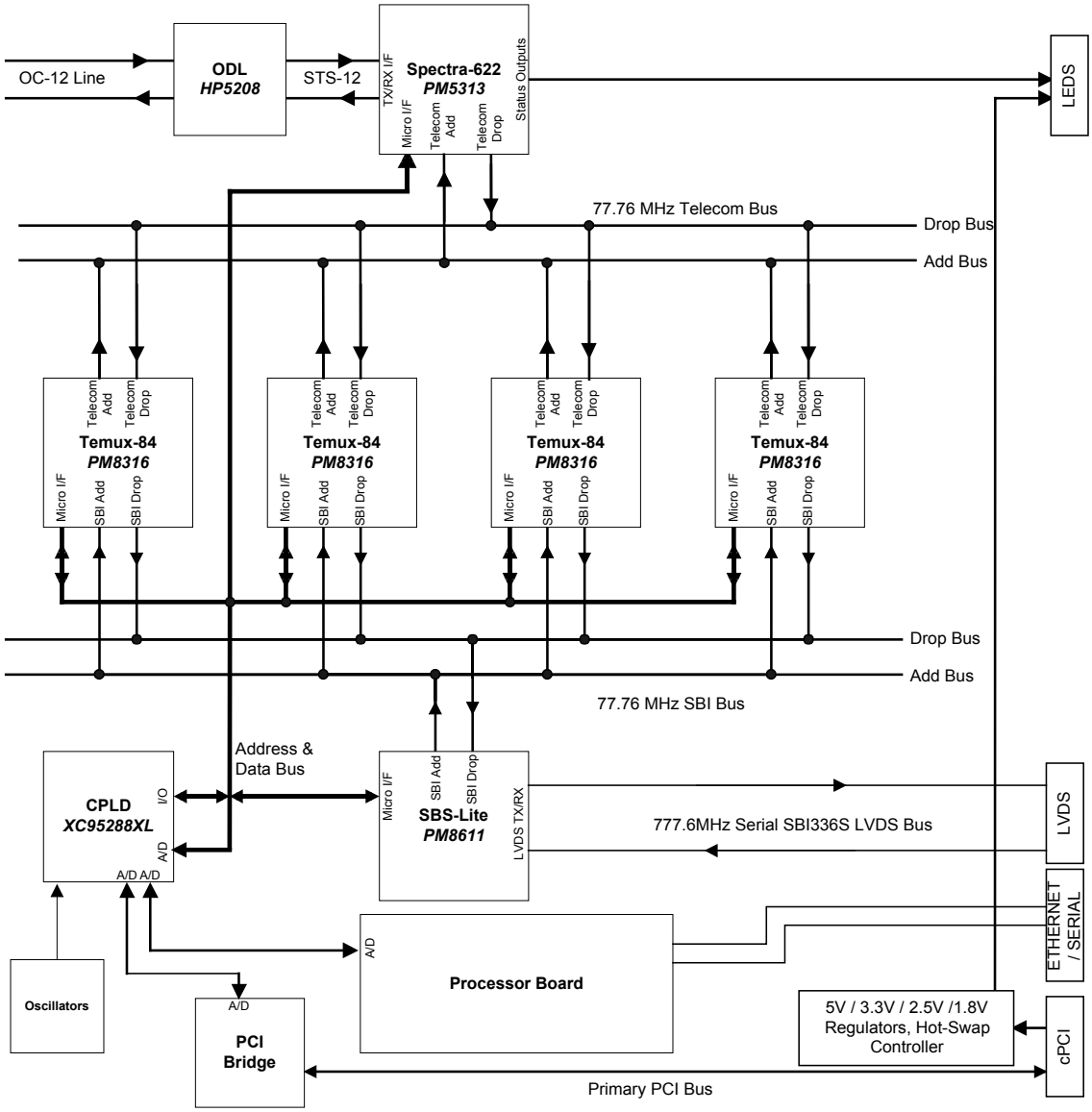
- PM5313 SPECTRA-622 OC-12 SONET/SDH payload extractor/aligner
- PM8316 TEMUX-84 High Density T1/E1 Framer with integrated VT/TU Mapper and M13 Multiplexer
- PM8611 SBI BUS Serializer (SBS-Lite)
- 3.3 Volt CMOS telecom bus configured to operate as a 77.76 MHz 8-bit wide telecom bus interface, between the SPECTRA-622 and four TEMUX-84s.
- Includes a 77.76 MHz 8-bit SBI336 bus, allowing communication between the four TEMUX-84s and the SBS-Lite.
- Interfaces to a +5V cPCI 33MHZ backplane.
- Generic onboard processor with ethernet/serial interface
- Contains oscillators for framing of T1, E1, and DS3 payloads over the Telecom and SBI busses.
- Provides dual 777.6 MHz Serial SBI336S LVDS links for communication with the core cards over the backplane.
- Front panel status LED’s which displays line status, alarms, and power supply status.
- Ability to receive 77.76 MHz clock and 2 KHz frame pulse from the backplane, onboard oscillators, or external sources through the front panel.
- Full Hot Swap Control with extraction indicator.

3 GENERAL DESCRIPTION

3.1 Block Diagram

The OC-12 Line Card is controlled via the CompactPCI bus from a host CPU or a generic processor daughterboard. Figure 2 illustrates the reference design block diagram.

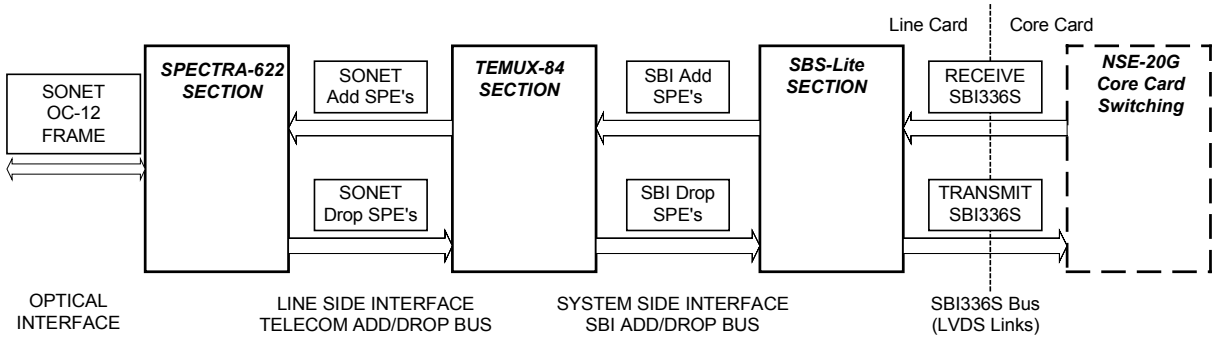
Figure 2 - OC-12 Line Card Block Diagram



A general data flow diagram for the OC-12 Line Card is shown in Figure 3. The following sections describe the receive and transmit data flows. The device functions described here are only a broad overview. Please refer to the product data sheets for a detailed description of each device's functionality.

The data flow description for this card uses T1 links as the data being transferred for an example of the capabilities. It supports a mix of T1s, E1s, TVT1.5s, TVT2s, DS3s, E3s, or fractional links. However, each SPE is restricted to carrying a single tributary type.

Figure 3 – OC-12 Line Card Data Flow



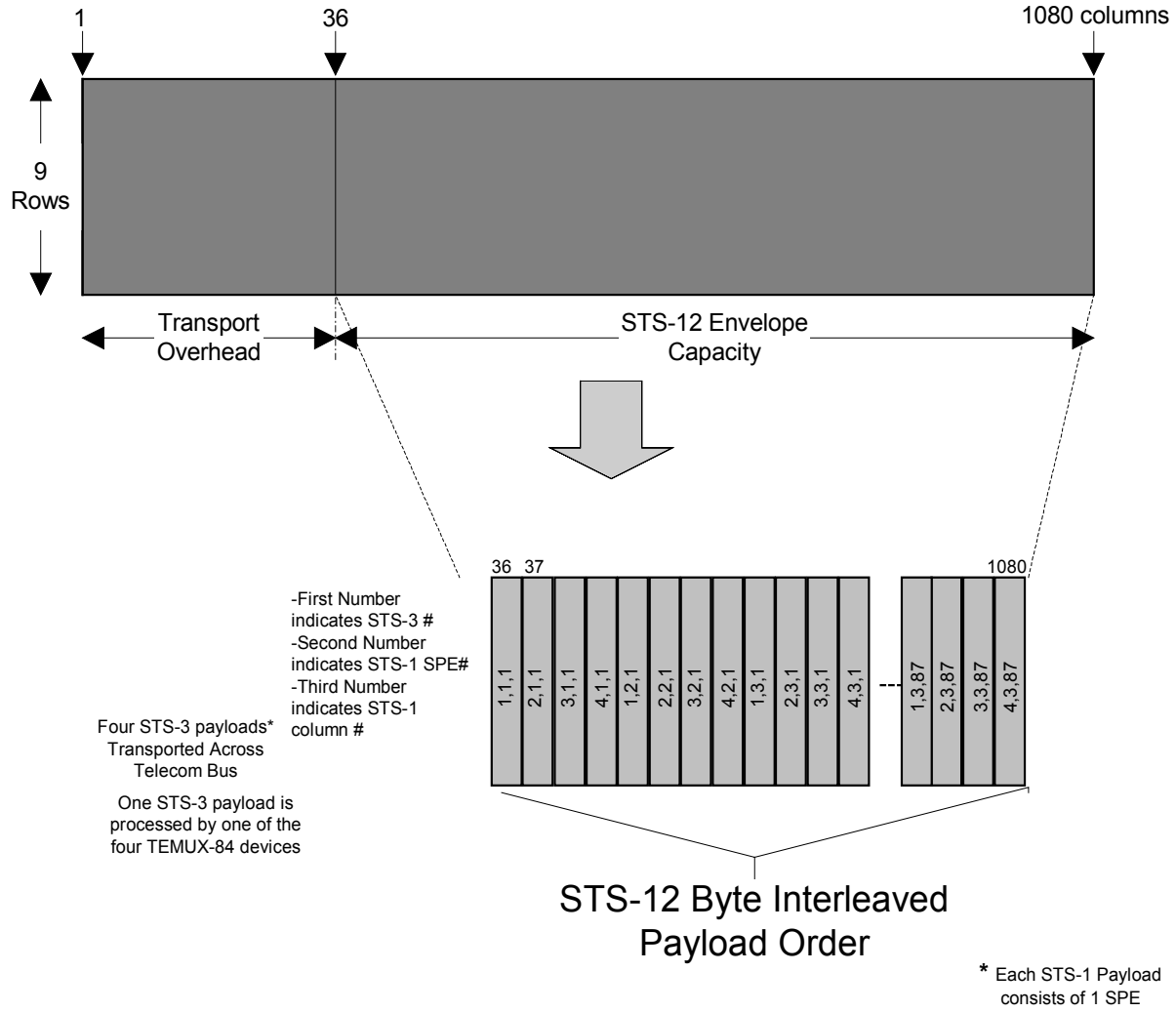
3.1.1 Upstream Data Flow

First, the optical receiver converts the OC-12 signal to an STS-12 electrical signal, and then the SPECTRA-622 recovers the clock from the serial data and converts the serial stream into a parallel format.

The SPECTRA-622 processes the section and line overhead of the SONET frame, then extracts the STS-12 Synchronous Payload Envelope.

The SPECTRA-622 is configured to extract the STS-12 payload from the receive stream and output it onto the 8-bit wide telecom drop bus. Each TEMUX-84 processes one STS-3 payload transmitted over the telecom bus by the SPECTRA-622. Figure 4 shows how the data is formatted as it is sent over the Telecom bus.

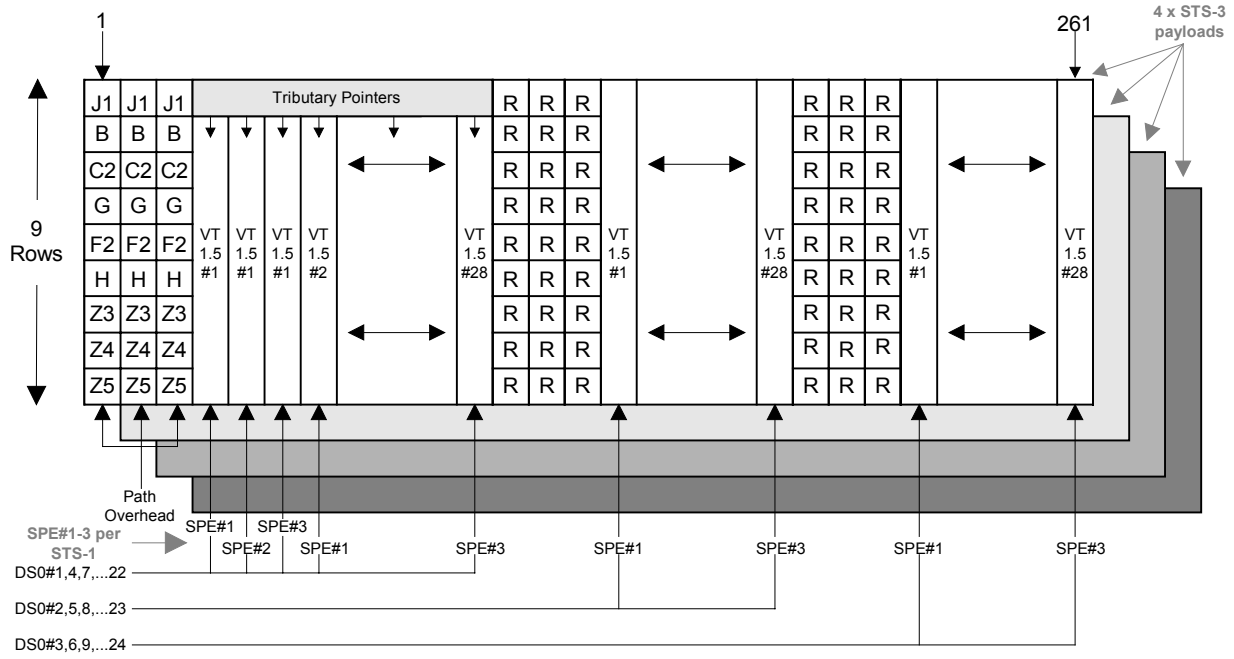
Figure 4 – Telecom Bus Data Format



Each TEMUX-84 demaps 84 SONET VT1.5 streams from one STS-3 payload. The VT1.5 structuring within the SPE is shown in Figure 5. After each T1 link is extracted from its respective VT1.5, the TEMUX-84 can frame to the common DS1 signal formats (SF, ESF) on each T1 link, or the framing can be bypassed in unframed mode.

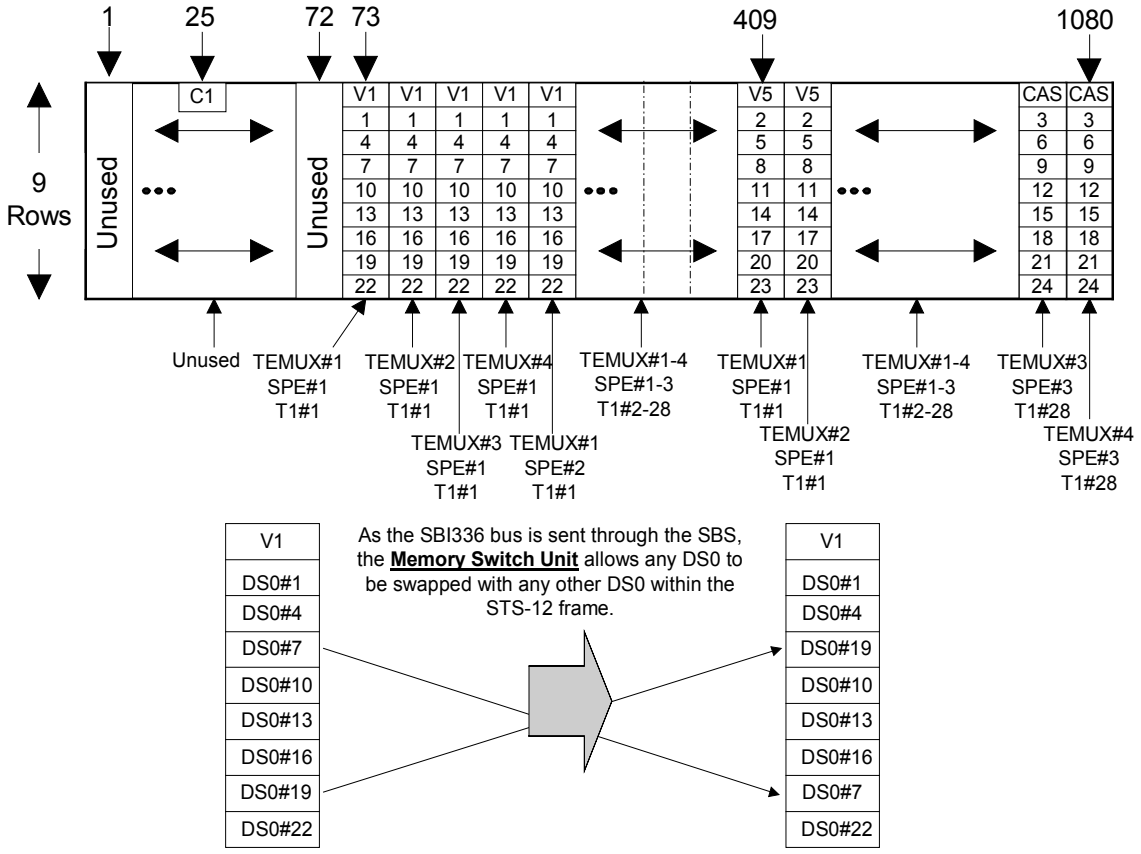
Each T1 framer supports performance monitoring and is independently software configurable. The host processor can access any T1 framer or transmitter on any of the TEMUX-84 devices.

Figure 5 – VT1.5 Demapping by the TEMUX-84



Each T1 is then byte-interleaved onto the SBI bus in the format shown in Figure 6. Note that the format used in the figure is representative of T1 streams being sent on the SBI bus. The format is slightly different for other data structures. For example, when sending DS3 or E3 data, SBI columns 60-72 are used.

Figure 6 – SBI336 Bus Data Format



As the SBS-Lite receives the data from the SBI Bus, it reads each DS0 into the Incoming Memory Switch Unit (IMSU). The Incoming Memory Switch Unit (IMSU) block has two connection memory pages and two data pages. The connection memory pages controls where each byte is switched and the alternating data pages fill up with one frame (9720 bytes) of data. The active page of the connection memory is controlled by the ICMP. When set to high, page 1 of the connection memory is active and when set to low, page 0 is active. The IMSU allows access to all DS0s within the STS-12 frame, so any DS0 can be swapped with any other DS0 within that frame.

The ICMP signal is controlled by the XC95288XL CPLD on the line card. In this system, the CPLD re-routes the ICMP signal received from the backplane or generates a signal depending on the values set in the SBS-Lite registers.

The data is then encoded using the 8B/10B format and is sent, using LVDS, over the backplane to a link layer device.

3.1.2 Downstream Data Flow

For this section of the data flow description, please refer to Figure 4 through Figure 6 for details.

In the downstream direction, the SBS-lite receives SBI336S data from the NSE via the backplane LVDS interface. The SBI336S data is decoded from 8B/10B format and then written into the OMSU of the SBS. The Outgoing Memory Switch Unit (OMSU) block has two connection memory pages and two data pages. The connection memory pages controls where each byte is switched and the alternating data pages fill up with one frame (9720 bytes) of data. The active page of the connection memory is controlled by the OCMP, which is generated by the CPLD or received from the backplane. When set to high, page 1 of the connection memory is active and when set to low, page 0 is active.

Each TEMUX-84 reads data from the SBI336 bus once every four SREFCLK cycles. When the TEMUX-84 is receiving data from the SBI336 bus, it uses the SAJUST_REQ signal to speed up, slow down, or maintain the rate at which the data is being transmitted. The SBS-Lite receives the JUST_REQ signal and passes it on to the link layer device, which appropriately changes the data rate.

Each TEMUX-84 processes the incoming data, recovering T1 clock and data for up to 84 links in framed or unframed mode. Please refer to Section 4.3 for a detailed description of the various framing formats that the TEMUX-84 supports. Each of the tributaries is then byte interleaved and sent to the SPECTRA-622 via the Telecom ADD Bus.

The SPECTRA-622 interprets the pointers bytes from all of the received STS-3s, then the path overhead from each SPE is processed. All four STS-3 payloads are then aligned to the frame of the transmit stream. The data is transformed into an STS-12 payload format. Line and the Path overhead are added to the payload to create a full STS-12 frame, which is mapped to the system timing reference. The full SONET STS-12 frame is then transmitted to the optical interface unit.

The transmitted signal is then converted to an OC-12 stream or optical format by the Optical Interface unit.

4 BLOCK DESCRIPTION

4.1 Optics

The HP HFCT-5208 optical transceiver performs the conversion between the optical OC-12 signal and the electrical STS-12 signal.

4.2 PM5313 SPECTRA-622

The PM5313 SONET/SDH PAYLOAD EXTRACTOR/ALIGNER (SPECTRA-622) terminates the transport and path overhead of STS-12 (STM-4/AU3 or STM-4/AU4) and STS-12c (STM-4-4c) streams at 622.08 Mbit/s. The SPECTRA-622 implements significant functions for a SONET/SDH compliant line interface, as well as DS3 mapping.

The SPECTRA-622 receives SONET/SDH frames via a bit serial interface, recovers clock and data, and terminates the SONET/SDH section (regenerator section), line (multiplexer section), and path. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section and line bit interleaved parity (BIP) (B1, B2), accumulating error counts at each level for performance monitoring purposes. B2 errors are also monitored to detect signal fail and signal degrade threshold crossing alarms. Line remote error indications (M1) are also accumulated. A 16 or 64 byte section trace (J0) message may be buffered and compared against an expected message. In addition, the SPECTRA-622 interprets the received payload pointers (H1, H2), detects path alarm conditions, detects and accumulates path BIPs (B3), monitors and accumulates path Remote Error Indications (REIs), accumulates and compares the 16 or 64 byte path trace (J1) message against an expected result and extracts the synchronous payload envelope (virtual container). All transport and path overhead bytes are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead, if desired.

The extracted SPE (VC) is placed on a Telecom DROP bus. In Telecombus applications, frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the received data stream and the DROP bus are accommodated by pointer adjustments in the DROP bus.

The SPECTRA-622 transmits SONET/SDH frames, via a bit serial interface, and formats section (regenerator section), line (multiplexer section), and path overhead appropriately. The SPECTRA-622 provides transmit path origination for a SONET/SDH STS-12 (STM-4/AU3 or STM-4/AU4) or STS-12c (STM-4-4c) stream. It performs framing pattern insertion (A1, A2), scrambling, alarm signal

insertion, and creates section and line BIPs (B1, B2) as required to allow performance monitoring at the far end. Line remote error indications (M1) are optionally inserted. A 16 or 64 byte section trace (J0) message may be inserted. In addition, the SPECTRA-622 generates the transmit payload pointers (H1, H2), creates and inserts the path BIP, optionally inserts a 16 or 64 byte path trace (J1) message, optionally inserts the path status byte (G1). In addition to its basic processing of the transmit SONET/SDH overhead, the SPECTRA-622 provides convenient access to all overhead bytes, which are inserted serially on lower rate interfaces, allowing additional external sourcing of overhead, if desired. The SPECTRA-622 also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors and BIP errors, which are useful for system diagnostics and tester applications.

On the OC-12 Line Card, the inserted SPE (VC) is sourced from a Telecombus ADD stream. For Telecombus applications, the SPECTRA-622 maps the SPE from a Telecom ADD bus into the transmit stream. Frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the transmit data stream and the ADD bus are accommodated by pointer adjustments in the transmit stream.

The SPECTRA-622 supports Time-Slot Interchange (TSI) on the Telecom ADD and DROP buses. On the DROP side, the TSI views the receive stream as twelve independent time-division multiplexed columns of data (i.e. twelve constituent STS-1 (STM-0/AU3) or equivalent streams or time-slots or columns). Any column can be connected to any time-slot on the DROP bus. Both column swapping and broadcast are supported. Time-Slot Interchange is independent of the underlying payload mapping formats. Similarly, on the ADD side, data from the ADD bus is treated as twelve independent time-division multiplexed columns. Assignment of data columns to transmit time-slots (STS-1 (STM-0/AU3) or equivalent streams) is arbitrary.

The SPECTRA-622 is implemented in low power, +3.3 Volt, CMOS technology. It has TTL and pseudo ECL (PECL) compatible inputs and outputs and is packaged in a 520 pin SBGA package.

4.3 PM8316 TEMUX-84

The High Density T1/E1 Framer with Integrated VT/TU Mappers and M13 Multiplexers (TEMUX-84) supports asynchronous multiplexing (demultiplexing) of 84 DS1s into (out of) three DS3 signals.

In the ingress direction, each of the 84 T1 links is either demultiplexed from a channelized DS3 or extracted from SONET VT1.5, TU-11 or TU-12 telecom mapped bus. Each T1 framer can be configured to frame to the common DS1

signal formats (SF, ESF) or to be bypassed (unframed mode). Each T1 framer detects and indicates the presence of Yellow and AIS patterns and also integrates Yellow, Red, and AIS alarms.

In the egress direction, framing is generated for 84 T1s into either a DS3 multiplex or a SONET/SDH mapped add bus. Each T1 transmitter frames to SF or ESF DS1 formats, or framing can be optionally disabled. The TEMUX-84 supports signaling insertion, idle code substitution, data insertion, line loopback, data inversion and zero-code suppression on a per-DS0 basis. PRBS generation or detection is supported on a framed and unframed T1 basis.

A Scaleable Bandwidth Interconnect (SBI) high density byte serial system interface provides higher levels of integration and dense interconnect. The SBI bus interconnects up to 84 T1s or 63 E1 EITHER synchronously or asynchronously. The SBI allows transmit timing to be mastered by either the TEMUX-84 or link layer device connected to the SBI bus. In addition to framed T1s and E1s, the TEMUX-84 can transport unframed T1 or E1 links and framed or unframed DS3 or E3 links over the SBI bus. This reference design utilizes a byte wide SBI bus running at 77.76 MHz.

4.4 PM8611 SBS-Lite

The PM8611 **S**BI336 **B**us **S**erializer (SBS-Lite) is a monolithic integrated circuit that implements conversion between byte-serial 77.76 MHz SBI336 bus and redundant 777.6 Mbps bit-serial LVDS links. In SBI bus mode the SBS-Lite implements conversion between 77.76 MHz SBI336 bus format and redundant 777.6 Mbps bit-serial 8B/10B-base serial SBI336S bus format. In line with the bus conversion is a DS0 granular switch allowing any input DS0 to be output on any output DS0.

The SBS-Lite can be used to connect and switch high density T1/E1 framer devices supporting an SBI bus with link layer devices supporting an SBI bus over a serial backplane. Putting the Narrowband Switch Element, NSE, between the framer and link layer devices allows construction of up to 20Gb/s NxDS0 switches.

In the ingress direction, the SBS-lite connects an incoming 77.76MHz SBI336 stream to a pair of redundant serial SBI336S LVDS links through a DS0 memory switch. In telecom bus mode an incoming 77.76MHz telecom bus that has the J1 path fixed and all high order pointer justifications converted to tributary pointer justifications can be switched through a VT granular switch to a pair of redundant serial LVDS telecom bus format links. The incoming data is encoded into an extended set of 8B/10B characters and transferred onto two redundant 777.6 Mbps serial LVDS links. SBI or telecom bus frame boundaries, pointer justification events and master timing controls are marked by 8B/10B control

characters. Incoming SPEs may be optionally overwritten with the locally generated $X^{23} + X^{18} + 1$ PRBS pattern for diagnosis of downstream equipment. The PRBS processor is configurable to handle any combination of SPEs and can be inserted independently into either of the redundant LVDS links. A DS0 memory switch provides arbitrary mapping of streams on the incoming SBI336 bus stream to the working and protect LVDS links at DS0 granularity. In telecom bus mode a VT1.5/VT2 memory switch provides arbitrary mapping of tributaries on the incoming telecom bus stream to the working and protect LVDS links. Multi-cast is supported.

In the egress direction, the SBS-lite connects two independent 777.6 Mbps serial LVDS links to an outgoing SBI336 Bus. Each link contains a constituent SBI336S stream. Bytes on the links are carried as 8B/10B characters. The SBS-lite decodes the characters into data and control signals for a single 77.76MHz SBI336 bus. Alternatively the SBS-lite decodes two independent 777.6 Mbps telecom bus formatted serial LVDS links characters into a single 77.76MHz telecom bus. A pseudo-random bit sequence (PRBS) processor is provided to monitor the decoded payload for the $X^{23} + X^{18} + 1$ pattern in each SPE. The PRBS processor is configurable to handle any combination of SPEs in the serial LVDS link. Data on the outgoing SBI336 bus stream may be sourced from either of the LVDS links.

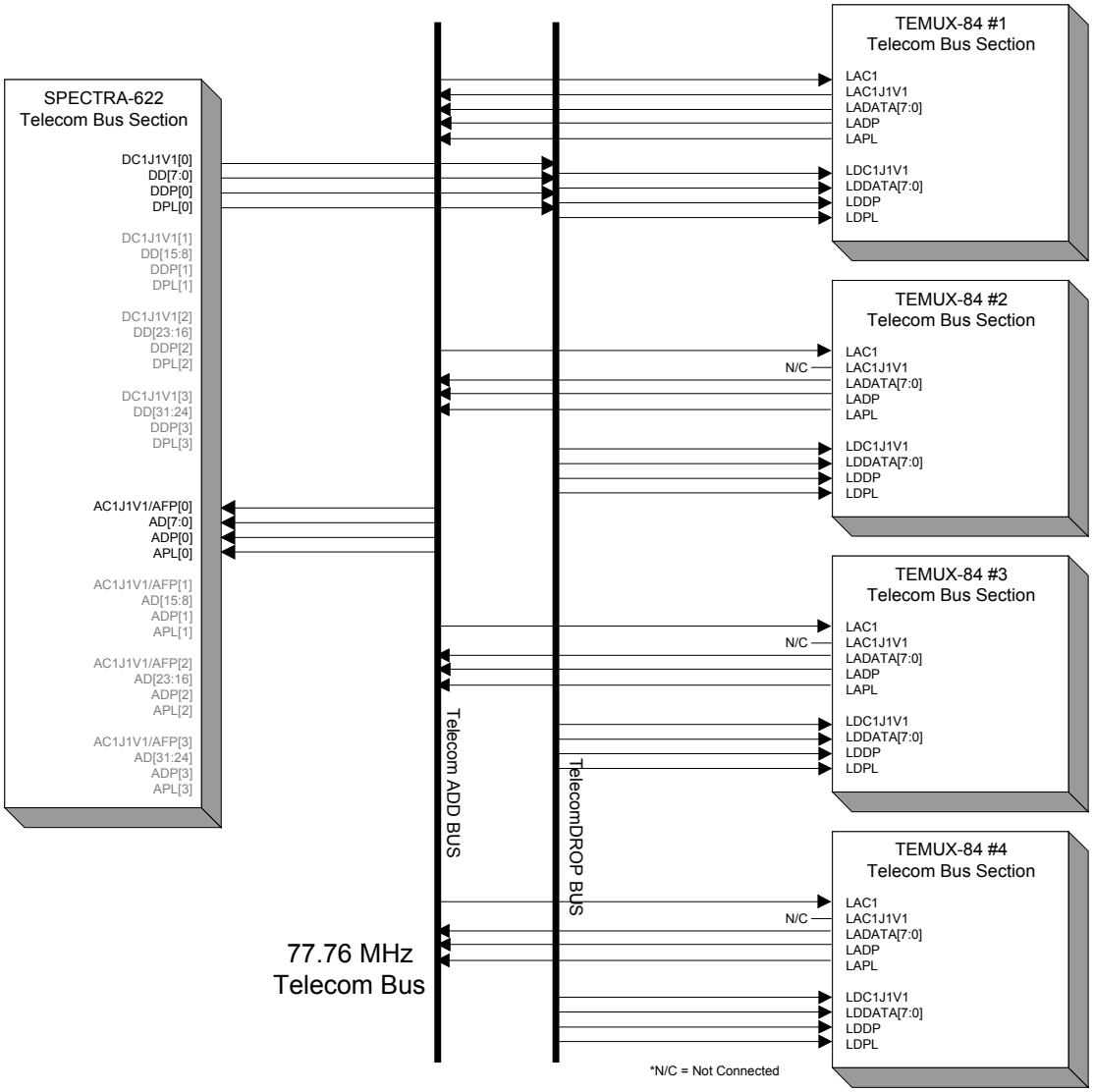
An In-band signaling link over the serial LVDS links allows this device to be controlled by a companion switching device, the Narrowband Switching Element, NSE20G. This link can be used as communication link between a central processor and the local microprocessor.

4.5 Telecom Bus Interface

The Telecom bus consists of an 8-bit wide interface that transports data between the SPECTRA-622 and the TEMUX-84 devices. In this application, the telecom bus runs at 77.76 MHz. The data is in the form of four interleaved STS-3 Payloads while on the bus, as show in Figure 4. Each TEMUX-84 has an 8-bit wide Telecom bus interface and receives one of the four STS-3 payloads from the SPECTRA-622. Only one TEMUX-84 needs to drive the LAC1J1V1 signal to the SPECTRA-622. All other TEMUX-84s must be configured via the TXPTR[9:0] bits, in the SONET/SDH Transmit Pointer Configuration Register, to use the same J1 offset.

A 77.76 MHz reference clock supplies the system clock for the bus. The LAC1 and DFP signals are generated by the CPLD.

Figure 7 – SPECTRA-622 to TEMUX-84 Telecom Bus Interface



4.6 SBI Bus Interface

The Scaleable Bandwidth Interconnect (SBI) bus provides an interface for the interconnection of asynchronous and synchronous multi-port physical interface devices with multi-channel and multi-function link layer devices.

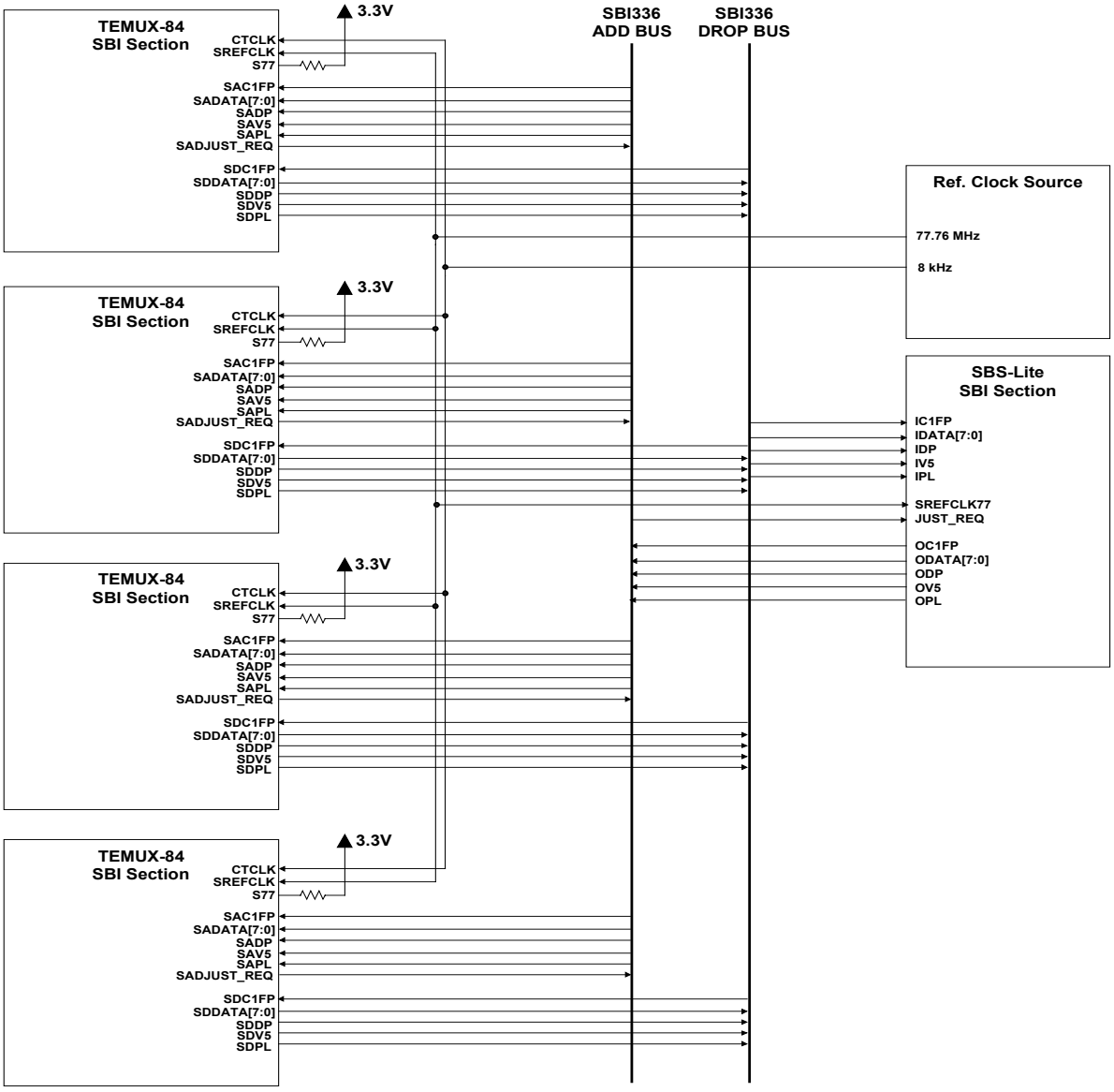
The OC-12 Line Card implements a SBI336 bus configuration. The bus will run at 77.76 MHz and is exactly four 19.44 MHz SBI buses byte-interleaved together. Since each device on the bus has its own timeslot, no capabilities for bus collision detection are required.

The I/O SDC1FP signal is used to indicate SBI bus multiframe alignment. The signal is supplied to the drop bus by the CPLD, rather than the TEMUX-84s directly driving this signal.

The OC1FP[1] signal from the SBS-Lite drives the SAC1FP signal. This signal also indicates the multiframe alignment which occurs every 4 frames, therefore this signal is pulsed every fourth octet to produce a 2kHz multiframe signal. See Section 4.10 for further details regarding frame pulses.

See Figure 8 for a detailed diagram of the connections between the TEMUX-84s and SBS-Lite.

Figure 8 – TEMUX-84 to SBS-Lite SBI336 Interface



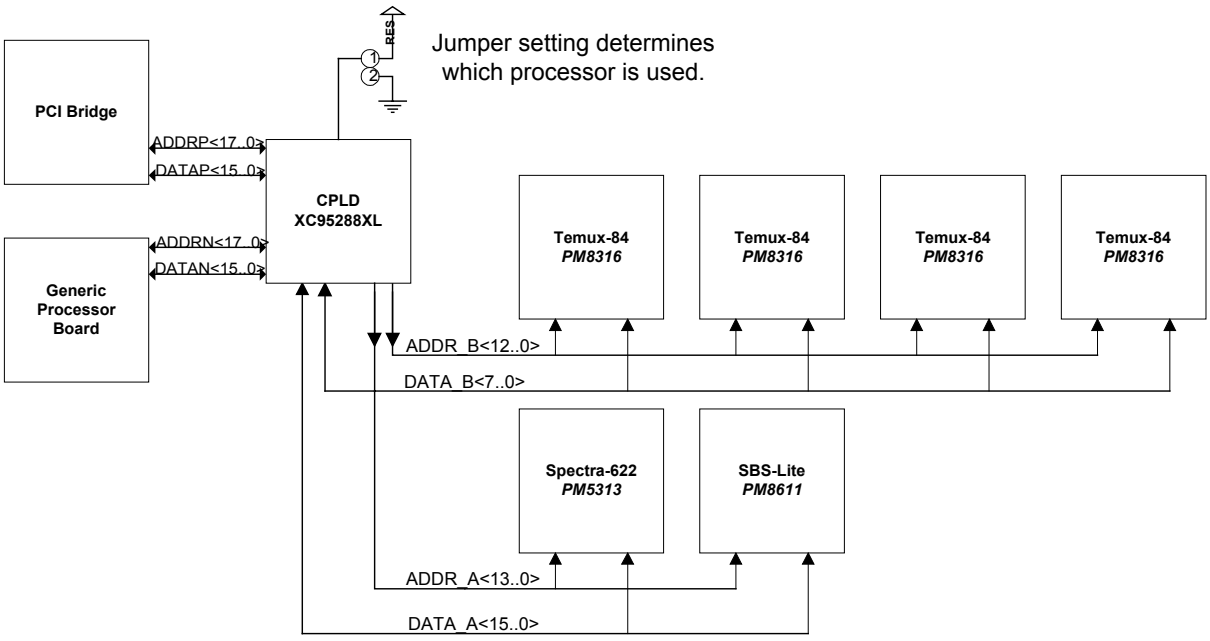
4.7 Microprocessors Interface

The board has been designed with two possible processor interfaces. One is an external processor that uses a PCI Bridge to access devices and the other is an onboard generic processor. The OC-12 Line Card switches between the two interfaces by setting a specified pin on the CPLD to either a logic high or low.

Set the pin to high when using the PCI Bridge interface and low when using the generic processor interface. See Table 27 for detailed pin settings.

Figure 9 demonstrates the board architecture.

Figure 9 – Microprocessor Interface Topology



4.7.1 CompactPCI Bridge

The host processor will access the devices on the line card via the CompactPCI interface. The card uses a PCI Bridge and various decode logic inside a CPLD so that all registers on each of the devices are accessible.

The PCI Bridge used is the PLX Technology PCI9030 PCI Bus Target Interface Chip. The PCI9030 provides a target only interface, and as such does not initiate PCI bus transactions.

Not all of the devices on the microprocessor bus have sufficient output drive to properly drive the bus. Therefore the CPLD creates two individual Data and Address buses, effectively splitting the bus into two sections. This split allows each device to correctly drive their section of the bus. Figure 9 above shows an overview of the bus topology.

The PCI9030 is configured for single read/write operation. Burst read/write operation is not supported by any devices on the line card. The local address space is configured to be 32-bit non-multiplexed, big endian, and non-prefetchable. Although most devices on the line card have only an 8-bit or 16-bit data bus, the PCI9030 is configured to use a 32-bit data bus. This was done to simplify the hardware design. Prefetching is not possible in this application because the line card has a number of registers with read side affects (e.g. interrupt status registers).

The local bus is clocked at 33MHz by looping the buffered PCI clock output (BCLKO) available from the PCI9030 back to the local bus clock input. The PCI9030 is 5V tolerant, so there is no need for level conversion when accessing a 5V PCI bus.

The local address spaces are allocated in the following fashion:

Table 1 PCI9030 Local Address Space Allocation

Address Space	Function
0	Spectra-622
1	TEMUX-84 (CPLD will decode addresses for each)
2	SBS-Lite
3	CPLD internal registers

Please refer to the PCI9030 datasheet [4] for more information.

4.7.1.1 SEEP

The NM93CS56 Serial EEPROM from National Semiconductor is used to store configuration information for the PCI9030 Bridge. This specific SEEP (or equivalent) is required by PCI9030 because it supports sequential read operations.

Refer to the PCI9030 datasheet [4] for information on the format of the configuration data stored in the SEEP.

4.7.2 Generic Onboard Processor

The OC12 Line Card is equipped with a generic onboard processor can be used to provide read and write operations. The local processor bus allows direct connection to memory and peripheral devices.

The generic processor must provide the following minimum requirements:

- 18 bit address bus and a 16 bit data bus
- Two chip selects. The CPLD will further decode the address bits so the microprocessor can individually read and write from any device.
- Runs from either a 3.3V and/or 1.8 V source.
- Single interrupt line.
- An Ethernet or serial interface to allow direct access to the onboard processor from an host computer.

As in the case of the PCI9030, the microprocessor bus does not have sufficient output drive to properly drive the bus to each device. Therefore the Address and Data signals are driven twice by the CPLD, effectively splitting up the bus. Figure 9 shows an overview of the bus topology.

A generic processor with two chip select lines would allocate the local address spaces in the following fashion:

Table 2 Local Address Space Allocation

Address Space	Function
CS0	Spectra-622, SBS-Lite
CS1	TEMUX-84 (1,2,3 & 4)

Further decoding is required by the CPLD in order to target each individual device.

4.8 Power Supply

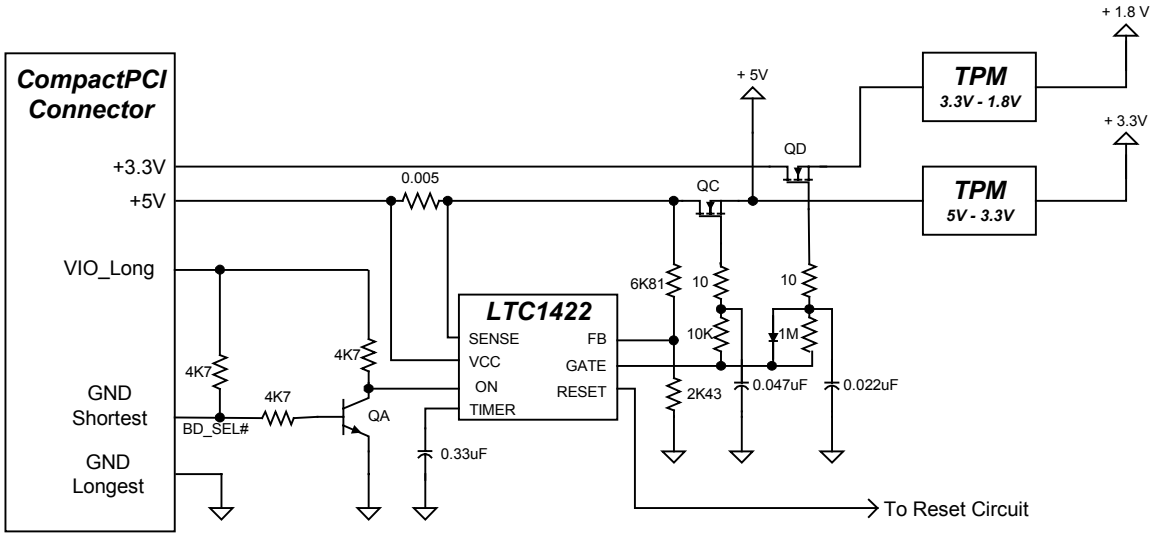
The OC-12 Line Card reference design contains components that operate at 1.8V and 3.3V, referenced to ground. The 5V and 3.3V supplies are provided to the board through the CompactPCI connector from the backplane. The 1.8V and 3.3V supplies are generated from onboard power modules.

4.9 Hot Swap

The Line Card has been designed to be hot-swap compatible. The Hot Swap Specification [2] says - “The basic purpose of the Hot Swap addition to CompactPCI is to allow the orderly insertion and extraction of boards without adversely affecting system operation.”

The Line Card employs a hot swap compatible cPCI bridge, PLX PCI9030, and a hot swap controller, the Linear Technology LTC1422. The cPCI connector is assembled with three different length pins, as required by the hot swap specification [2]. An example of the hot swap circuit is shown in Figure 10 below.

Figure 10 - Example of a Hot Swap Circuit



4.10 Clocks and Oscillators

A 77.76 MHz ± 20ppm PECL oscillator is required on the card to drive the SPECTRA-622 receive section.

A 37.056 MHz ± 32ppm oscillator is required on the card to drive the digital phase locked loop on the TEMUX-84s that perform jitter attenuation on the T1 recovered clocks.

A 51.84 MHz ± 50ppm oscillator is required on the TEMUX-84s to generate a gapped DS3 clock when demapping a DS3 from the SONET stream and for receiving a DS3 from the SBI bus interface.

A 44.736 MHz ± 32ppm oscillator is required for mapping of DS3s onto the Telecom Bus.

A 49.152 MHz ± 32ppm oscillator is required on the card to drive the digital phase locked loop on the TEMUX-84s that perform jitter attenuation on the E1 recovered clocks.

A 77.76 MHz clock will be used to drive the SBI336 Bus and the Telecom bus. The clock must have between 40%-60% duty cycle. The CPLD will also divide this signal by 9720 to generate the 8 kHz synchronization pulse (CTCLK) and other framing pulses. From the onboard oscillators the CTCLK signal is then divided by 4 to generate the 2 kHz synchronization pulses (DFP/LAC1) and other framing pulses. The 77.76 MHz can be attained from the following three sources.

- Backplane reference clock.
- Local clock source.
- External clock source.

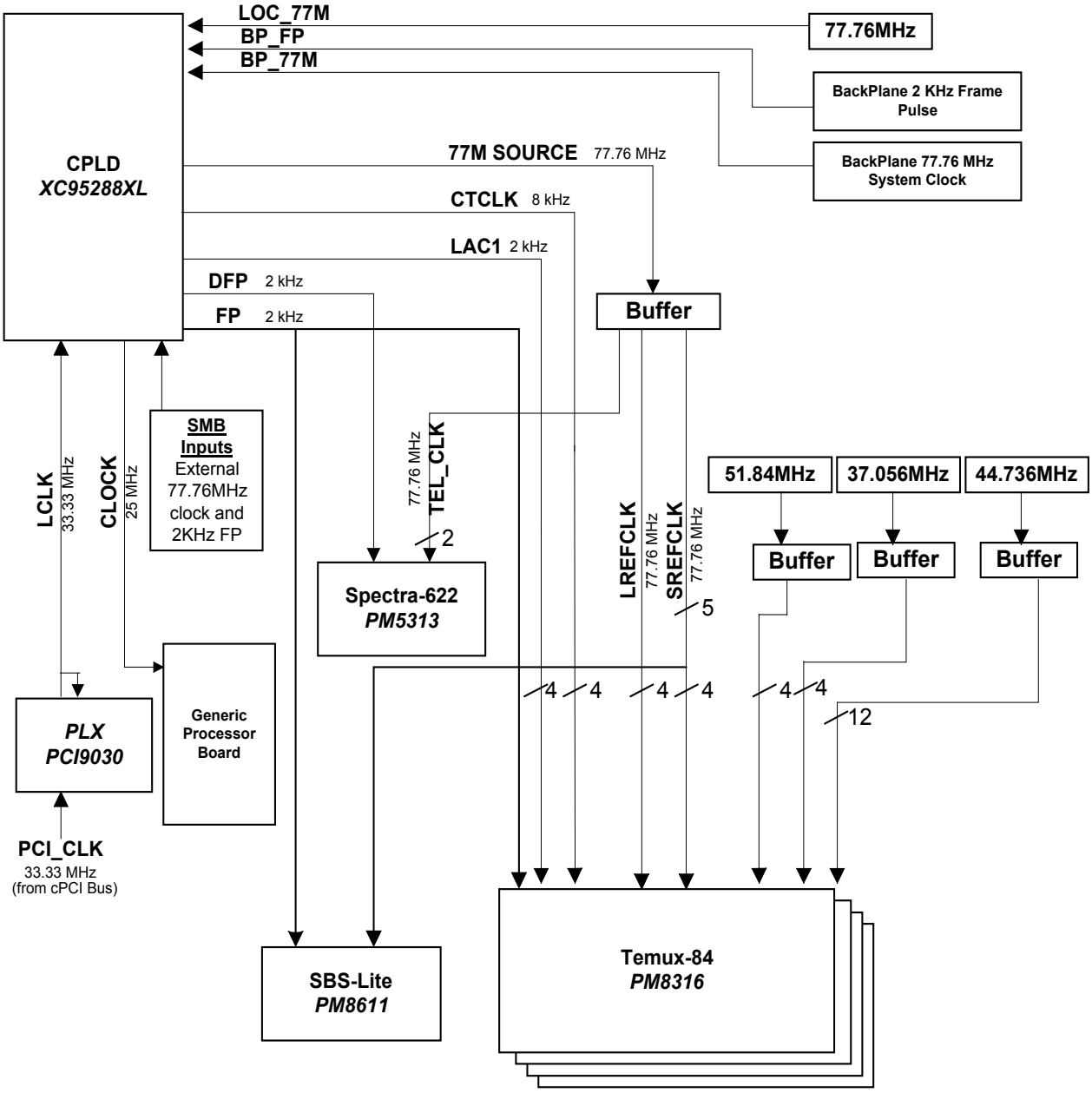
All three 77.76 MHz sources are fed into the CPLD. The CPLD has jumpers that are set to one of the sources.

As the 77.76 MHz reference clock, the board can attain a 2 kHz framing pulse from the same three sources listed above. All three 2 kHz sources are fed into the CPLD. The CPLD has jumpers that are set to one of the sources. See Table 27 for details on the CPLD pin settings.

The two SMB connector that are connected to the CPLD are used for receiving synchronization or clock signals from an external source. The OC-12 line card can receive a 77.76 MHz clock and a 2 kHz frame pulse from an external source.

Most clocks that are connected to more than one device are fed through a clock buffering device. The OC-12 Line Card uses several Pericom PI49FCT3805 clock buffers, combined with series termination resistors, to ensure that a clean, fast clock signal is provided to all devices. A diagram showing the major clock distribution networks on the card are shown below in Figure 11.

Figure 11 - Clock Distribution



5 DESIGN ISSUES

5.1 Power Supply

5.1.1 Decoupling

The power modules used require proper input and output decoupling. Refer to section 6.2.1 for details about the Power Module.

The analog power supply pins require a filtering network between the ground plane and the power plane. This filtering method should be used when supplying analog power to both 1.8V and 3.3V devices. Please refer to Appendix A: Bill of Materials for component values.

5.1.2 Power-Up Sequence

The power up sequence must be adhered to, otherwise device latch-up can occur. The power supplies must turn on in the following sequence:

1. 5V Power
2. 3.3V Digital Power
3. 3.3V Analog Power
4. 1.8V Digital Power
5. 1.8V Analog Power

The power down of the card must be performed in the reverse sequence.

The delaying of the 1.8V digital power versus the 3.3V digital power is the critical factor since 1.8V is the core supply voltage for some of the devices and must come up after the 3.3V I/O supply voltage. The delaying of analog supplies to come up after its digital counterpart is easily accomplished by the analog supply filtering components. Since it takes time to charge the filter capacitors, the charging delays the analog supply rail a reasonable amount of time for the digital power to stabilize.

If the simple solution of a filtering network cannot be implemented, then the analog power pins should be current limited to the maximum latch-up current of 100mA while the digital power stabilizes.

5.2 SPECTRA-622 Design Considerations

Provide separate +3.3V analog transmit, +3.3V analog receive, and +3.3V digital supplies. Connect the supplies together at one point close to the +3.3V output of the power supply.

High-frequency decoupling capacitors are required to prevent the transmitter from coupling noise into the receiver and to prevent transients from coupling into the reference circuitry.

BIAS voltages (VBIAS and PBIAS) must be applied before VDD or simultaneously with VDD to prevent current flow through the ESD protection devices that exist between BIAS and VDD power supplies.

5.3 TEMUX-84 Design Considerations

The clock signals XCLK_T1 and DS3_REF signals must be carefully routed from the clock buffers to the TEMUX-84 parts. The lines should be properly terminated and should not run near any of the data busses if possible.

5.4 SBS-Lite Design Considerations

The SBS-Lite should be placed so that there are no major components between the SBS-Lite and the backplane connector. The LVDS links should be able to be routed in the shortest distance possible to the backplane.

The length of the traces in each of the LVDS line pairs should be matched in order to minimize skew. Skew between the signals of a pair means a phase difference between signal. This destroys the magnetic field cancellation and results in EMI. Therefore the pair lengths should be matched within 100 mils.

5.5 Telecom and SBI Bus Design Considerations

Each signal on the busses requires adequate termination to prevent reflections. At each point where a bus line connects to a driving device, a series resistor should be placed on the line. The value should be large enough to reduce ringing and reflections, but not too large, as it would impair the drive capability of the output. The MICTOR connectors that are used to monitor the signals on these busses should be placed in such a way to minimize trace length between all points on the bus. However, the spacing around the connectors must allow for the special MICTOR pin adapter boards to be plugged in without physical interference between adjacent connectors.

Any multipoint bus that has tristate ability should have pull-up resistors to avoid the bus floating to unknown levels when not being driven. A suitable pull-up value is 10K.

On the OC-12 Line Card both the Telecom bus and SBI bus run at 77.76 MHz 8-bit busses.

5.6 PCI Bridge Design Considerations

During power up, the PCI RST# signal resets the default values of the PCI 9030 internal registers. In return, the PCI 9030 outputs the local reset signal (LRESET#) and checks for the existence of the serial EEPROM. If a serial EEPROM is installed, and the first 16-bit word is not FFFF, the PCI 9030 initializes the internal registers from the serial EEPROM. Otherwise, default values are used. The PCI 9030 configuration registers can only be written by the optional serial EEPROM or the PCI host processor. During the serial EEPROM initialization, the PCI 9030 response to PCI target accesses is RETRYs.

6 ANALYSIS

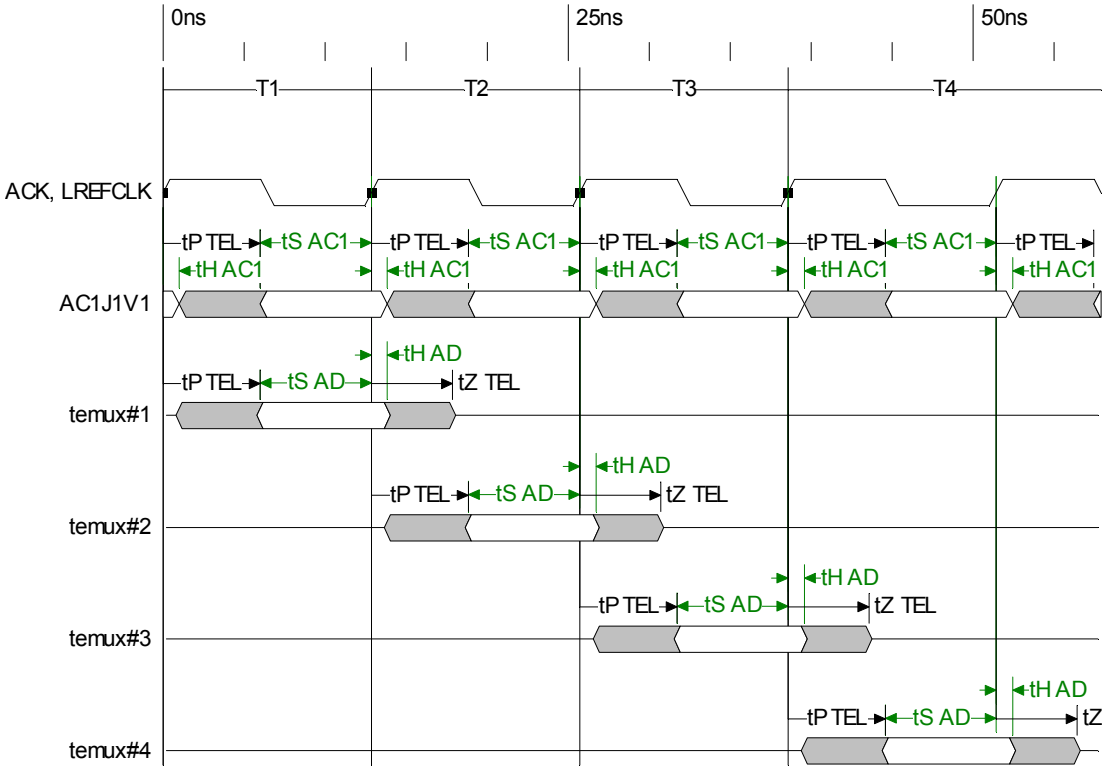
6.1 Timing

In the timing analysis figures of this section, a gray waveform indicates uncertainty, and a black waveform indicates an input that is not valid since more than one device may be driving the signal at that time. **All times are measured in nanoseconds. (ns)**

6.1.1 SPECTRA-622 – TEMUX-84 Telecom Bus Interface

The telecom bus is a synchronous interface that carries SPE data between the SPECTRA-622 and the four TEMUX-84 devices. The telecom bus is synchronized to a 77.76 MHz clock source. The AC1J1V1 signal is sampled on the rising edge of LREFCLK and indicates frame, payload and tributary multiframe boundaries. See Figure 12 below for a diagram of the Telecom Add bus timing and Figure 13 for the drop bus timing.

Figure 12 – Telecom ADD Bus Timing Diagram



In reference to Figure 12, the sequence of events for one Telecom ADD bus clock cycle is as follows:

1. On the rising edge of LREFCLK, at the start of T1, the first TEMUX-84 drives valid data onto the Telecom Add bus after the propagation delay tP TEL.

2. On the rising edge of LREFCLK, at the start of T2, the SPECTRA-622 samples the data from the Telecom Add bus and the first TEMUX-84 has a delay of tZ TEL before tristating. All Telecom Add bus signals require that the bus data be valid during setup time, tS AD, and hold time, tH AD. Also at the start of T2, TEMUX-84 #2 drops valid data onto the Telecom Add bus.

3. At the start of T3, TEMUX-84 #3 uses the Telecom Add bus and at the start of T4, TEMUX-84 #4 uses the Telecom Add bus. The cycle repeats with each TEMUX-84.

The output propagation delays involved in Figure 12 are shown in the following table:

Table 3 Telecom Add Bus Propagation Delays

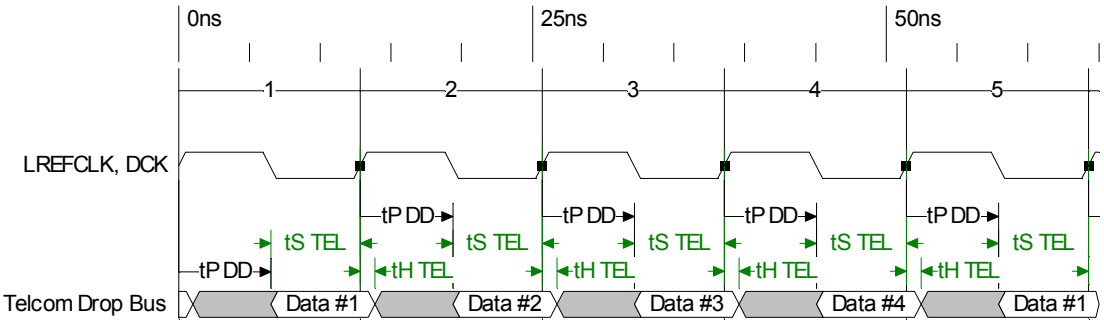
Name	Device	Description	Min	Max
tP TEL	TEMUX-84	LREFCLK to TEMUX-84 Outputs going Valid from Tristate	1	6
tZ TEL	TEMUX-84	Time to Data tristating again	1	5

The input constraints involved in Figure 12 are shown in the following table:

Table 4 Telecom Add Bus Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS AC1	SPECTRA-622	Telecom Bus Set-up Time	3.5	6.86	3.36
tS AD	SPECTRA-622	Telecom Bus Set-up Time	3.5	6.86	3.36
tH AC1	SPECTRA-622	Telecom Bus Hold Time	1	1	0
tH AD	SPECTRA-622	Telecom Bus Hold Time	1	1	0

Figure 13 – Telecom DROP Bus Timing Diagram



In reference to Figure 13, the sequence of events for one Telecom Drop bus clock cycle is as follows:

1. On the rising edge of LREFCLK, at the start of T1, the Telecom Drop bus is updated by the first valid data output of the SPECTRA-622, after the propagation delay tP DD.

2. On the rising edge of LREFCLK, at the start of T2, the TEMUX-84 samples the data from the Telecom Drop bus. All Telecom Drop signals require that the bus data be valid during setup time tS TEL and hold time tH TEL.

The output propagation delays involved in Figure 13 are shown in the following table:

Table 5 Telecom Drop Bus Propagation Delays

Name	Device	Description	Min	Max
tP DD	SPECTRA-622	Propagation delay of LREFCLK to SPECTRA-622 Outputs going Valid	1	6.5

The input constraints involved in Figure 13 are shown in the following table:

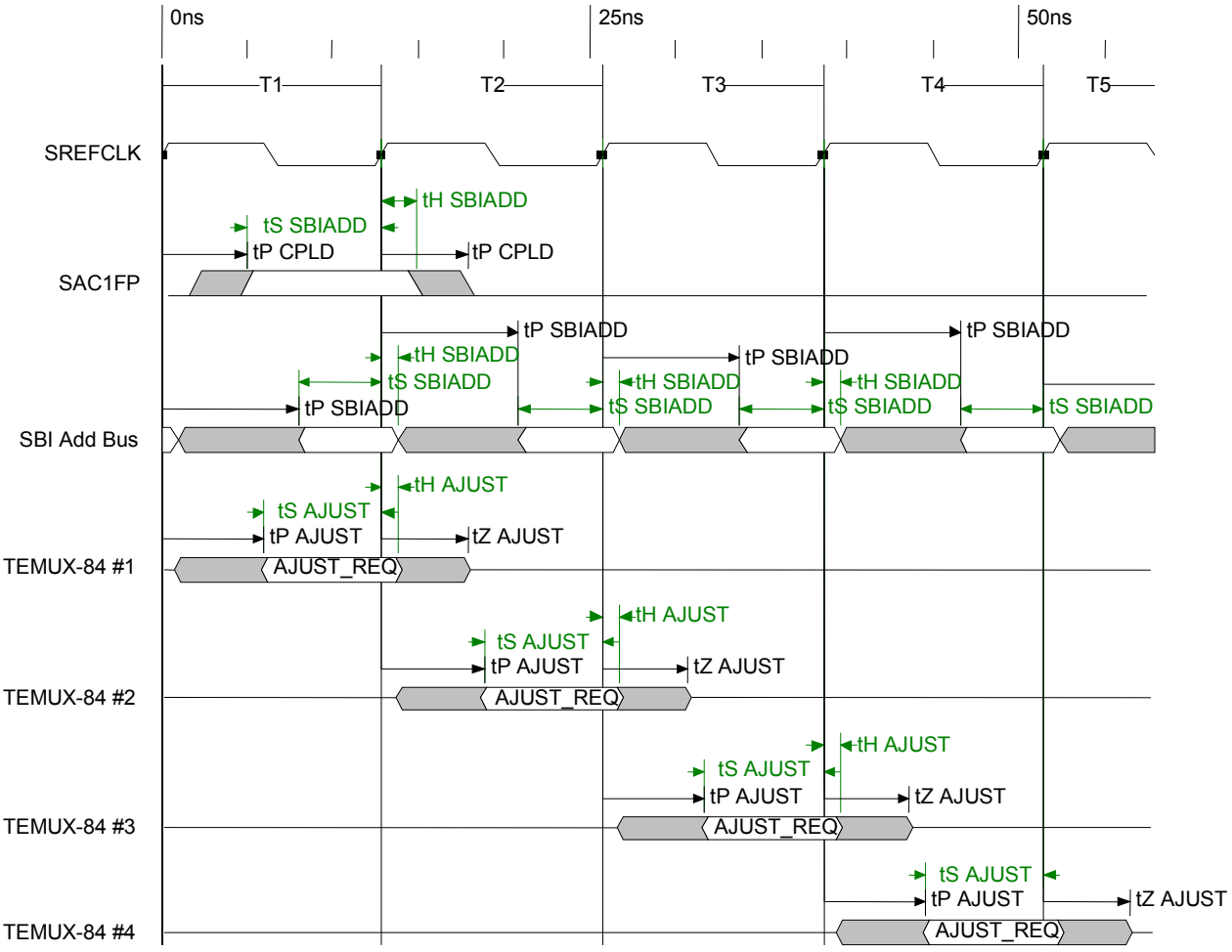
Table 6 Telecom Drop Bus Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS TEL	TEMUX-84	Telecom Bus Set-up Time	3	6.36	3.36
tH TEL	TEMUX-84	Telecom Bus Hold Time	0	1	1

6.1.2 TEMUX-84 – SBS-Lite SBI336 Interface

The SBI336 bus is a synchronous interface that carries data between the four TEMUX-84 devices and the SBS-Lite. The SBI336 bus is synchronized to a 77.76 MHz clock source. See Figure 14 below for a diagram of the SBI Add bus timing and Figure 15 for the Drop bus.

Figure 14 – SBI ADD Bus Timing Diagram



In reference to Figure 14, the sequence of events for one SBI Add bus clock cycle is as follows:

1. On the rising edge of SREFCLK, at the start of T1, all signals on the SBI Add bus are updated by the SBS-Lite outputs after the propagation delay tP SBIADD.

2. Also, on the same edge of SREFCLK, the SAC1FP pulse is pulsed once every four frames or 4 x 9720 SREFCLKs, after a propagation delay of tP CPLD.

3. The AJUST_REQ signal is asserted by each TEMUX-84 to control the data rate of the Link Layer Device. The AJUST_REQ signal comes out of tristate after a delay of tP AJUST and returns to tristate on the next clock cycle, after a delay of tZ AJUST.

4. On the rising edge of SREFCLK, at the start of T2, the TEMUX-84 samples the data from the SBI Add bus and the SAC1FP input. All TEMUX-84 SBI inputs require that the data be valid during setup time tS SBIADD and hold time tH SBIADD.

5. Also, on the same edge of SREFCLK, the SBS-Lite samples the AJUST_REQ signal. The AJUST_REQ input requires a setup time of tS AJUST and a hold time tH AJUST.

The output propagation delays involved in Figure 14 are shown in the following table:

Table 7 SBI Add Bus Propagation Delays

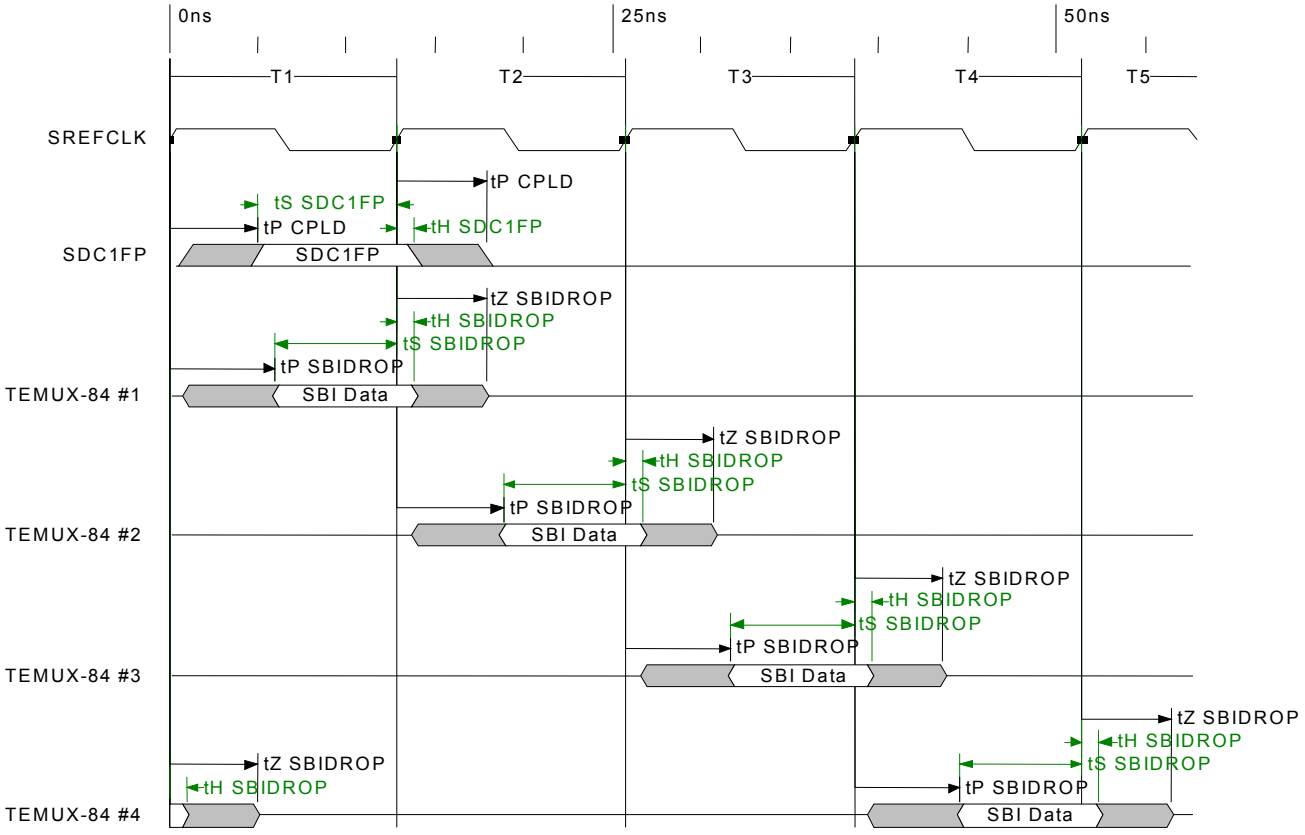
Name	Device	Description	Min	Max
tP SBIADD	SBS	Propagation delay of SREFCLK to SBS-Lite Outputs going Valid	1	7
tP AJUST	TEMUX-84	Propagation delay of SREFCLK to TEMUX-84 Output going Valid	1	6
tZ AJUST	TEMUX-84	Propagation delay of SREFCLK to TEMUX-84 Output going to tristate	1	5
tP CPLD	CPLD	Propagation delay of SREFCLK to TEMUX-84 Output going Valid	1	7

The input constraints involved in Figure 14 are shown in the following table:

Table 8 SBI Add Bus Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS SBIADD	TEMUX-84	TEMUX-84 input setup time	3	5.86	2.86
tH SBIADD	TEMUX-84	TEMUX-84 input hold time	0	1	1
tS AJUST	SBS-Lite	SBS-Lite input setup time	3	6.86	3.86
tH AJUST	SBS-Lite	SBS-Lite input hold time	0	1	1

Figure 15 – SBI DROP Bus Timing Diagram



In reference to Figure 15, the sequence of events for one SBI DROP bus clock cycle is as follows:

1. On the rising edge of SREFCLK, at the start of T1, The TEMUX-84 #1 puts valid data onto the SBI drop bus after the propagation delay tP SBIDROP.

2. On the rising edge of the T2 cycle, the SBS-Lite samples the data from the drop bus. The SBS-Lite requires a set-up time of tS SBIDROP and a hold time of tH SBIDROP to read the data. After the tZ SBIDROP delay, the TEMUX-84 #1 tristates its outputs, and TEMUX-84 #2 begins writing to the bus after a delay of tP SBIDROP.

3. The above steps are repeated for each of the four TEMUX-84s that can drive the data and control signals. When TEMUX #n is not driving the signals, its telecom ADD bus outputs are in a high impedance state.

The output propagation delays involved in Figure 15 are shown in the following table:

Table 9 SBI DROP Bus Propagation Delays

Name	Device	Description	Min	Max
tP CPLD	CPLD	SREFCLK to data output delay	1	5
tP SBIDROP	TEMUX-84	SREFCLK to data valid delay	1	6
tZ SBIDROP	TEMUX-84	SREFCLK to data tristate delay	1	5

The input constraints involved in Figure 15 are shown in the following table:

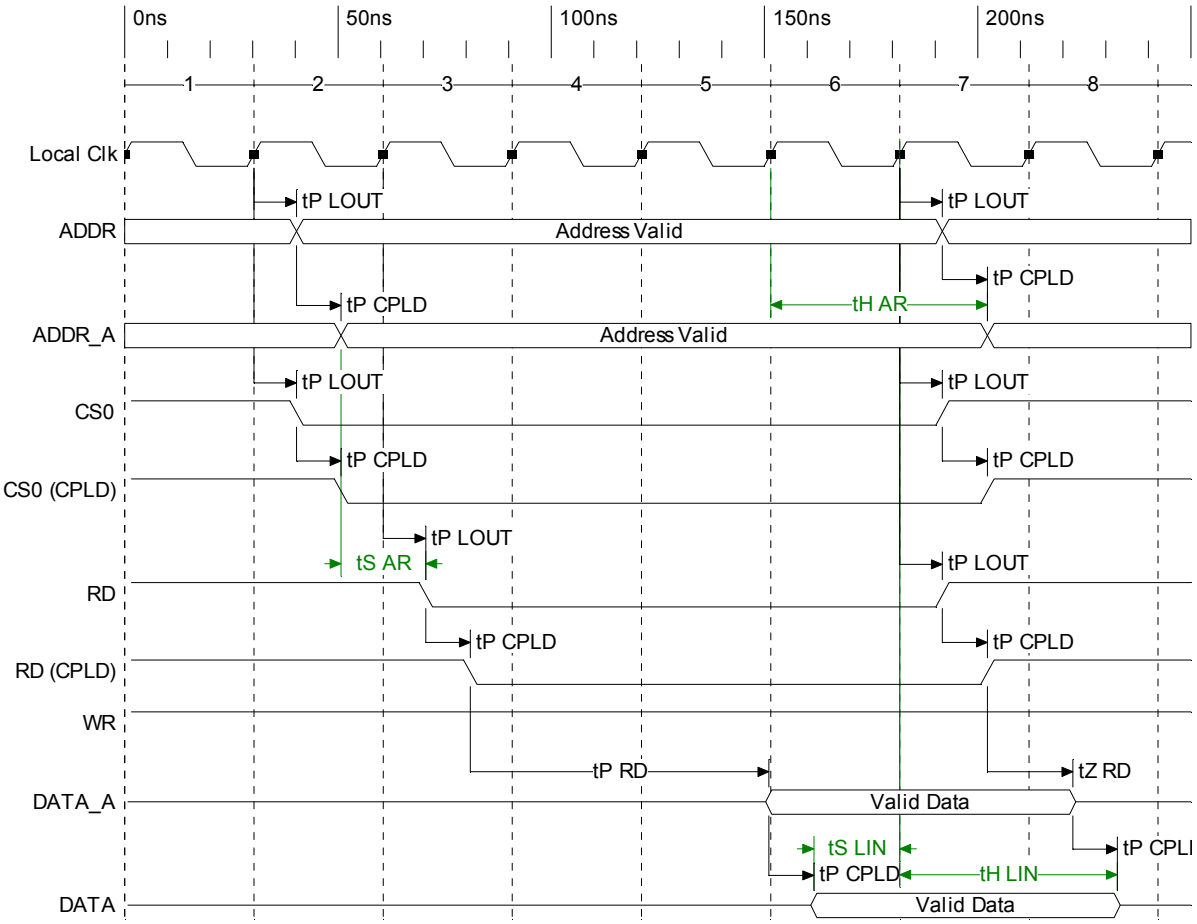
Table 10 SBI DROP Bus Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS SDC1FP	TEMUX-84	Input set-up time	3	7.86	4.86
tH SDC1FP	TEMUX-84	Input hold time	0	1	1
tS SBIDROP	SBS-Lite	Input set-up time	3	6.86	3.86
tH SBIDROP	SBS-Lite	Input hold time	0	1	1

6.1.3 SPECTRA-622 – PCI9030 Interface

The host processor can access the registers on the SPECTRA-622 via the PCI9030 Target Interface Device. The following diagrams show the timing that is required to read and write data between the SPECTRA-622 and PCI9030

Figure 16 – SPECTRA-622 to PCI9030 Read Access Timing Diagram



Address, Data, RD, WR and CS signals are further delayed by the CPLD (tP CPLD). In reference to Figure 16, the sequence of events for the PCI9030 to read data from the SPECTRA-622 is as follows.

1. On the rising edge of clock cycle 2, the PCI9030 outputs the required address and the appropriate chip select after a propagation delay of tP LOUT.

2. On the rising edge of clock cycle 3, the PCI9030 asserts the RD signal after a propagation delay of tP LOUT. The cycle in which the RD signal is asserted is set by the Read Strobe Delay bits in the LAS0BRD register of the PCI9030. For this interface, the value is 1.

3. After the propagation delay tP RD, the SPECTRA-622 puts valid data on the data bus. At the start of cycle 7, The PCI9030 reads the data from the data bus. The PCI 9030 inputs require a setup time of tS LIN and a hold time of tH

LIN. Note that the PCI 9030 waits 6 cycles for the data to be placed on the data bus, the NRAD bits in LAS0BRD set this delay.

4. At the start of cycle 7, the PCI9030 de-asserts the address lines, RD and CS after a propogation delay of tP LOUT. The de-assertion of the RD signal causes the SPECTRA-622 data bus to tristate after a propagation delay tZ RD.

The output propagation delays involved in Figure 16 are shown in the following table:

Table 11 PCI9030 to SPECTRA-622 Read Propagation Delays

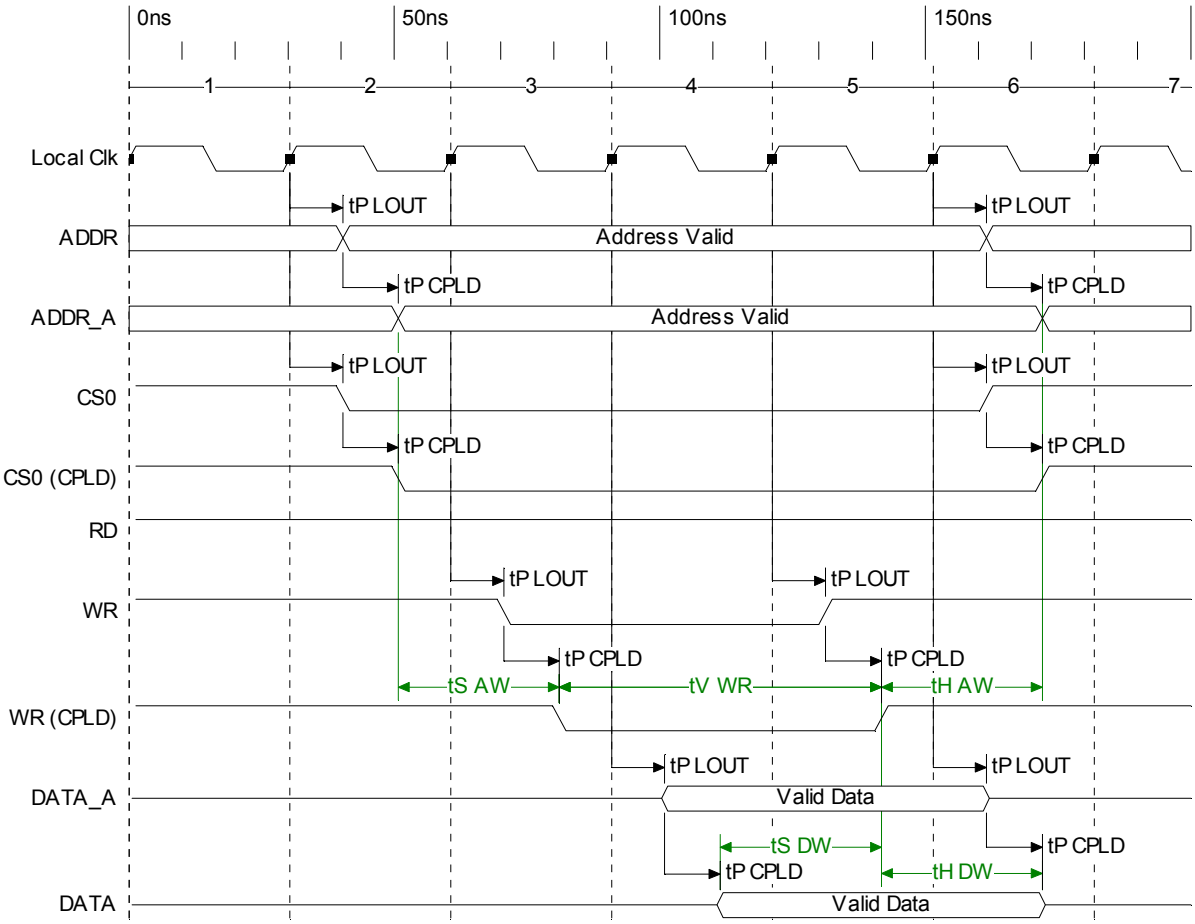
Name	Device	Description	Min	Max
tP LOUT	PCI9030	Local Clock edge to Local output delay	10	
tP RD	SPECTRA-622	RD to valid data delay	-	70
tZ RD	SPECTRA-622	RD negated to data tristate delay	-	20
tP CPLD	CPLD	Propogation delay through CPLD	10.5	

The input constraints involved in Figure 16 are shown in the following table:

Table 12 PCI9030 to SPECTRA-622 Read Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS AR	SPECTRA-622	Address to valid read setup	10	19.8	9.8
tH AR	SPECTRA-622	Address to valid read hold	5	50.8	45.8
tS LIN	PCI9030	Input setup time	5	20.21	15.21
tH LIN	PCI9030	Input hold time	1	51	50

Figure 17 – SPECTRA-622 to PCI9030 Write Access Timing



Address, Data, RD, WR and CS signals are further delayed by the CPLD (tP CPLD). In reference to Figure 17, the sequence of events for the PCI9030 to write data to the SPECTRA-622 is as follows:

1. On the rising edge of clock cycle 2, the PCI9030 outputs the required address and the appropriate chip select after a propagation delay of tP LOUT.

2. On the rising edge of clock cycle 3, the PCI9030 asserts the WR signal after a propagation delay of tP LOUT. The cycle in which the WR signal is asserted is set by the Write Strobe Delay bits in the LAS0BRD register of the PCI9030. For this interface, the value is 1. This delay is required to satisfy tS AW, the address to write setup time.

3. At the start of cycle 4, the PCI9030 puts valid data on the data bus after a propagation delay of tP LOUT.

4. The SPECTRA-622 inputs require the data to be present for a setup time of tS DW and a hold time of tH DW. To satisfy these requirements, the PCI 9030 waits 2 cycles with valid data on the data bus. The NWDD bits in LAS0BRD set the wait delay. This wait delay also satisfies tV WR, the Valid Write Pulse width.

5. On the rising edge of clock cycle 5, the PCI9030 deasserts the WR signal after a propagation delay of tP LOUT. This causes the SPECTRA-622 to latch the data from the bus. The data must remain present on the bus for an additional tH DW. This is accomplished by setting the Write Cycle Hold bits in LAS0BRD to 1. The write cycle hold causes LDATA, CS, and ADDR to stay active until the rising edge of cycle 6, when they deassert after tP LOUT.

The output propagation delays involved in Figure 17 are shown in the following table:

Table 13 PCI9030 to SPECTRA-622 Write Propagation Delays

Name	Device	Description	Min	Max
tP LOUT	PCI9030	Local Clock edge to Local output delay	10	
tP CPLD	CPLD	Delay through the CPLD	10.5	

The input constraints involved in Figure 17 are shown in the following table:

Table 14 PCI9030 to SPECTRA-622 Write Timing Constraints

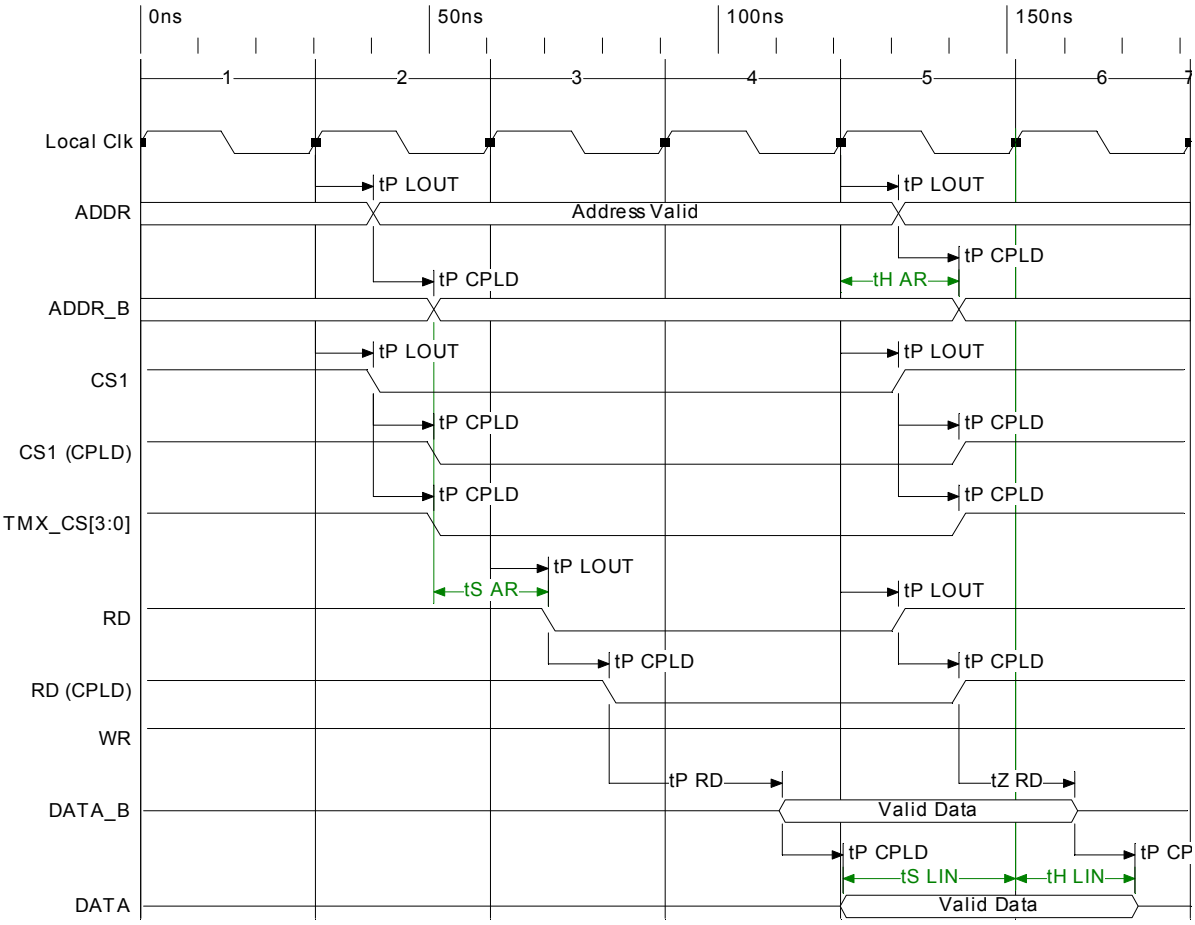
Name	Device	Description	Min	Actual	Margin
tS AW	SPECTRA-622	Address to valid write set-up	10	30.3	20.3
tV WR	SPECTRA-622	Valid write pulse width	40	60.61	20.61
tH AW	SPECTRA-622	Address to valid write hold	5	30.8	25.3
tS DW	SPECTRA-622	Data to valid write set-up	20	30.3	10.3
tH DW	SPECTRA-622	Data to valid write hold	5	30.3	25.3

6.1.4 TEMUX-84 – PCI9030 Interface

The host processor can access the registers on the each of the four TEMUX-84 devices via the PCI9030 Target Interface Device. There will be one chip select and address range in the PCI9030 allocated for all TEMUX-84 devices. The CPLD on the card will use this chip select signal plus the information on the address bus to allow individual access to each of the TEMUX-84 devices. See Section 8.1 below for a detailed description of the CPLD address decoding implementation. The read and write accesses of the TEMUX-84's are shown below in Figure 18 and Figure 19 - PCI9030 to TEMUX-84 Write Access Timing

Diagram respectively. Please refer to the respective device datasheets for the timing data.

Figure 18 – TEMUX-84 to PCI9030 Read Access Timing Diagram



Address, Data, RD, WR and CS signals are further delayed by the CPLD (tP CPLD). In reference to Figure 18, the sequence of events for the PCI9030 to read data from any TEMUX-84 is as follows:

1. On the rising edge of clock cycle 2, the PCI9030 outputs the required address after a propagation delay of tP LOUT. An appropriate chip select is outputted by the PCI9030 and then the individual TEMUX-84 chip select is decoded after a delay of tP LOUT.

2. On the rising edge of clock cycle 3, the PCI9030 asserts the RD signal after a propagation delay of tP LOUT. The cycle in which the RD signal is asserted is

set by the Read Strobe Delay bits in the LAS1BRD register of the PCI9030. For this interface, the value is 1.

3. After the propagation delay tP RD, the TEMUX-84 puts data on the data bus. At the start of cycle 5, The PCI9030 reads the data from the data bus. The PCI 9030 inputs require a setup time of tS LIN and a hold time of tH LIN. Note that the PCI 9030 waits 2 cycle for the data to be placed on the data bus, this delay is set by the NRAD bits in LAS1BRD.

4. Also at the start of cycle 5, the PCI9030 de-asserts the RD, CS, and address lines after the propagation delay, tP LOUT. The de-assertion of the RD signal causes the TEMUX-84 data bus to tristate after a propagation delay tZ RD.

The output propagation delays involved in Figure 18 are shown in the following table:

Table 15 PCI9030 to TEMUX-84 Read Propagation Delays

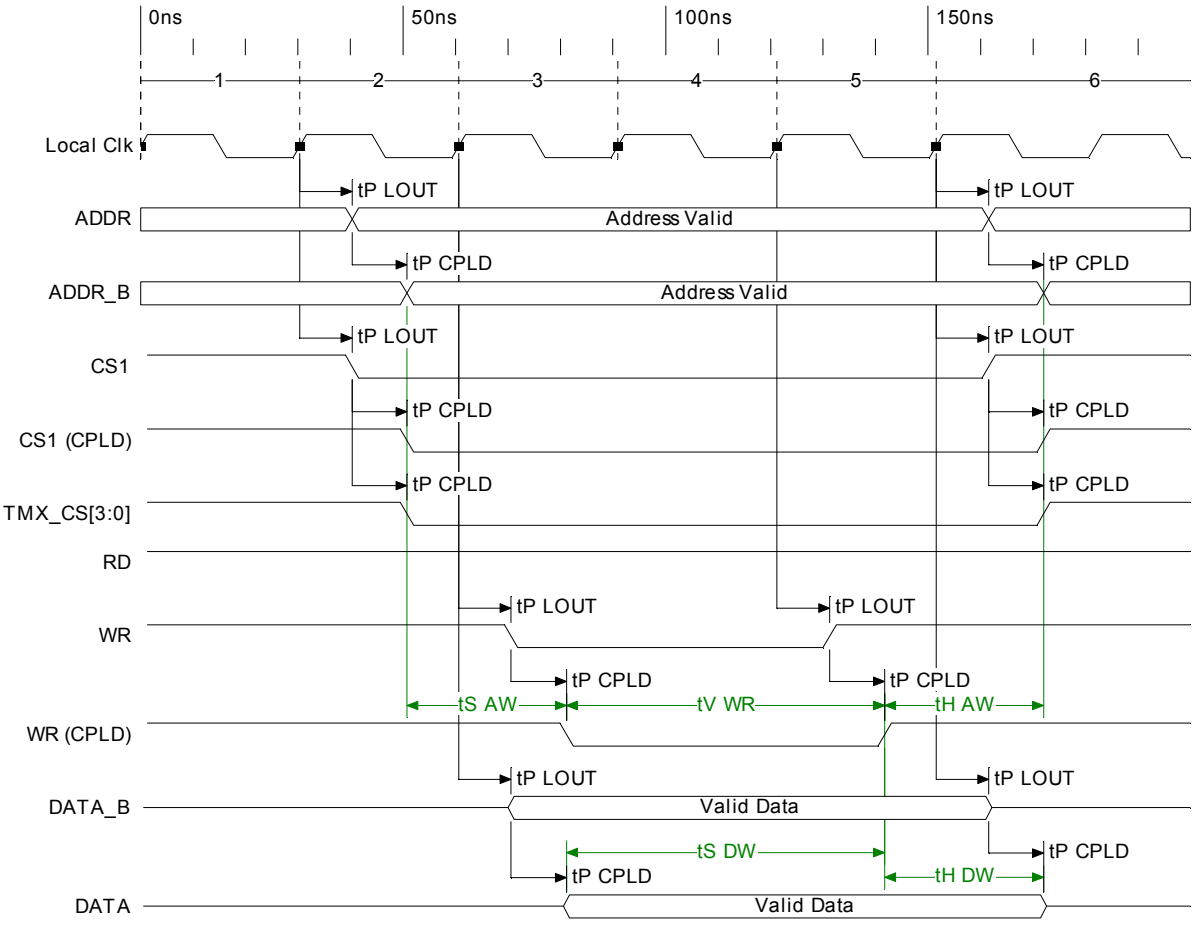
Name	Device	Description	Min	Max
tP LOUT	PCI9030	Local Clock edge to Local output delay	10	
tP RD	TEMUX-84	RD to valid data delay	-	30
tZ RD	TEMUX-84	RD negated to data tristate delay	-	20
tP CPLD	CPLD	CS Decode Input to Output Delay	10.5	-

The input constraints involved in Figure 18 are shown in the following table:

Table 16 PCI9030 to TEMUX-84 Read Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS AR	TEMUX-84	Address to valid read setup	10	19.8	9.8
tH AR	TEMUX-84	Address to valid read hold	5	20.5	15.5
tS LIN	PCI9030	Input setup time	5	29.91	24.91
tH LIN	PCI9030	Input hold time	1	20.7	19.7

Figure 19 - PCI9030 to TEMUX-84 Write Access Timing Diagram



Address, Data, RD, WR and CS signals are further delayed by the CPLD (tP CPLD). In reference to Figure 19, the sequence of events for the PCI9030 to write data to the TEMUX-84 is as follows:

1. On the rising edge of clock cycle 2, the PCI9030 outputs the required address and the appropriate chip select after a propagation delay of tP LOUT.

2. On the rising edge of clock cycle 3, the PCI9030 puts valid data on the data bus and asserts the WR signal after a propagation delay of tP LOUT. The cycle in which the WR signal is asserted is set by the Write Strobe Delay bits in the LAS1BRD register of the PCI9030. For this interface, the value is 1. This delay is required to satisfy tS AW, the address to write setup time.

3. The TEMUX-84 inputs require the data to be present for a setup time of tS DW. To satisfy these requirements, the PCI 9030 waits 1 cycles with valid

data on the data bus. The NWDD bits in LAS1BRD set the wait delay. This wait delay also satisfies tV WR, the Valid Write Pulse width.

4. On the rising edge of clock cycle 5, the PCI9030 deasserts the WR signal after a propagation delay of tP LOUT. This causes the TEMUX-84 to latch the data from the bus. The data must remain present on the bus for an additional tH DW. This is accomplished by setting the Write Cycle Hold bits in LAS1BRD to 1. The write cycle hold causes LDATA, CS, and ADDR to stay active until the rising edge of cycle 6, when they are de-asserted after tP LOUT.

The output propagation delays involved in Figure 19 are shown in the following table:

Table 17 PCI9030 to TEMUX-84 Write Propagation Delays

Name	Device	Description	Min	Max
tP LOUT	PCI9030	Local Clock edge to Local output delay	10	
tP CPLD	CPLD	CS Decode Input to Output Delay	10.5	-

The input constraints involved in Figure 19 are shown in the following table:

Table 18 PCI9030 to TEMUX-84 Write Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS AW	TEMUX-84	Address to valid write set-up	10	24.8	14.8
tV WR	TEMUX-84	Valid write pulse width	40	55.11	15.11
tH AW	TEMUX-84	Address to valid write hold	5	26.8	19.8
tS DW	TEMUX-84	Data to valid write set-up	20	55.11	35.11
tH DW	TEMUX-84	Data to valid write hold	5	26.8	19.8

6.1.5 SBS-Lite – PCI9030 Interface

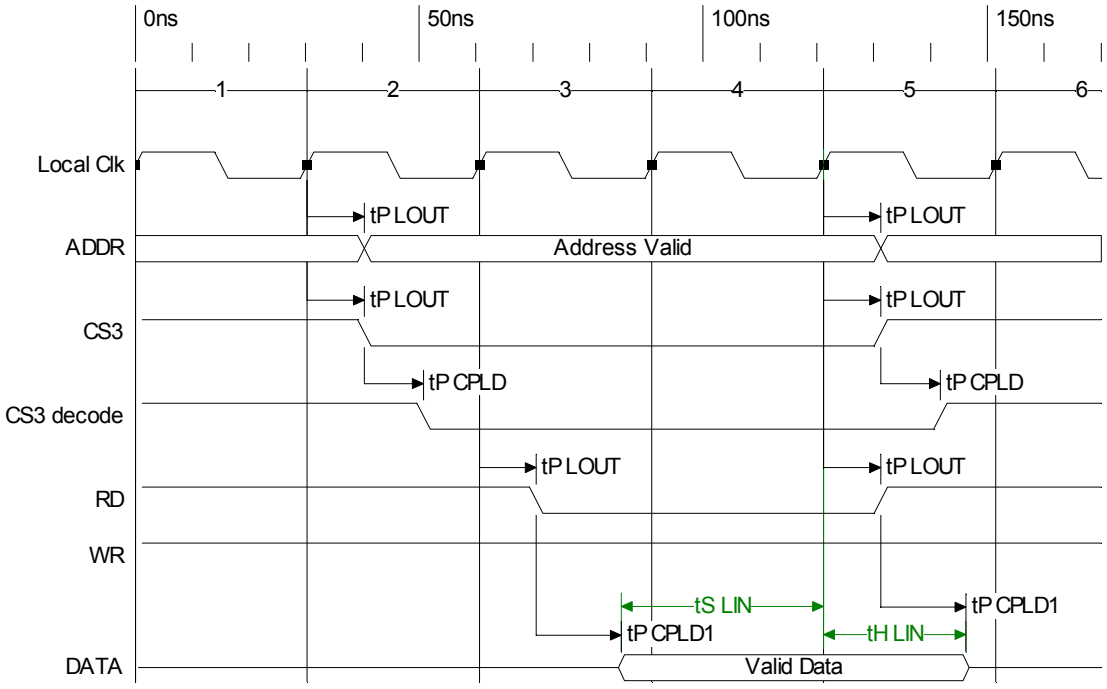
The host processor can access the registers on the SBS-Lite via the PCI9030 Target Interface Device. There will be one chip select and address range in the PCI9030 allocated for the SBS-lite.

An explanation of timing, delays, and constraints will not be shown in this section since all timing information is identical between the SBS-Lite and the TEMUX-84. Please refer to Section 6.1.4 for all of the necessary information.

6.1.6 XC95288XL CPLD – PCI9030 Interface

The host processor can access the internal registers of the XC95288XL CPLD via the PCI9030 Target Interface Device. There will be one chip select and address range in the PCI9030 allocated for the CPLD. See Section 8.1 belowbelow for a detailed description of the CPLD address decoding implementation. The read and write accesses to the CPLD are shown below in Figure 20 and Figure 21 - PCI9030 to CPLD Write Access Timing Diagram respectively. Please refer to the respective device datasheets for complete timing data.

Figure 20 – PCI9030 to CPLD Read Access Timing Diagram



Address, Data, RD, WR and CS signals are further delayed by the CPLD (tP CPLD). In reference to Figure 20, the sequence of events for the PCI9030 to read data from the CPLD is as follows:

1. On the rising edge of clock cycle 2, the PCI9030 outputs the required address and the appropriate chip select after a propagation delay of tP LOUT.

2. On the rising edge of clock cycle 3, the PCI9030 asserts the RD signal after a propagation delay of tP LOUT. The cycle in which the RD signal is asserted is

set by the Read Strobe Delay bits in the LAS3BRD register of the PCI9030. For this interface, the value is 1.

3. After the propagation delay tP CPLD1, the XC95288 puts valid data on the data bus. At the start of cycle 5, the PCI9030 reads the data from the data bus. The PCI 9030 inputs require a setup time of tS LIN and a hold time of tH LIN. Note the PCI 9030 waits 1 cycle for the data to be placed on the data bus, this delay is set by the NRAD bits in LAS1BRD

4. Also at the start of cycle 5, the PCI9030 de-asserts the RD, CS, and address lines after the propagation delay, tP LOUT. The de-assertion of the RD signal causes the CPLD data bus pins to tristate after a propagation delay tP CPLD1.

The output propagation delays involved in Figure 20 are shown in the following table:

Table 19 PCI9030 to XC95288 Read Propagation Delays

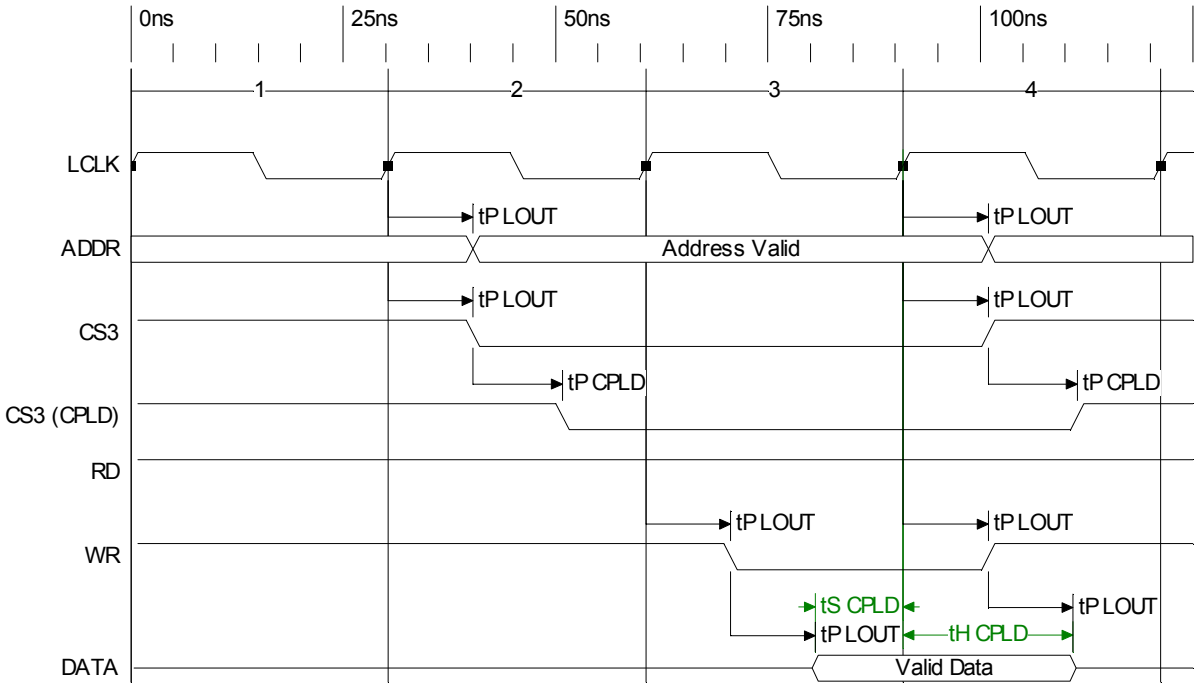
Name	Device	Description	Min	Max
TP LOUT	PCI9030	Local Clock edge to Local output delay	10	
TP CPLD	CPLD	Propogation delay	10.5	

The input constraints involved in Figure 20 are shown in the following table:

Table 20 PCI9030 to XC95288 Read Timing Constraints

Name	Device	Description	Min	Actual	Margin
TS LIN	PCI9030	Input setup time	5	35.61	30.61
TH LIN	PCI9030	Input hold time	1	25	24

Figure 21 - PCI9030 to CPLD Write Access Timing Diagram



Address, Data, RD, WR and CS signals are further delayed by the CPLD (tP CPLD). In reference to Figure 21, the sequence of events for the PCI9030 to write data to the XC95288 CPLD is as follows:

1. On the rising edge of clock cycle 2, the PCI9030 outputs the required address and the appropriate chip select after a propagation delay of tP LOUT.

2. On the rising edge of clock cycle 4, the PCI9030 puts valid data on the data bus and asserts the WR signal after a propagation delay of tP LOUT. The cycle in which the WR signal is asserted is set by the Write Strobe Delay bits in the LAS3BRD register of the PCI9030. For this interface, the value is 2.

3. The CPLD inputs require the data to be present for a setup time of tS CPLD. A wait cycle is required in order to meet the constraints. The NWDD bits in LAS3BRD set the wait delay, and its set to 1.

4. The CPLD latches the data on the rising edge of clock cycle 6 and then the PCI9030 deasserts the DATA, ADDR, CS3, and WR signals after a propagation delay of tP LOUT. The data must remain present on the bus for an additional tH CPLD. This requirement is satisfied since the hold time is

less than the propagation delay of the outputs. For longer hold times, the Write Cycle Hold bits in LAS3BRD could be used.

The output propagation delays involved in Figure 21 are shown in the following table:

Table 21 PCI9030 to XC95288 CPLD Write Propagation Delays

Name	Device	Description	Min	Max
tP LOUT	PCI9030	Local Clock edge to Local output delay	10	
tP CPLD	XC95288XL	CPLD propagation delay	10.5	

The input constraints involved in Figure 21 are shown in the following table:

Table 22 PCI9030 to XC95288 CPLD Write Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS CPLD	XC95288 CPLD	Input Setup time	3.7	10.3	6.6
tH CPLD	XC95288 CPLD	Input Hold time	0	20	20

6.2 Power Estimate and Thermal Analysis

Table 23 Power Consumption by Supply Rail for Each Device

1.8V	Quantity	Power (Watts) **	Current (mA)
SBS-Lite*	1	0.454	252
TEMUX-84*	4	3.88	2000
TOTAL		4.334	2252

3.3V	Quantity	Power (Watts) **	Current (mA)
SBS-Lite*	1	0.95	288
TEMUX-84*	4	0.898	272
SPECTRA-622	1	3.102	940
PCI 9030	1	0.495	150
PI49FCT3805	5	1.32	400
OSC EP26	5	0.924	280
XC95288XL	1	0.561	170
HP HFCT-5208	1	0.792	240
PECl OSC	1	0.198	60
TOTAL		9.979	3024

*Once accurate data for the TEMUX-84 and SBS-Lite is available, calculations should be done to show the total draw current draw through the 1.8V and 3.3V regulators, which will then reflect the total current drawn from the 5V and 3.3V cPCI power rails.

**The Power data calculated using

I = P / V
where I = current (A) IDDOP
P = power (Watt)
V = voltage (Volts) e.g. VDDQ

6.2.1 Titania™ Power Modules

The Austin Power Module Series delivers high quality, ultra compact, DC-DC conversion. The OC12 Line Card requires two power modules. The TPM_108612961 performs 5V to 3.3V conversion and the TPM_108612920 performs 3.3V to 1.8V conversion. Both modules are rated to operate in an ambient temperature range of 0°C to 80°C. The datasheets provide thermal derating curves, which provide max output current at specified temperatures.

The TPM_108612961 is supplying approximately 3024 mA to the board. In accordance with the derating curve for the case of zero air flow, the power module can provide the required current up to an ambient temperature of 47°C.

The TPM_108612920 is supplying approximately 2252 mA to the board In accordance with the derating curve for the case of zero air flow, the power module can provide the required current up to an ambient temperature of 70°C.

6.3 Signal Integrity Simulations

The following sections contain pre-layout simulations for the Telecom Bus, SBI336 Bus, and the PCI9030 Microprocessor Interface Bus. Since these simulations were performed before layout, certain trace lengths may change to accommodate physical restrictions. It is recommended that the approximate lengths, termination values, and bus topology not change without using a simulation program to verify that signal integrity is maintained. In each of the simulation layout diagrams, each driver and receiver represents the internal logic of each device pin. Microstrip represents the trace length from the device pin to via. Stripline is representative of the internal layer trace from one pin via to another. The stripline length and connection topology is very important to the success of these simulations. Other topologies should be simulated before being considered for routing.

6.3.1 Telecom Bus

The layout for the Telecom bus is shown below in Figure 22.

Figure 22 – Telecom ADD Bus Simulation

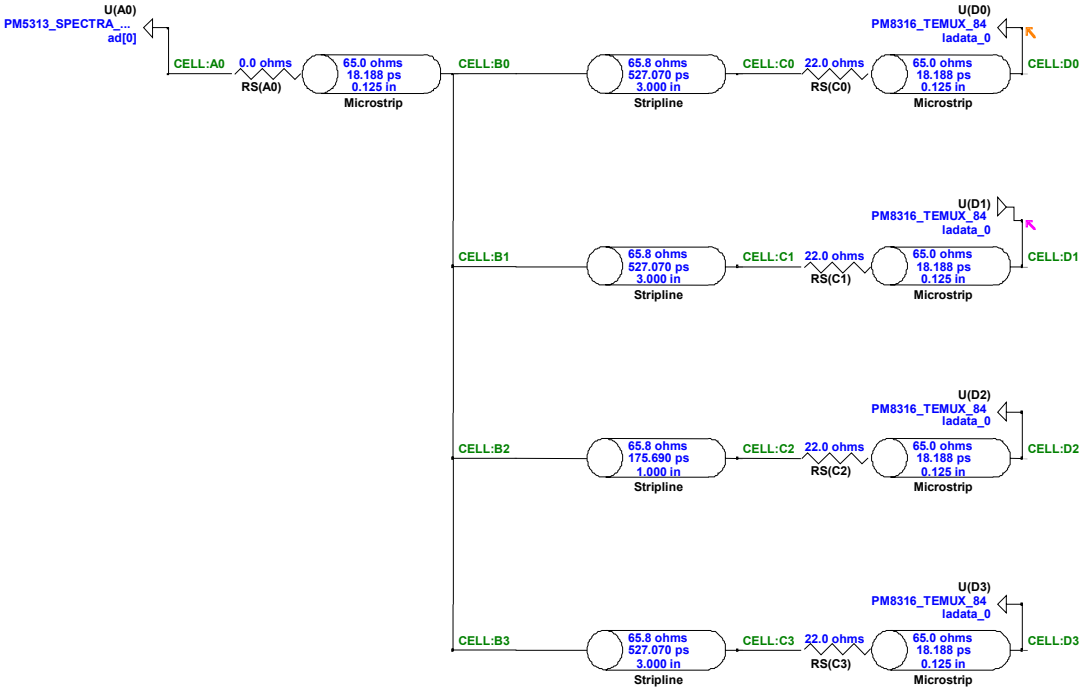
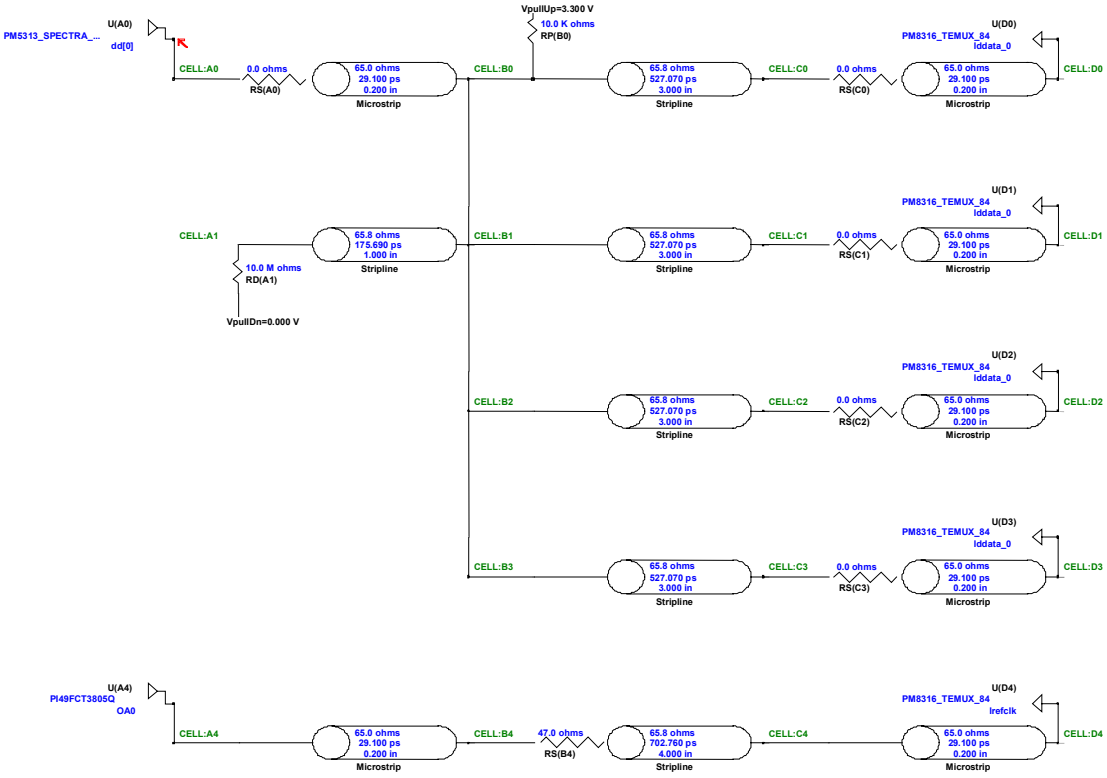
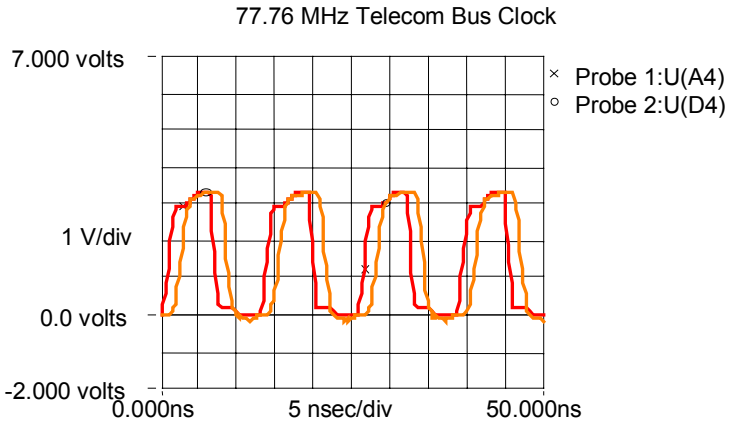


Figure 23 – Telecom DROP Bus Simulation



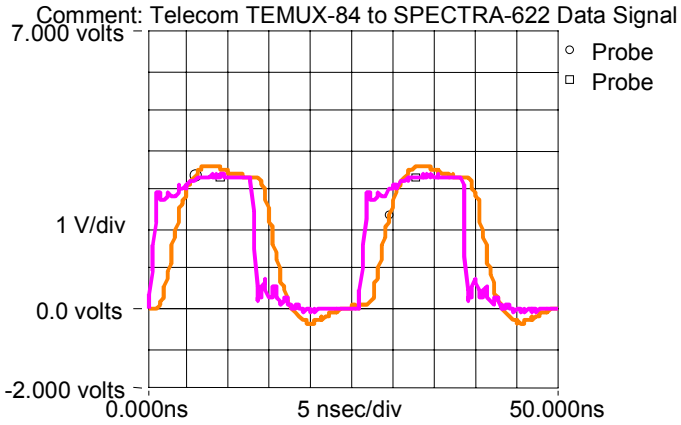
The pull down on the drop bus is added in order to simulate effects of the mictor connector. The 77.76 MHz clock drives the telecom bus. The simulated waveform is shown below in Figure 24.

Figure 24 – Telecom Bus Clock Signal



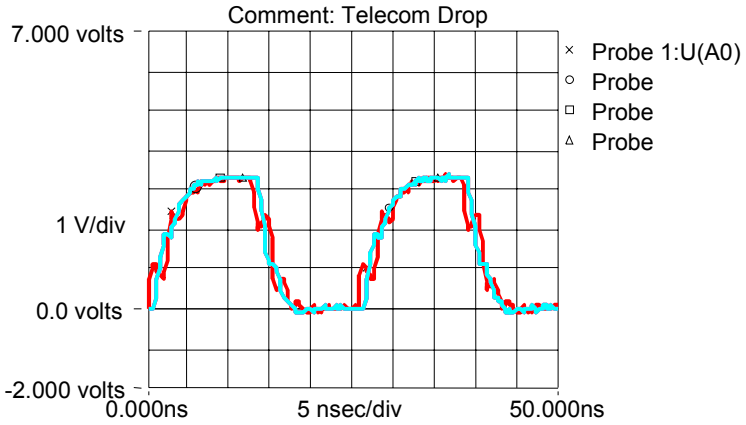
The data on the Telecom Bus is sampled on every rising clock edge. Since the clock frequency is 77.76 MHz, the data rate is half the clock frequency, 38.89 MHz. A simulation of a TEMUX-84 writing data to the SPECTRA-622 is shown in Figure 25 below.

Figure 25 – Telecom ADD Bus Data Signals



The data transmission on the bus is simulated in both the ADD and DROP directions, since the drivers and receivers of each device have slightly different characteristics. Figure 26 shows the SPECTRA-622 driving the Telecom bus.

Figure 26 – Telecom DROP Bus Data Signals



For some sections of the Telecom bus, a termination resistor is placed near the signal driver. Values of the resistors are chosen to lower excessive overshoot/undershoot.

6.3.2 SBI336 Bus

The layout for the SBI336 bus is shown in Figure 27. It is important to include the entire bus in this simulation, since each tri-stated output on the bus affects the signal integrity.

Figure 27 – SBI336 DROP Bus Simulation

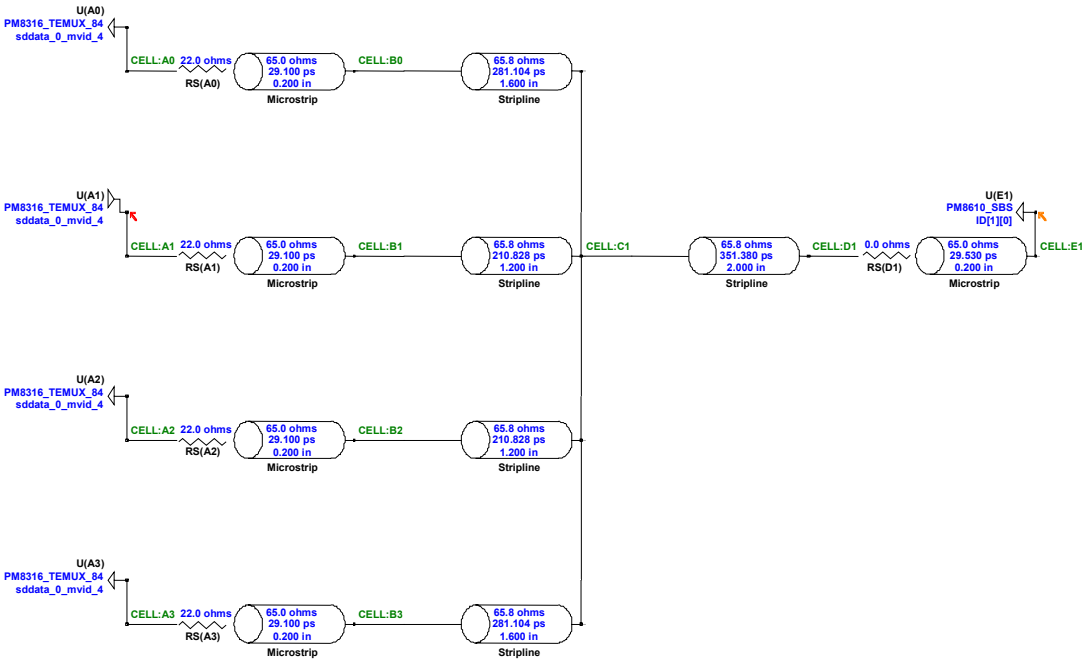
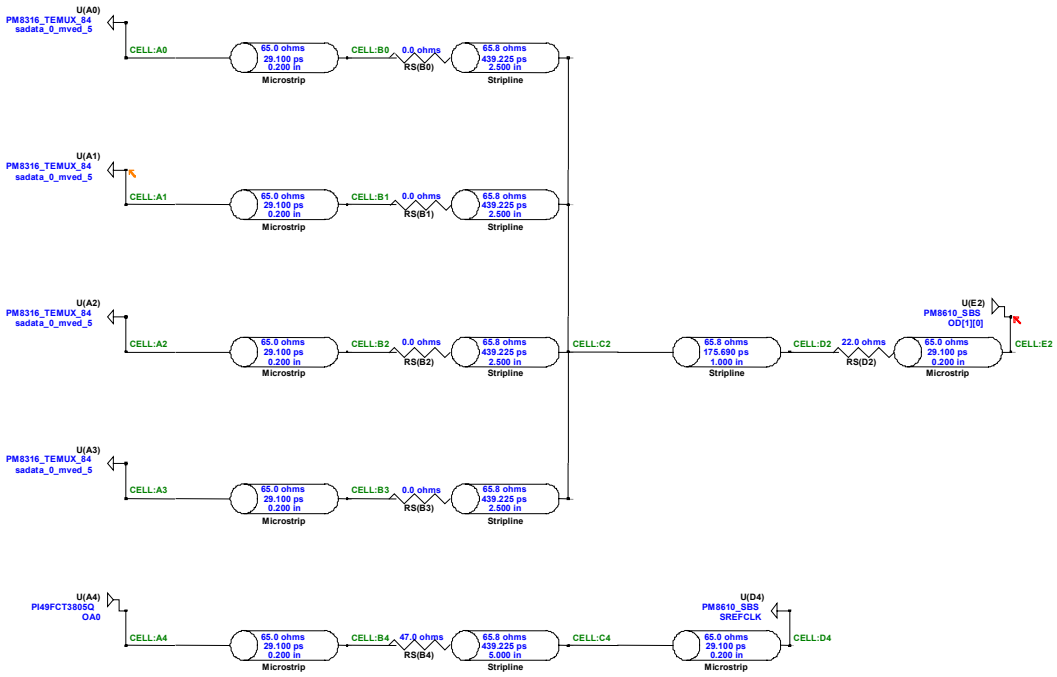
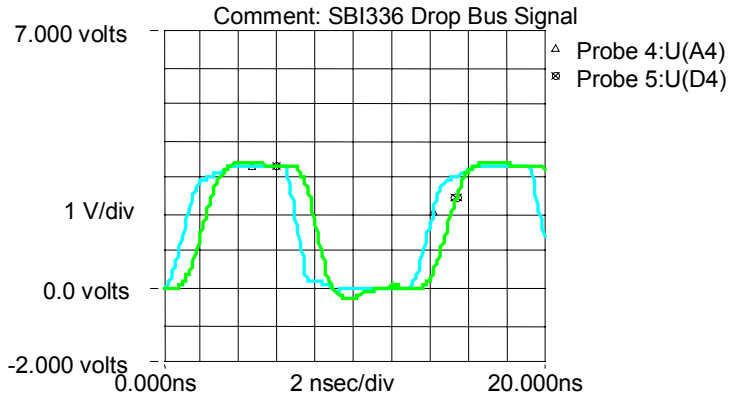


Figure 28 – SBI336 ADD Bus Simulation



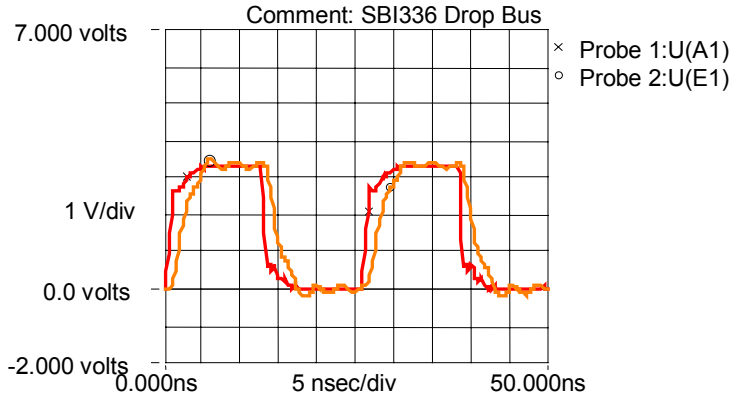
The 77.76 MHz clock drives the SBI bus. The simulated waveform is shown below in Figure 29.

Figure 29 – SBI336 Clock Signal



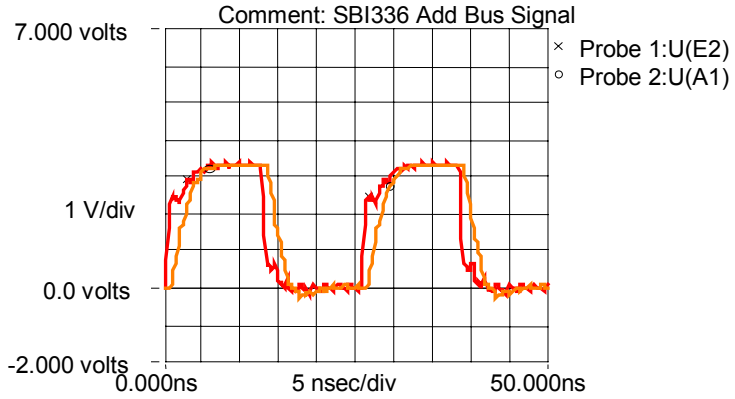
The data on the SBI336 Bus is sampled on every rising clock edge. Since the clock frequency is 77.76 MHz, the data rate is half the clock frequency, 38.89 MHz. A simulation of a TEMUX-84 writing data to the SBS-Lite is shown in Figure 30 below.

Figure 30 – SBI336 DROP Bus Waveform



The data transmission on the bus is simulated in both the ADD and DROP directions, since the drivers and receivers of each device have slightly different characteristics. Figure 31 shows the SBI336 ADD bus.

Figure 31 – SBI336 ADD Bus Waveform



For the clock lines of the SBI336 bus, the desired series termination value will be 47Ω, to be placed near the signal driver.

For the data lines that are shared between all bus devices, the simulations have shown that using a series termination resistor near each device on a multi-driver bus reduces the reflections from the driving device. Therefore, each device will have a series termination located near the pin. The optimum value has been found to be 22Ω.

Values lower than those tend to cause excessive overshoot/undershoot, while larger values will eventually reduce the current that the driver can supply.

6.3.3 Microprocessor Interface

6.3.3.1 Data Bus

The OC12 Line card has the option of choosing from two possible microprocessors. Using a specified jumper, one can choose either of the two microprocessors. For the following simulation, the PCI9030 controller is used. The address and data signals are routed via the CPLD. The microprocessor interface connects between 8 different devices, with the PCI9030 performing read and write operations on the other 7 devices, the initial simulations indicated that the PCI9030 cannot drive that many devices at the required bus speed. See Section 4.7.1 for a diagram of the microprocessor interface topology.

The data lines between the XC95288XL and devices require series termination since both are strong drivers and cause excessive overshoot/undershoot when not terminated. Refer to Figure 32 for the PCI9030 to CPLD simulation layout.

Figure 32 – PCI9030 / XC95288XL Simulation Layout

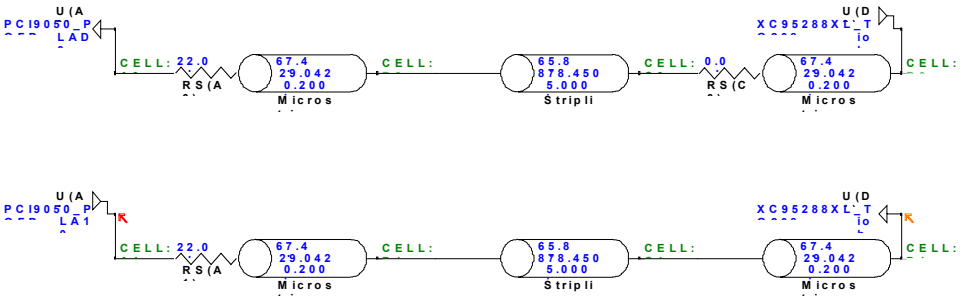
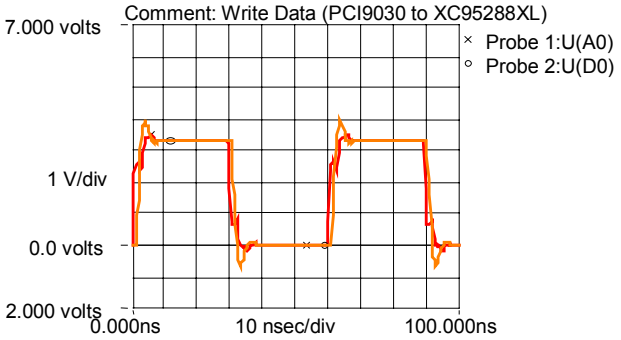


Figure 33 – PCI9030 / XC95288XL Data Waveforms



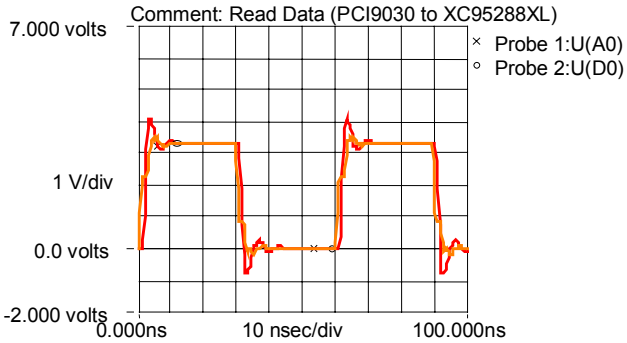
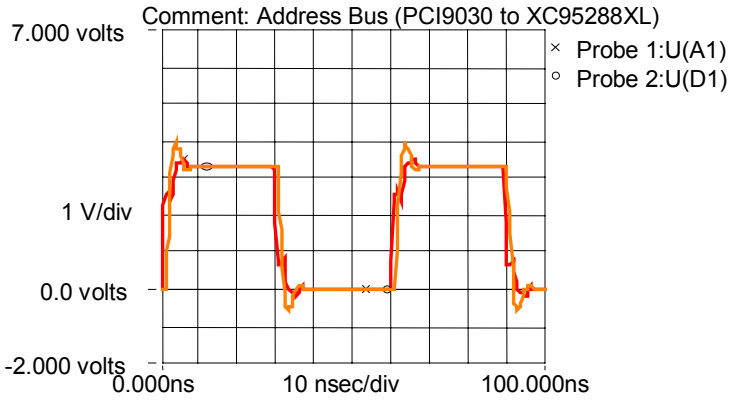


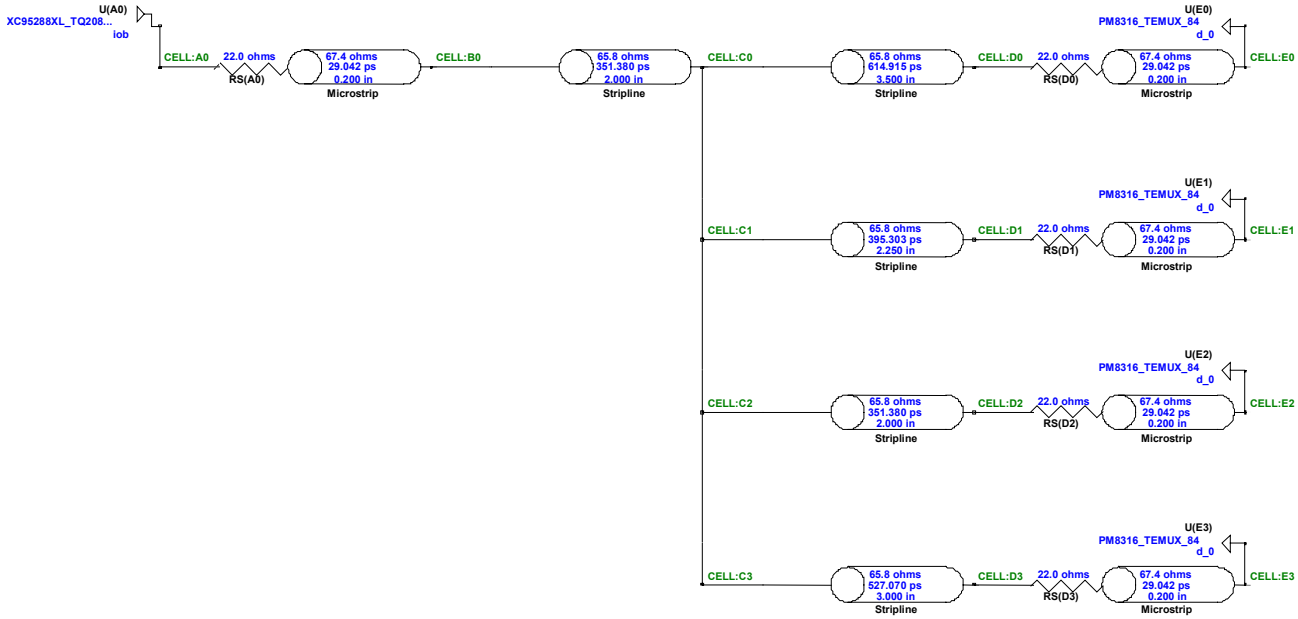
Figure 34 – PCI9030 / XC95288XL Address Waveforms



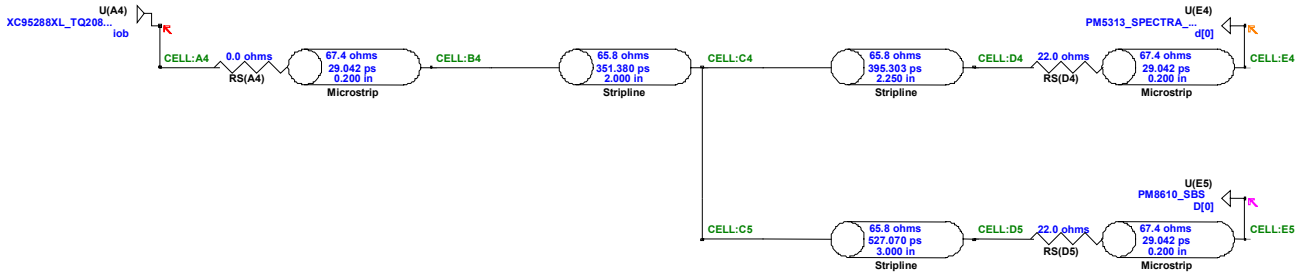
The microprocessor bus consists of two separate sections. Section 1 refers to the four TEMUX-84s device group and the other two devices group is labelled section 2. (The TEMUX-84 devices are all grouped on the same bus to simplify the bus design.) Since only one transceiver can be active during a read operation, the TEMUX-84 chip select pin is used to select which transceiver is currently active.

Figure 35 - Microprocessor Interface Data Bus Simulation Layout

Section 1



Section 2



There is no clock simulation required for the microprocessor interface, since the clock is only used by the PCI9030 to synchronously read in data. All writes to the other devices are asynchronously controlled by the PCI9030.

Since the clock frequency of the local bus is 33.33 MHz, the data rate is half the clock frequency, 16.67 MHz.

Please refer to Figure 36 and Figure 37 below, which show the waveforms for read and write operations on both sections of the microprocessor data bus interface.

Figure 36 - Microprocessor Data Bus, Section 1 Waveforms

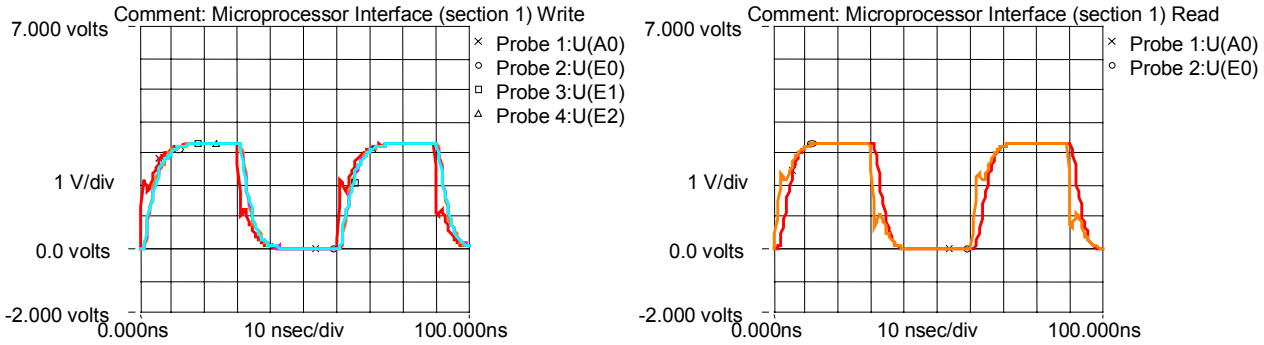
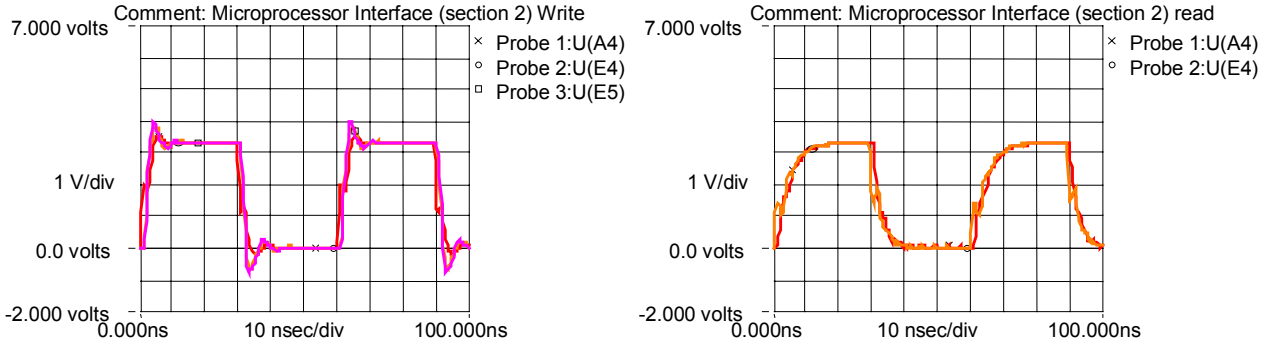


Figure 37 - Microprocessor Data Bus, Section 2 Waveforms



For some of the multi-point, bi-directional data lines, the simulations have shown that a series termination resistor is required near each device to reduces the reflections from the driving device. Therefore, those devices will have a series termination. The optimum value has been found to be 22Ω.

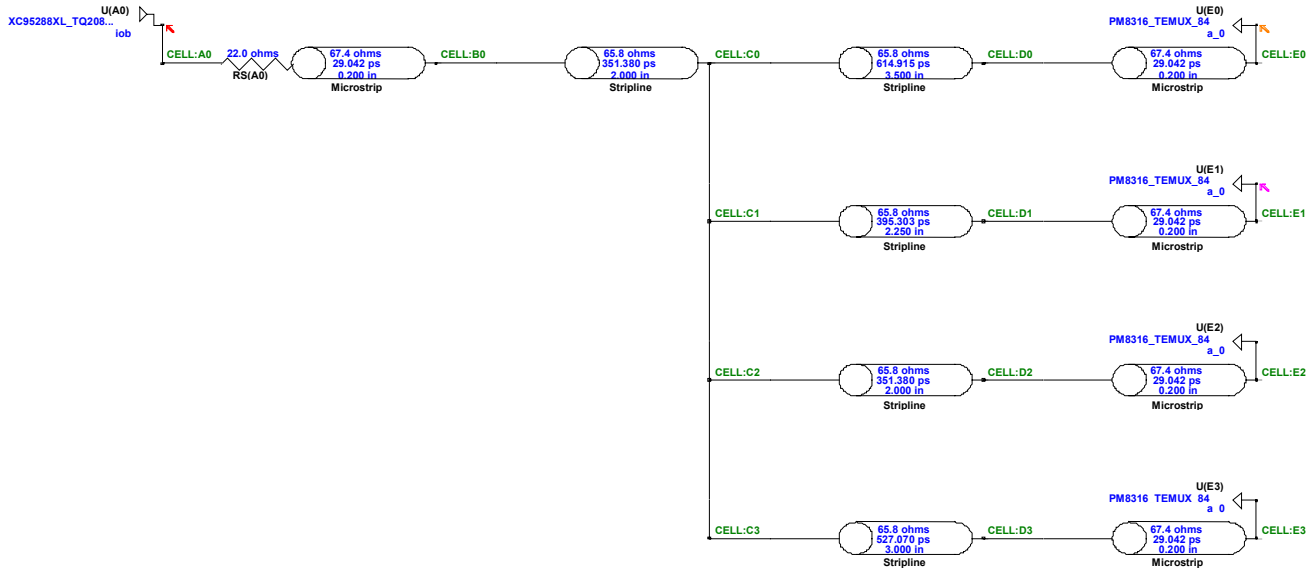
Values lower than those tend to cause excessive overshoot/undershoot, while larger values will eventually reduce the current that the driver can supply.

6.3.3.2 Address Bus

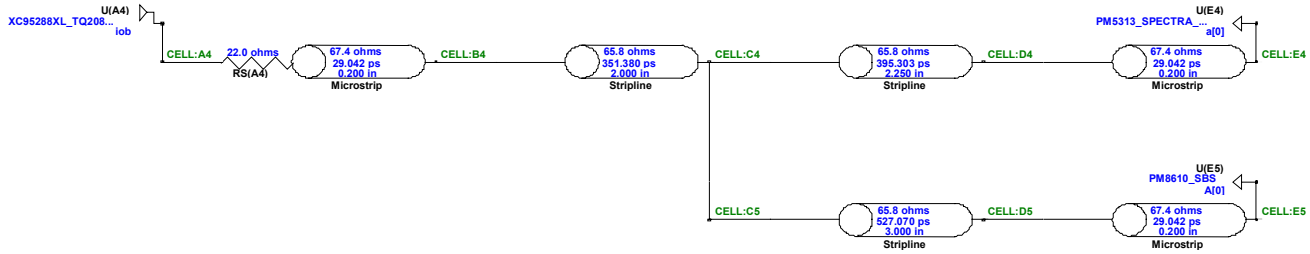
The address bus is designed using a similar methodology to the data bus, with the exception being that the bus is uni-directional. The address bus is still divided into two sections generated by the CPLD, then connected as shown below in Figure 38. Section 1 as before controls the four TEMUX-84s and section 2 controls the other three devices.

Figure 38 - Microprocessor Interface Address Bus Simulation Layout

Section 1

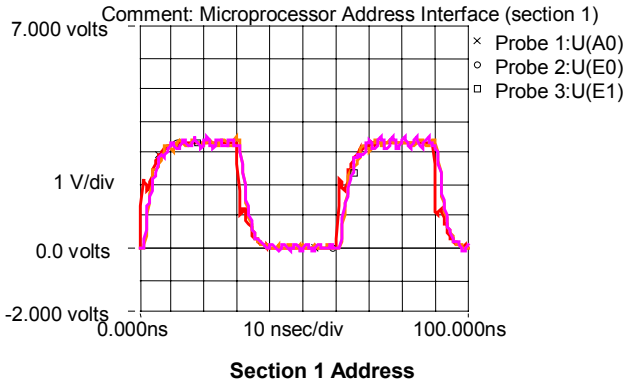


Section 2

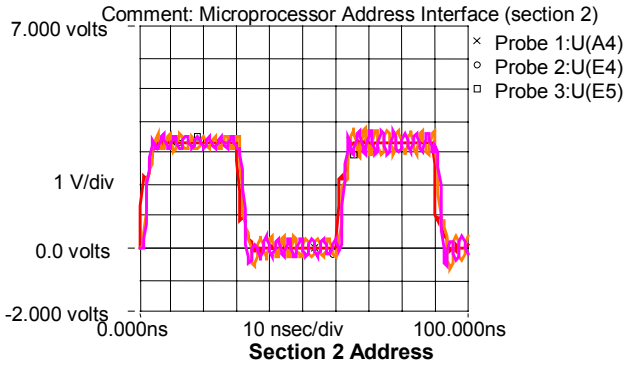


The address lines change at the same frequency as the data lines, 16.67 MHz. Please refer to Figure 39 below, which show the waveforms for both sections of the microprocessor address bus interface.

Figure 39 - Microprocessor Address Bus Waveforms



Section 1 Address



Section 2 Address

For the multi-point, uni-directional address lines, the simulations have shown that using a series termination resistor near the driver reduces the overshoot and undershoot of the signal. Therefore, only the driving device will have a series termination that should be physically located near the output. The optimum value has been found to be 22Ω.

7 DESIGN DETAILS

7.1 Component Placement

The overall placement strategies of the components are:

Place the analog circuitry away from the digital circuitry.

Keep the analog transmit side components separate from the analog receive side components.

For high-speed data lines on bi-directional busses, series termination resistors are placed near each pin on the bus to reduce reflections.

For high-speed data lines on uni-directional busses, source termination resistors are placed near the driver outputs to reduce ringing. Ringing usually occurs when the driver is driving a smaller number of gates.

The Telecom bus and the SBI bus should be routed so that the bus length is approximately the same to each TEMUX-84 from the SPECTRA-622 or the SBS-Lite.

The PCI Bridge and the CPLD should be placed so that the I/O interface bus can be routed perpendicular to the telecom/SBI buses. This is not a critical requirement, but it helps make routing more efficient and reduces crosstalk.

All pull up/down resistors are placed near the output pins.

The oscillator is placed in a quiet digital section as noise on its power supply will cause jitter on the output, and the oscillator itself generates noise that may affect sensitive analog circuits.

The PCI Bridge device is placed such that all the PCI interface traces are within the specified length limits of the PCI Rev. 2.1 Specification.

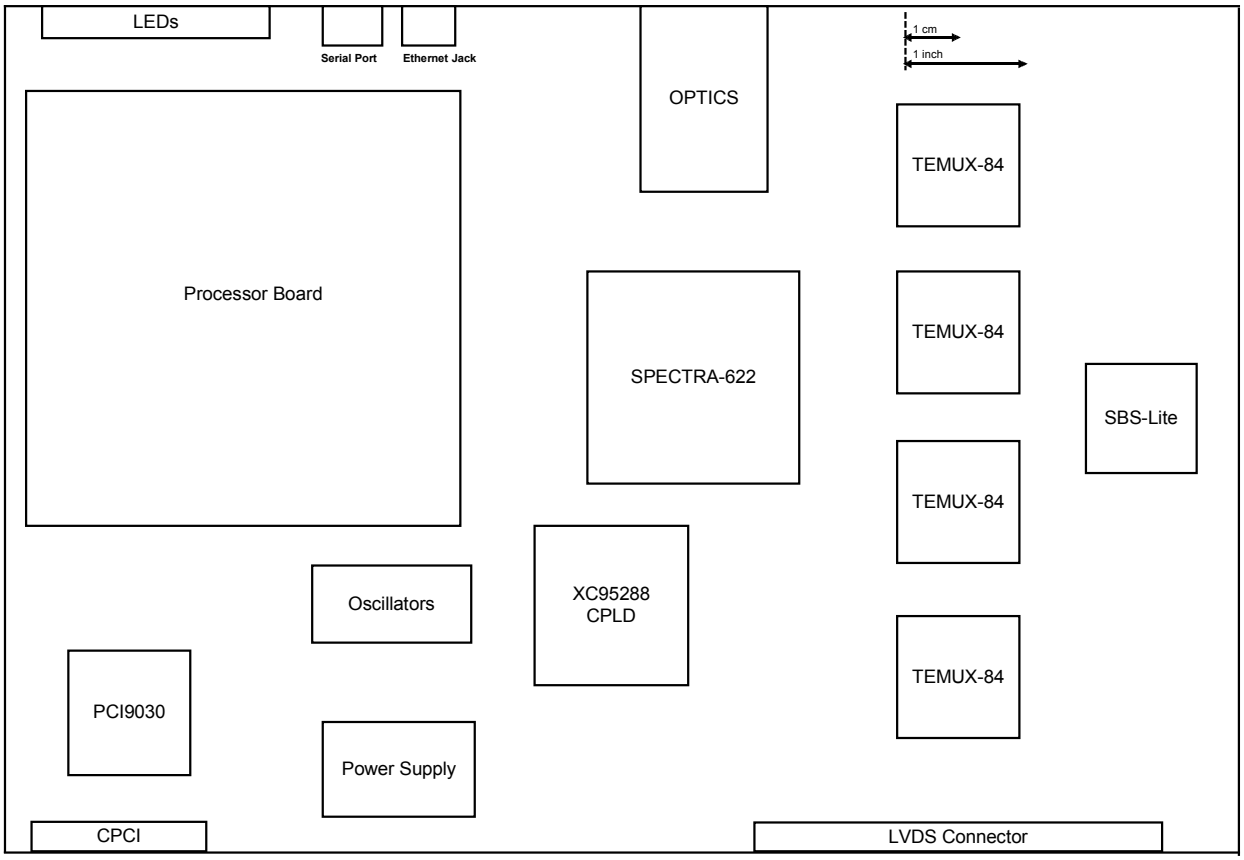
All decoupling capacitors are placed near the power supply pins.

The power supply should be placed in a low-component density area of the board so that sufficient copper on the component layer can be used for heatsinking of the supply regulators. (See Section 6.2 for the calculations of required copper surface area)

Use a single plane for both analog and digital grounds.

The approximate placement of major components is shown in Figure 40 below. (The diagram is drawn to scale.)

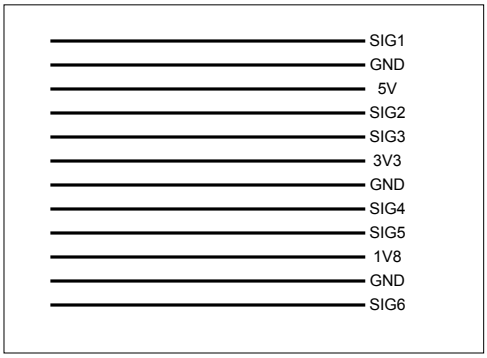
Figure 40 – Card Floorplan



7.2 Layer Stacking and Impedance Control

The OC-12 Line Card has 12 layers. Six layers are signal layers and six layers are power/ground layers. It important to orient the layers in the stacking arrangement shown in Figure 41 in order to minimize EMI and crosstalk from the signal layers.

Figure 41 – Layer Stack



To reduce signal degradation due to reflection and radiation, the traces that carry high speed signals should be treated as micro strip transmission lines with controlled impedance and matched resistive termination.

Given characteristic impedance Zo, the dielectric thickness is proportional to trace width. A small dielectric thickness will result in the traces being too thin to be accurately fabricated. Wider traces can be more precisely manufactured, but they take up too much board space. Therefore, the thickness of the board for a given trace impedance and adequate trace width should be chosen so that the traces take up as little board space as possible yet still leaving enough margin to allow accurate fabrication.

The dielectric material and thickness of the board is chosen such that when using a 6-mil trace, the characteristic impedance is 65Ω.

7.3 PCI Bus Signal Specification

This layout follows the PCI Rev. 2.1 Specification layout restrictions. The PCI SIG specification has stringent and detailed rules on decoupling, power consumption, trace length limits, routing, trace impedance, as well as signal loading. Therefore, it is essential to check the latest PCI specification before proceeding with new designs and layouts.

The OC-12 Line Card conforms to the following PCI Specification/Recommendations:

Component height on the component side does not exceed 0.570 inches, and on the solder side does not exceed 0.105 inches.

PCI CLK signal trace is 2.5 inches +/- 0.1 inches and is connected to only one load.

All 32-bit interface signals have the maximum trace length of 1.5 inches.

Trace impedance for shared PCI signals are within 60 - 100 Ohm range, and trace velocity is between 150 and 190 ps/inch.

15 mil wide traces are used to connect the power and ground pins on PCI connector to their respective planes and the trace lengths are limited to 250 mil.

7.4 Routing

All power and ground traces are as wide and as short as possible to minimize trace inductance.

All high speed traces are routed over continuous image planes (power or ground planes).

All traces carrying transmit and receive line rate data should be routed on the same side and kept as short as possible.

Both signals of a differential pair should be of equal length and routed close to each other.

7.5 Emission

Effective ways of reducing EMI include proper routing, de-coupling, power and ground distribution, shielding, and filtering. Most of the additional measurements listed below for EMI improvements also lend themselves towards improving system level performance.

Data lines should be kept away from the clock signals to avoid noise coupling.

Capacitor footprints can be placed along signals with fast rise and fall times. In the event that fast edges cause excessive EMI, installing these capacitors can slow them down.

7.6 Connectors

7.6.1 CompactPCI Connector

The CompactPCI connector is defined as a 5 row by 47 position array of pins divided logically into two groups corresponding to the physical connector implementation. 32-bit PCI and connector keying is implemented on one connector (J1). An additional connector (J2) is defined for 64-bit transfers. In this design only 32-bit transfers are supported.

The pinout of the CompactPCI connector is detailed in the CompactPCI specification [3].

J1 is used to supply power and ground to the board, as well as a 32-bit interface to the CPCI motherboard. LVDS data from the OC-12 Line Card is sent to the NSE over a custom section of the backplane.

7.6.2 OC-12 Optical Connector

The Optical Transceiver converts incoming SONET OC-12 signals (622 Mb/s) to PECL levels for interfacing to the SPECTRA-622 (and vice versa in the transmit direction). The optical transceiver is mounted against the front panel allowing fiberoptic connectors on the cable to be plugged directly into the transceiver.

7.6.3 HS3 Connector

AMP's Z-PACK HS3 connector is a two-piece board-to-board backplane connector. This high-density, high-speed connectors are modular devices with 25mm signal modules and half-size end modules with guide pins of six rows with 60 high-speed lines per 25mm, respectively. The Z-PACK HS3 connector has a controlled impedance of 50 and comes in dual microstrip configuration

7.6.4 RJ-45 Shielded Ethernet Connector

AMP’s (or Stewart’s) RJ-45 shielded 8-pin female connector allows access to an onboard generic processor from a workstation via an ethernet connection. The pins are connected as follows

Table 24 RJ-45 Shielded Ethernet Connector Pin Assignment

Pin	**SIGNAL**
1	TX+
2	TX-
3	RX+
4	N/C
5	N/C
6	RX-
7	N/C
8	N/C
9	GND
10	GND
11	GND
12	GND

7.6.5 JTAG Debug Port

The board supports in-system boundary scan testability through the use of the IEEE 1149.1 JTAG Debug Port. The devices are connected in the following order:

- SPECTRA-622
- TEMUX-84 #1
- TEMUX-84 #2
- TEMUX-84 #3
- TEMUX-84 #4
- SBS-Lite
- PCI9030 or generic onboard processor

The pin assignment for the JTAG Debug Port is listed in Table 25.

Table 25 JTAG Debug Port Pin Assignment

Pin	**SIGNAL**
1	+3.3V
2	TRST
3	TMS
4	TDO
5	TDI
6	TCK
7	GND
8	GND

7.6.6 CPLD ISP Port

The CPLD can be reprogrammed in-circuit through the use of the IEEE 1149.1 JTAG interface. The CPLD is the only device attached to this port.

The pin assignment for the CPLD ISP Port is listed in Table 26.

Table 26 CPLD ISP Port Pin Assignment

Pin	SIGNAL
1	+3.3V
2	TRST
3	TMS
4	TDO
5	TDI
6	TCK
7	GND
8	GND

7.6.7 CPLD Clock SMB Connector

The Clock SMB Connector is provided to allow the use of an external clock source to be distributed via the CPLD. The CPLD has access an external 77.76 MHz clock and 2 KHz framing pulse from an external source via SMB connectors. Jumpers have to be set in order to take advantage of the external signals.

7.6.8 MICTOR Connectors

There are two high-density MICTOR 38-pin connectors used on the board. These connectors allow test equipment to connect directly into various busses so that signal activity can be easily monitored.

The MICTOR connectors attached to the 77.76 MHz SBI336 Bus and the 77.76 MHz Telecom Bus.

Please refer to the attached schematic in APPENDIX B: SCHEMATICS, for more details regarding which signals are available on each connector.

7.7 Jumper Configuration

Jumpers are used on the Line Card to select certain software and hardware configuration options that require user selection. Jumpers are used when a feature only needs to be configured once at start-up to select a feature. Any feature that could require configuration changes more than once during card operation are mapped to a configuration register in the CPLD or on another device. On the line card a 8x2 header is used to act as jumper. When specified pins are connected and disconnected, as seen in the table below, features of the card can be altered. Table 27 show which features the jumpers on the OC-12 Line Card control and which pins on the header control these features.

Table 27 OC-12 Line Card Jumper Configuration

Reference Designator	Name	Operation
J12 / J13	JTAG Enable	To use the JTAG Debug Port, J14, to access the JTAG interface, there should be no jumpers on J14 and there must be a jumper on J9. To use the JTAG interface over the cPCI bus, J9 must be left unconnected, and a jumper must connect pins 4 and 5 of J14.
J10 (Header)		
Pin 1 & 2	Outgoing Frame Pulse Source	The default setting for the outgoing frame pulse is using the incoming backplane frame pulse as the signal's source. When a jumper connects pins 1 and 2, the source of the frame pulse is the CPLD generated 2 kHz pulse.
Pin 3 & 4	PCI9030 or Generic Processor Configuration	The default setting is use of the external host processor via the PCI9030 as the board's microprocessor. When a jumper connects pins 3 and 4, the onboard processor is used as the board's microprocessor.
Pin 5 & 6	77MHz Clock Source 1	The backplane 77.76 MHz Clock source will be the default clock source. When a jumper connects pins 5 and 6, this indicates that the Local onboard 77.76 MHz oscillator will be the clock source.
Pin 7 & 8	77MHZ Clock Source 2	The backplane 77.76 MHz Clock source will be the default clock source. If a jumper connects pins 7 and 8, this indicates that the external 77.76 MHz clock source will be used. (the onboard oscillators overrides the external clock if both are activated)
Pin 9 & 10	Frame Pulse Source 1	The incoming backplane frame pulse will be the default frame pulse source. When the jumper connects pins 9 and 10, this indicates that the locally generated frame pulse will be the frame pulse source.
Pin 11 & 12	Frame Pulse Source 2	The incoming backplane frame pulse will be the default frame pulse source. When the jumper connects pins 11 and 12, this indicates that the external frame pulse source will be used.

Reference Designator	Name	Operation
		(the locally generated frame pulse overrides the external frame pulse if both are activated)
Pin 13 & 14	CMP Signal Source	The backplane CMP signal is the default source that controls the connection memory of the SBS-Lite. When the jumper connects pins 13 and 14, this indicates that the SBS-Lite xCMP registers inside the CPLD generate the xCMP signals.

When the jumpers on the header pins are unconnected the pin is set to a logic high (3.3V source). With a jumpers connected the CPLD pin is set to a logic low (GND).

7.8 LEDs

Several LEDs will be used on the front panel to indicate the status of the SONET/SDH links and the status of the card power supply. See Table 28 below for a description of all status LEDs.

Table 28 LED Description

Function	Color	Description
+5V Status (Vcc)	Green	Indicates when +5V supply is on.
+3.3V Status	Green	Indicates when +3.3V supply is on.
+1.8V Status	Green	Indicates when +1.8V supply is on.
Reset	Green	Indicates when RESET is asserted.
LOF (Loss of frame)	Red	Active when out of frame state persists for more than 3 ms.
LOS (Loss of signal)	Red	Active when a violating period (20±2.5us) of consecutive all zeroes is detected in the incoming stream.
LRDI (Line remote defect indication)	Red	Active when line RDI is detected in the incoming stream.
LAIS (Line alarm indication signal)	Red	Active when line AIS is detected in the incoming stream.
SALM (Section alarm)	Red	Active when any one of the alarms in the SPECTRA-622 Section Alarm Output Control #1 and #2 registers is active.

RALM (Receive alarm)	Red	Active when any of the alarms specified in the SPECTRA-622 RPPS RALM Output Control #1 and #2 are active.
INTB (Interrupt)	Red	Active when the interrupt pin on any device is active.
OOF (out of frame)	Red	The OOF signal is high when the spectra622 is out of frame.

8 SOFTWARE INTERFACES

8.1 Memory Map

The valid range of addressable registers is shown in Table 29. All other addresses are not used. Each device datasheet contains a list of all addressable registers for that device. The register address should be added to the lower address for each device in Table 29 to determine the actual address of that register on the card.

Table 29 System Memory Map

PCI9030 Local Address Space	Local Address Range	Device	R/W	Description
CS_0	00000h to 0FFFFh	SPECTRA-622	R/W	SPECTRA-622 Registers
CS_1 (Individual TEMUX-84 chip selects generated by CPLD)	10000h to 17FFFh	TEMUX-84 #1	R/W	TEMUX-84 Registers
	18000h to 1FFFFh	TEMUX-84 #2		
	20000h to 27FFFh	TEMUX-84 #3		
	28000h to 2FFFFh	TEMUX-84 #4		
CS_2	30000h to 3 31FFFh	SBS-Lite	R/W	SBS-Lite Registers
CS_3	32000h to 3FFFFh	CPLD	R/W	CPLD Registers

8.2 Address Mapping

Within this reference design, there is a local bus on which a 16-bit device (SBS-Lite) and 8-bit devices (TEMUX-84 / SPECTRA-622) reside. Dealing with this constraint allowed for 2 possibilities.

Using the PCI9030, one can dynamically interface a 32-bit PCI bus to 8-, 16-, and 32-bit local busses. While this option would have maximized memory efficiency on the CPU side, it also would have increased the design's complexity, both in hardware and in software.

When the PCI9030 is activated, all the devices are assigned a 32-bit address space by the CPU. In the case of the 8-bit devices, the upper 24 bits of every CPU Lword are ignored. For the 16-bit device, half of all CPU Lwords are ignored. The major fault with this design choice is the waste of CPU memory. However, because the OC-12 Line Card does not require a large amount of memory space, this design choice is acceptable, considering the reduction in complexity it offers.

Address translation works as follows: For a 32-bit local bus, the PCI9030 expects all addresses to be Lword (32-bit) aligned, causing all addresses to end with '00'. Because of this, the PCI9030 does not even provide the lowest 2 local address bits on the address bus. To accommodate this, every local address is mapped to a Lword aligned boundary on the CPU side. (i.e. register 0x0011 on the SPECTRA-622 is addressed as 0x001100 on the CPU side.) Because the 3rd SPECTRA-622 register is mapped to the 12th CPU register, several CPU registers are unused. This corresponds to the ignored bits mentioned in the previous paragraph.

8.3 CPLD Operation

The Xilinx XC95288XL High performance CPLD is chosen for its high pin count. One of the main functions of the CPLD is to mimic a large switch or multiplexer. The board has the ability to support two processor configurations, the external processor using the PCI9030 and generic onboard processor. On the CPLD, one pin (JUMPER_SIG) is set to determine which of the two is used. The JUMPER_SIG pin is set high (+3.3V) when the PCI9030 is used and low (grounded) when the onboard processor is used. The setting of this pin, controls many operations that the CPLD performs. All the I/O signals from the onboard processor and PCI9030 controller are routed into the CPLD. Depending on the settings of JUMPER_SIG, the CPLD will re-route these signals from one of the processors to all other devices on the board.

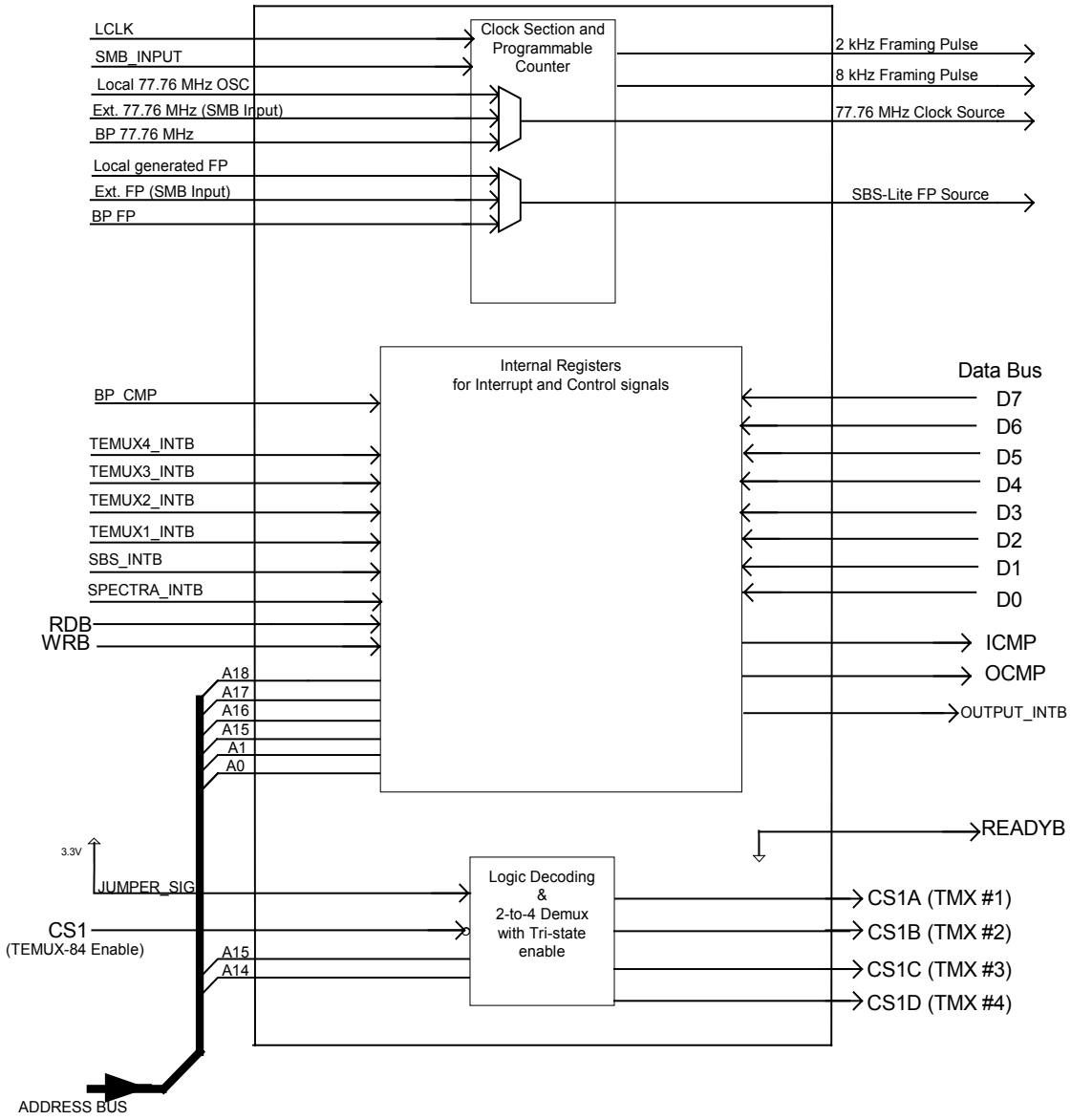
The CPLD also determines which of the three 77.76 MHz clock and 2 kHz frame pulse sources is used by the devices. The local, external and backplane sources, are fed into the CPLD and one source is used as the 77.76 MHz timing master and one is used as the global frame pulse via the setting of specified jumpers.

The OCMP and ICMP signal can also be retrieved from the backplane or generated onboard by the CPLD. Specified jumpers control these signals as well. See Table 27 for details on the jumper settings. .

The PCI9030 will perform the address decoding for the four chip selects. Table 29 shows how the chip selects are mapped to the devices. The CPLD will use the TEMUX-84 chip select to enable one of the four TEMUX-84 devices

depending on the selected address. Figure 42 shows the equivalent digital logic that is implemented inside of the CPLD.

Figure 42 - CPLD Logic Diagram with PCI9030 Activated



The READYB signal is held low because it is not required for the current memory access scheme. Reprogramming the CPLD could enable its use in the future.

The CPLD will also contain logic for monitoring the interrupts that occur on the board. When an interrupt occurs, it will be stored into a register so that the host processor may read that register to determine the origin of the interrupt. This method simplifies interrupt handling because the host processor only needs to check one address to determine the location of the interrupt. Table 30 describes the function of each bit inside of the interrupt status register.

The logical OR of all interrupt sources on the card is sent from the CPLD to the PCI9030, which is then sent over the PCI bus to the host processor.

Table 30 CPLD Interrupt Status Register

Local Address	Bit #	R/W	Description
32000h	31-6	R	0 (Not Used)
32000h	5	R	TEMUX-84 #4 Interrupt
32000h	4	R	TEMUX-84 #3 Interrupt
32000h	3	R	TEMUX-84 #2 Interrupt
32000h	2	R	TEMUX-84 #1 Interrupt
32000h	1	R	SBS-Lite Interrupt
32000h	0	R	SPECTRA-622 Interrupt

The CPLD contains a register called the SBS-Lite Control Register. This register contains bits that directly drive status lines on the SBS-Lite device. The ICMP and OCMP signal controls the selection of the connection memory page in the IMSU and OMSU (Memory Switch Unit), respectively. Table 31 shows the function of each bit inside of the SBS-Lite Control register.

Table 31 SBS-Lite Control Register

Local Address	Bit #	R/W	Description
32004h	31-3	R	0 (Not Used)
32004h	2	R/W	CMP Control Mode
32004h	1	R/W	OCMP
32004h	0	R/W	ICMP

The SBS-Lite is comprised of two connection memory pages, page 0 and 1. The incoming and outgoing CMP (where CMP refers to either the ICMP or OCMP) signal determines which page is active. When the CMP control mode bit is set to 0, the CPLD drives the CMP signal with the value that is currently in the CMP bit. When the CMP control mode bit is set to 1, The connection memory page in the SBS-Lite is altered. Please refer to the SBS-Lite datasheet [7] for further details on the SBS-Lite functions.

9 DISCLAIMER

This document is a paper reference design, and as such, has not been built or tested as of this date.

Please check the PMC-Sierra website regularly for updates to this document.

10 REFERENCES

1. ANSI, “Synchronous Optical Network (SONET) Basic Description including Multiplex Structure, Rates, and formats”, T1.105-1995.

2. PCIMG, “CompactPCI Hot Swap Specification”, May 14, 1998, Draft R1.0

3. PCI Special Interest Group, “PCI Local Bus Specification Revision 2.1”, Portland OR, June 1995.

4. PLX Technology, “PCI9030 Data Book”, April 2000, Version 1.0

5. PMC-Sierra Inc., PMC-1981162, “SONET/SDH Payload Extractor/Aligner for 622 Mbits/s”, September 2000, Issue 6.

6. PMC-Sierra Inc., PMC-1991437, “High Density 84 T1/63 E1 Framer with Integrated VT/TU Mappers and M13 Multiplexers Telecom Standard Product Data Sheet”, October 2000, Issue 3.

7. PMC-Sierra Inc., PMC-2010883, “SBS-Lite Datasheet”, Issue 1.

11 APPENDIX A: BILL OF MATERIALS

Table 32 Major Components List

REF DES	PART NUMBER	MANUFACTURER	DESCRIPTION	QTY
U2	NM93CS56LEN	FAIRCHILD SEMI	2048 BIT SERIAL EEPROM W/ DATA PROTECT AND SEQ READ DIP8	1
U3	PCI9030-AA60PI	PLX TECHNOLOGY	IC 3.3V PCI TARGET INTERFACE(32-BIT, 33MHZ, PQFP PACKAGE)	1
U8-U11	PM8316	PMC SIERRA	IC HIGH DENSITY T1/E1 FRAMER WITH INTEGRATED VT/TU MAPPER AND M13 MUX	4
U12	V23826-H18-C363	SIEMENS	IC 3.3V DC/DC SINGLE MODE 1300NM 622MBD 1X9 TRANSCEIVER	1
U15	PM8611	PMC-SIERRA	SCALABLE BANDWIDTH SERIALIZER	1
U18	PM5313	PMC-SIERRA	SONET/SDH PAYLOAD EXTRACTOR/ALIGHNER FOR 622MBITS/S	1
U26	XC95288XL-10BG256 I	XILINX	3.3 V CPLD, 288 MICROCELLS, 192 I/O PINS	1

Table 33 Bill of Materials

REF DES	PART NUMBER	MANUFACTURER	DESCRIPTION	QTY
D3	1N4148W	VISHAY/LITE- ON	SURFACE MOUNT SWITCHING DIODE	1
U19	SN74AHC540DW	TEXAS INSTRUMENTS	OCTAL BUFFER/DRIVER, 3-STATE OUTPUTS	1
J14	120786-1	AMP	Z-PACK 6 ROW HS3 BACKPLANE CONNECTOR, RIGHT ANGLE RECEPTACLE	1
C22, C23, C25, C26, C29, C30	NEWARK -- 52F019	?	MURATA NICKEL INNER ELECTRODE TYPE	6
C106	2222 370 22473	BC COMPONENTS	CAP METAL POLY PETP 100V 5% .047UF	1
C278, C279	ECU-E1C103KBQ	PANASONIC	CAP CERAMIC X7R 0402 16V 0.01UF	2
C32, C33, C79, C93-C96, C104, C129, C131, C133, C135, C139, C143, C159, C160, C217, C243, C244, C246, C247	ECU-V1H103KBV	PANASONIC	CAP CERAMIC X7R 0603 50V 0.01UF	21
C19	ECJ-1VB1E223K	PANASONIC	CAP CERAMIC X7R 0603 25V 0.022UF	1
C18	08055C473JATN	AVX	CAP CERAMIC X7R 0850 50V 0.047UF	1
C1-C12, C14, C17, C24, C31, C34-C78, C80-C87,	ECJ-1VB1C104K	PANASONIC	CAP CERAMIC X7R 0603 16V 0.1UF	214

C92, C97-C103, C105, C107-C128, C130, C132, C134, C136-C138, C140-C142, C144-C154, C157, C158, C161-C179, C190-C213, C218-C242, C245, C248-C267, C273, C276, C277				
C16	ECJ-3VB1C334K	PANASONIC	CAP CERAMIC X7R 1206 16V 0.33UF	1
C20, C21	ECE-V1AA102P	PANASONIC	CAP ELECTRO VA SMD 10V 20% 1000UF	2
C27, C28	ECS-T1AD107R	PANASONIC	CAP TANTALUM 10V 20% 100UF	2
C88-C91, C181, C269-C272, C274, C275	ECS-H1AC106R	PANASONIC	CAP TANCAPC 10V 20% 10UF	11
C155, C156	ECS-H1CD226R	PANASONIC	CAP TANCAPD 16V 20% 22UF	2
C180, C182-C189, C214-C216	ECS-H1AD336R	PANASONIC	CAP TANCAPD 10V 20% 33UF	12
C13, C15	ECS-T0JY475R	PANASONIC	CAP TANCAPA 6.3V 20% 4.7UF	2
C268	ECS-H0JD476R	PANASONIC	CAP TANCAPD 6.3V 20% 47UF	1
J3, J5	2-767004-2	AMP	CONNECTOR 38 POS VERTICAL .025" TO .64" SMD MICTOR	2
P1	PART OF PCB	PART OF PCB	PART OF PCB COMPACT PCI ESD STRIP	1
J8	DIGI-KEY -- A2100-ND	?	RIGHT ANGLE	1
J4	PZC36DAAN X 25/36	SULLINS	HEADER 25X2 GOLD 0.1" SPACING	1
J12, J13	PZC36SAAN	SULLINS	CONN HEADER 8 PIN	2
J9	PZC36DAAN	SULLINS	CONN HEADER 2 ROW 0.1"X0.1" 2X16	1
J2	53047-0310	MOLEX	PITCH HEADER - STRAIGHT SQUARE 3 ROW 1 POSITION/ROW	1
J10	PZC36DAAN	SULLIN	HEADER 2X8 100 MIL	1
Q4, Q5	IRL3502S	INTERNATIONA L RECTIFIER	0.007 OHM, 20 V, HEXFET POWER MOSFET	2
D1	PANASONIC LNG91LCFB	?	T-1 3/4 LED BLUE VERTICAL PCB MOUNT STATIC SENSITIVE	1
U4	LTC1422CS8	LINEAR TECHNOLOGY	HOT SWAP CONTROLLER	1
Q1, Q3	MMBT3904LT1	MOTOROLA	GENERAL PURPOSE TRANSISTOR	2
M1	MOUNTING HOLE	N/A	MOUNTING HOLE .150" DIA	1
J6	NANOENGINE/5348 1- 1609	BRIGHTSTAR ENGINEERING/ MOLEX	NANOENGINE SINGLE BOARD COMPUTER WITH MOLEX_7MM MATING CONNECTOR	1
U2	NM93CS56LEN	FAIRCHILD SEMI	2048 BIT SERIAL EEPROM W/ DATA PROTECT AND SEQ READ DIP8	1

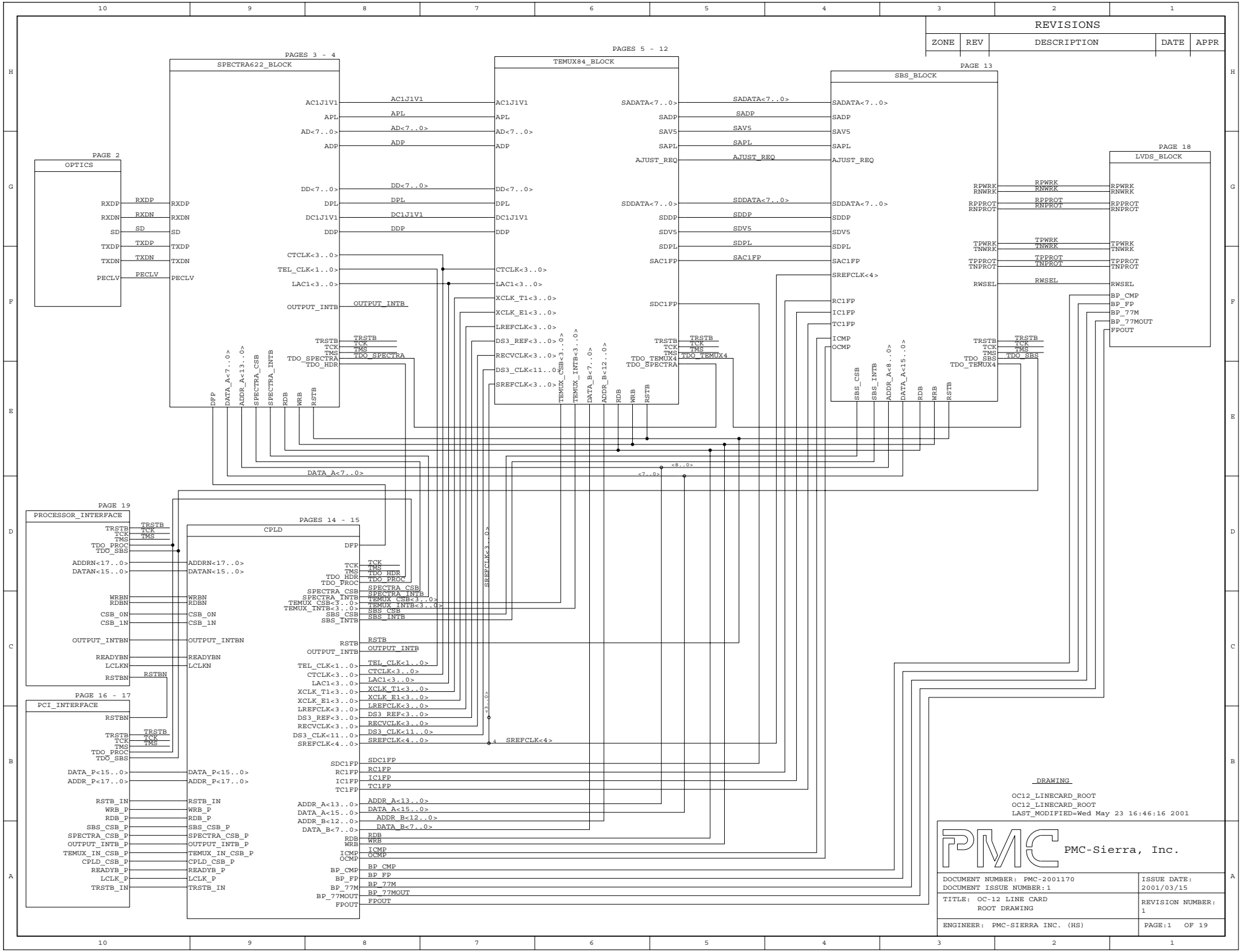
Y2	EH2645TS-37.056M	ECLIPTEK	OSCILLATOR 37.056MHZ 3.3V [TOL= 32PPM] [TEMP= 0-70C] [DUTY= 10%]	1
Y3	EH2645TS-49.152M	ECLIPTEK	OSCILLATOR 49.152MHZ 3.3V [TOL= 32PPM] [TEMP= 0-70C] [DUTY= 10%]	1
Y6	EH2620TTS-77.760M	ECLIPTEK	OSCILLATOR 77.760MHZ 3.3V [TOL= 20PPM] [TEMP= 0-70C] [DUTY= 5%]	1
Y7	EP2645TTS-44.736M	ECLIPTEK	OSCILLATOR, 44.736MHZ, 3.3V, 50PPM	1
Y4	EP2645TTS-51.840M	ECLIPTEK	OSCILLATOR, 51.84MHZ, 3.3V, 50PPM	1
Y1	CONNOR WINFIELD -- EE14-541	?	77.76 MHZ, LVPECL OSCILLATOR, 20 PPM, 3.3V	1
SW1	DIGIKEY -- P8009S-ND	?	VERT PCB MOUNT SPST PUSH BUTTOM	1
U3	PCI9030-AA60PI	PLX TECHNOLOGY	IC 3.3V PCI TARGET INTERFACE(32-BIT, 33MHZ, PQFP PACKAGE)	1
U1, U13, U14, U20, U23, U24	PI49FCT3805CQ	PERICOM	IC 3.3V 2X1:5 CMOS CLOCK DRIVER SPEED-GRADE-C QSOP20	6
R40, R63	ERJ-6RQJR47V	PANASONIC	RES 0805 1/10W 5% .47 OHM	2
R24, R25, R61, R62	ERJ-3GSY0R00V	PANASONIC	RES 0603 1/16W 5% ZERO OHM	4
R31, R32	WSL2512-R01-1	VISHAY	RES 2512 1W 1% 0.01 OHM	2
R12, R21, R34, R75, R76	ERJ-3GSYJ102V	PANASONIC	RES 0603 1/16W 5% 1.0K OHM	5
R14	ERJ-3GSYJ122V	PANASONIC	RES 0603 1/16W 5% 1.2K OHM	1
R16, R33, R35	ERJ-3GSYJ100V	PANASONIC	RES 0603 1/16W 5% 10 OHM	3
R27, R29, R54, R135-R141	ERJ-3GSYJ101V	PANASONIC	RES 0603 1/16W 5% 100 OHM	10
R10	ERJ-3GSYJ104V	PANASONIC	RES 0603 1/16W 5% 100K OHM	1
R1-R3	ERJ-6GEYJ106V	PANASONIC	RES 0805 1/10W 5% 10M OHM	3
R56, R57, R60	ERJ-3GSYJ150V	PANASONIC	RES 0603 1/16W 5% 15 OHM	3
R20, R421, R422	ERJ-3GSYJ151V	PANASONIC	RES 0603 1/16W 5% 150 OHM	3
R68	ERJ-3EKF2001V	PANASONIC	RES 0603 1/16W 5% 2.00K OHM	1
R81, R82	ERJ-3GSYJ2R2V	PANASONIC	RES 0603 1/16W 5% 2.2 OHM	2
R38	ERJ-3EKF2431V	PANASONIC	RES 0603 1/16W 1% 2.43K OHM	1
R47	ERJ-3GSYJ221V	PANASONIC	RES 0603 1/16W 5% 220 OHM	1
R17	ERJ-3GSYJ271V	PANASONIC	RES 0603 1/16W 5% 270 OHM	1
R13	ERJ-3GSYJ302V	PANASONIC	RES 0603 1/16W 5% 3.0K OHM	1
R83	ERJ-3EKF3161V	PANASONIC	RES 0603 1/16W 1% 3.16K OHM	1
R58, R59	ERJ-6RQF3R3V	PANASONIC	RES 0805 1/10W 1% 3.3 OHM	2
R44, R46, R67, R69, R70, R94, R113, R604-R606, R608-R612	ERJ-3GSYJ331V	PANASONIC	RES 0603 1/16W 5% 330 OHM	15
R52, R53	ERJ-3GSYJ4R7V	PANASONIC	RES 0603 1/16W 5% 4.7 OHM	2
R4-R9, R11, R26, R28, R30, R39,	ERJ-3GSYJ472V	PANASONIC	RES 0603 1/16W 5% 4.7K OHM	33

R41-R43, R45, R48-R51, R55, R64-R66, R89, R93, R95-R97, R111, R112, R119, R142, R271				
R15, R18, R19, R22, R23, R71, R72	ERJ-3GEYJ470V	PANASONIC	47 OHM SINGLE RESISTOR	7
R84, R85	ERJ-3EKF49R9V	PANASONIC	RES 0603 1/16W 1% 49.9 OHM	2
R37	ERJ-3EKF6811V	PANASONIC	RES 0603 1/16W 1% 6.81K OHM	1
R88	ERJ-3EKF63R4V	PANASONIC	RES 0603 1/16W 1% 63.4 OHM	1
R36	DIGI-KEY -- P<VALUE>ACT-ND	?	?	1
RN1-RN13	PANASONIC -- EXB-V8V100JV	?	?	13
RN233-RN23 8	PANASONIC -- EXB-V8V103JV	?	?	6
RN18-RN25, RN40-RN42, RN48-RN53, RN55-RN60, RN62, RN63, RN66, RN79, RN86, RN87, RN90, RN91, RN94, RN95, RN119, RN120, RN136, RN139, RN140, RN147-RN15 6, RN158, RN159, RN163, RN166-RN16 9, RN173, RN174, RN176, RN195, RN203, RN205-RN20 8, RN215-RN22 2	DIGI-KEY -- Y4<VALUE CODE>-ND	?	?	72
RN27	PANASONIC -- EXB-V8V330JV	?	?	1
RN38, RN45, RN47, RN68-RN72, RN74, RN77, RN78, RN80-RN85, RN88, RN89,	DIGI-KEY -- Y4<VALUE CODE>-ND	?	?	82

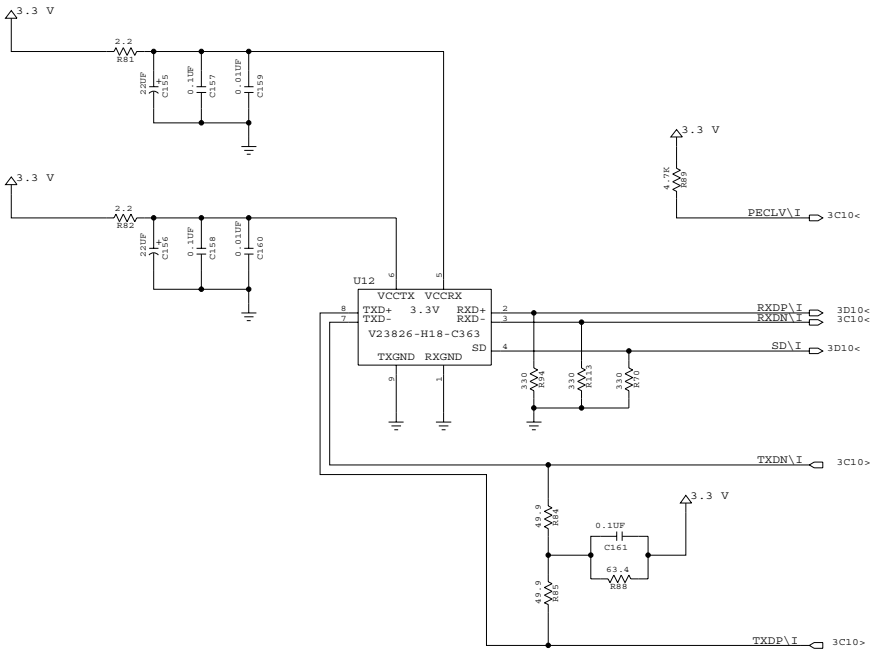
RN96-RN104 , RN108-RN11 3, RN116-RN11 8, RN124-RN13 1, RN137, RN138, RN157, RN160-RN16 2, RN164, RN165, RN170-RN17 2, RN175, RN177-RN18 3, RN185-RN18 8, RN197, RN204, RN211, RN224, RN228, RN265-RN27 3				
RN14-RN17, RN28-RN37, RN39, RN43, RN44, RN54, RN61, RN67, RN114, RN115, RN134, RN141, RN142, RN189-RN19 3, RN196, RN199, RN232, RN239, RN248	PANASONIC -- EXB-V8V472JV	?	?	35
RN26, RN73, RN75, RN76, RN105-RN10 7, RN133, RN135, RN143, RN212-RN21 4, RN223, RN225, RN226	DIGI-KEY -- Y4<VALUE CODE>-ND	?	?	16
RN46, RN64, RN65, RN92, RN93, RN121-RN12 3, RN132, RN144-RN14 6, RN184, RN194, RN198, RN200-RN20 2, RN209, RN210	PANASONIC -- EXB2HVR000V	?	?	20
J7	STEWART OR AMP	?	CONNECTOR SHIELDED RJ45	1
U15	PM8611	PMC-SIERRA	SCALABLE BANDWIDTH SERIALIZER	1
J11, J15	903-499J-51P2	AMPHENOL	SMB VERTICAL GOLD	2
U18	PM5313	PMC-SIERRA	SONET/SDH PAYLOAD	1

			EXTRACTOR/ALIGHNER FOR 622MBITS/S	
D2	SSF-LXH5147LGD	LUMEX	LED QUAD GREEN HORIZONTAL	1
D6, D7	SSF-LXH5147LID	LUMEX	LED QUAD RED HORIZONTAL	2
U6	TC74LVX08FN	TOSHIBA	IC HIGHSPEED CMOS QUAD 2 INPUT AND GATE SO14NB	1
U8-U11	PM8316	PMC SIERRA	IC HIGH DENSITY T1/E1 FRAMER WITH INTEGRATED VT/TU MAPPER AND M13 MUX	4
U5	1.09E+08	LUCENT	TITANIA POWER MODULE, 3.3VDC AND 5.0VDC INPUT, 1.5VDC TO 3.3VDC OUTPUT 6A	1
U7	1.09E+08	LUCENT	TITANIA POWER MODULE, 3.3VDC AND 5.0VDC INPUT, 1.5VDC TO 3.3VDC OUTPUT 6A	1
U12	V23826-H18-C363	SIEMENS	IC 3.3V DC/DC SINGLE MODE 1300NM 622MBD 1X9 TRANSCEIVER	1
U26	XC95288XL-10BG256 I	XILINX	3.3 V CPLD, 288 MICROCELLS, 192 I/O PINS	1
J1	352068-1	AMP	CONNECTOR ZPACK CPCI 2MM HM 110 POS. TYPE A WITH GND SHIELD	1

12 APPENDIX B: SCHEMATICS


REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPR
PAGE 2
OPTICS
RXDP
RXDN
SD
TXDP
TXDN
PECLV
PAGES 3 - 4
SPECTRA622_BLOCK
AC1J1V1
APL
AD<7..0>
ADP
DD<7..0>
DPL
DC1J1V1
DDP
CTCLK<3..0>
TEL_CLK<1..0>
LAC1<3..0>
OUTPUT_INTB
TRSTB
TCK
TMS
TDO_SPECTRA
TDO_HDR
DFP
DATA_A<7..0>
ADDR_A<13..0>
SPECTRA_CSB
SPECTRA_INTB
RDB
WRB
RSTB
PAGES 5 - 12
TEMUX84_BLOCK
XCLK_T1<3..0>
XCLK_E1<3..0>
LREFCLK<3..0>
DS3_REF<3..0>
RECVCLK<3..0>
DS3_CLK<11..0>
SREFCLK<3..0>
TEMUX_CSB<3..0>
TEMUX_INTB<3..0>
DATA_B<7..0>
ADDR_B<12..0>
PAGE 13
SBS_BLOCK
SADATA<7..0>
SADP
SAV5
SAPL
AJUST_REQ
SDDATA<7..0>
SDDP
SDV5
SDPL
SAC1FP
SDC1FP
SREFCLK<4>
RC1FP
IC1FP
TC1FP
ICMP
OCMP
TDO_TEMUX4
TDO_SBS
SBS_CSB
SBS_INTB
ADDR_A<8..0>
DATA_A<15..0>
PAGE 18
LVDS_BLOCK
RPWRK
RNWRK
RPPROT
RNPROT
TPWRK
TNWRK
TPPROT
TNPROT
RWSEL
BP_CMP
BP_FP
BP_77M
BP_77MOUT
FPOUT
PAGE 19
PROCESSOR_INTERFACE
TDO_PROC
ADDRN<17..0>
DATAN<15..0>
WRBN
RDBN
CSB_0N
CSB_1N
OUTPUT_INTBN
READYBN
LCLKN
RSTBN
PAGES 14 - 15
CPLD
PAGE 16 - 17
PCI_INTERFACE
DATA_P<15..0>
ADDR_P<17..0>
RSTB_IN
WRB_P
RDB_P
SBS_CSB_P
SPECTRA_CSB_P
OUTPUT_INTB_P
TEMUX_IN_CSB_P
CPLD_CSB_P
READYB_P
LCLK_P
TRSTB_IN
DRAWING
OC12_LINECARD_ROOT
OC12_LINECARD_ROOT
LAST_MODIFIED=Wed May 23 16:46:16 2001
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-2001170
DOCUMENT ISSUE NUMBER:1
ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD ROOT DRAWING
REVISION NUMBER: 1
ENGINEER: PMC-SIERRA INC. (HS)
PAGE:1 OF 19

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

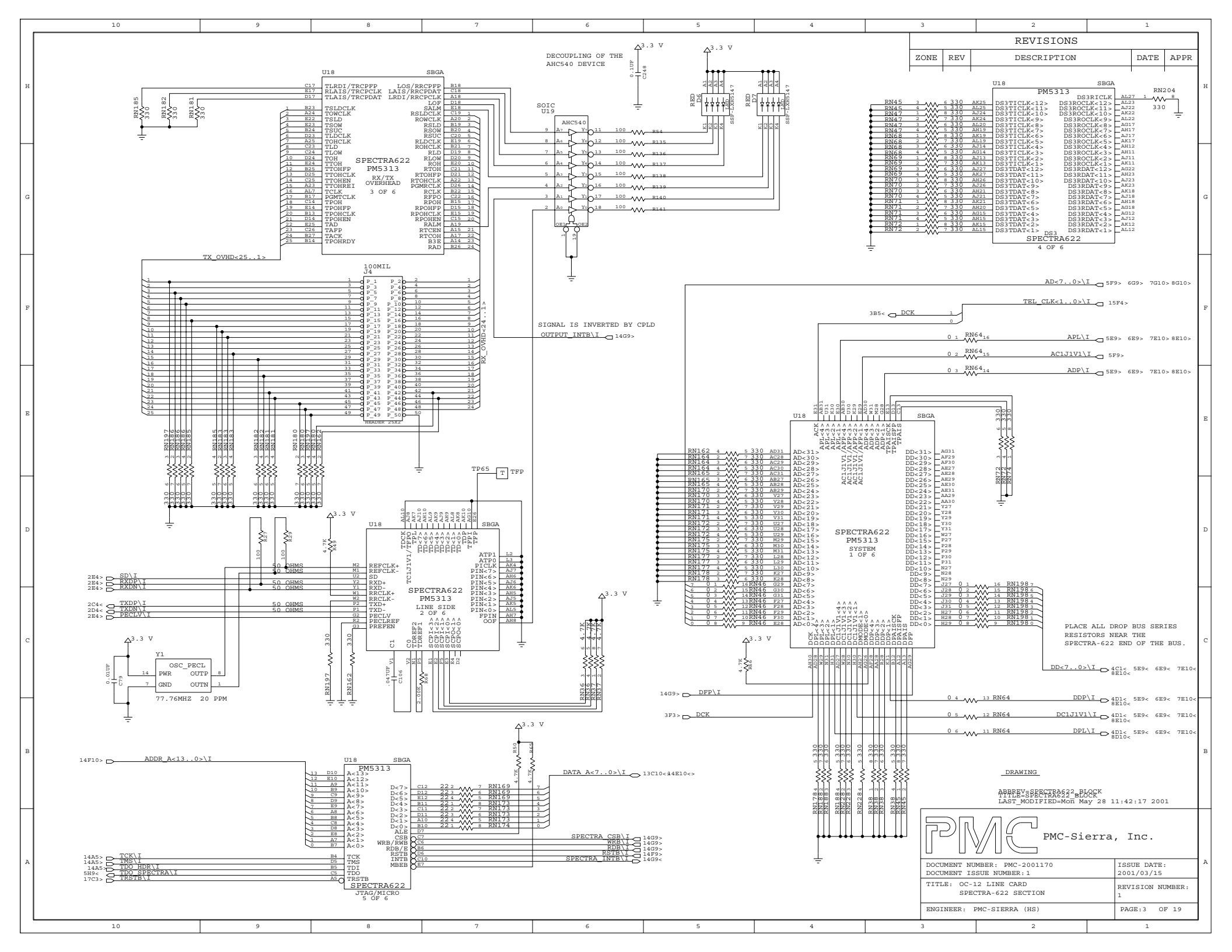


DRAWING

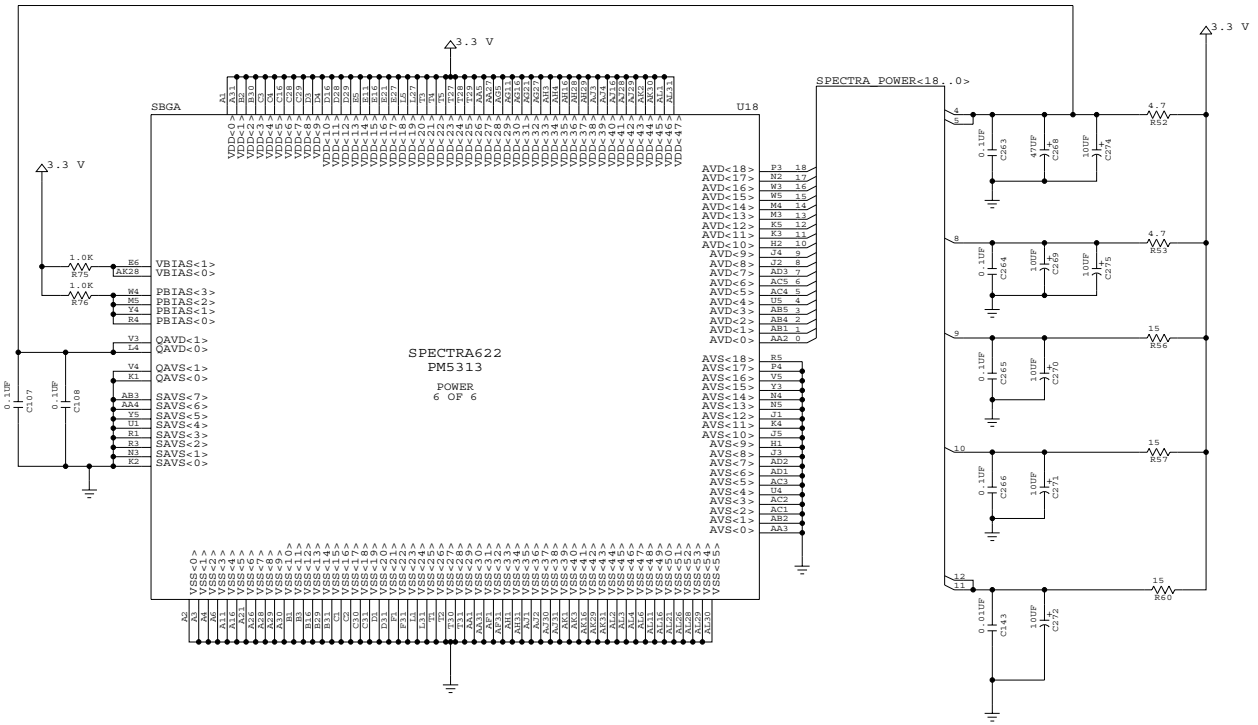
ABBREV=OPTICS
TITLE=OPTICS
LAST_MODIFIED=Mon May 28 11:42:54 2001

PMC-Sierra, Inc.

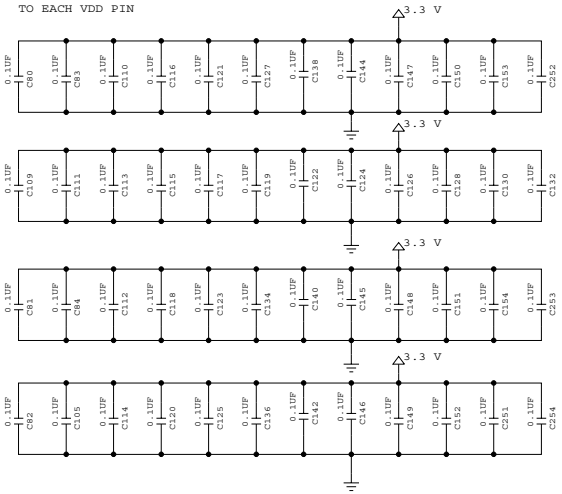
DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD OPTICAL TRANSCEIVER	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA INC	PAGE:2 OF 19


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPR
DECOUPLING OF THE AHC540 DEVICE
SIGNAL IS INVERTED BY CPLD
OUTPUT_INTB\I
PLACE ALL DROP BUS SERIES RESISTORS NEAR THE SPECTRA-622 END OF THE BUS.
DRAWING
ABBREV=SPECTRA622_BLOCK
TITLE=SPECTRA622_BLOCK
LAST_MODIFIED=Mon May 28 11:42:17 2001
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-2001170
DOCUMENT ISSUE NUMBER:1
ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD SPECTRA-622 SECTION
REVISION NUMBER: 1
ENGINEER: PMC-SIERRA (HS)
PAGE:3 OF 19

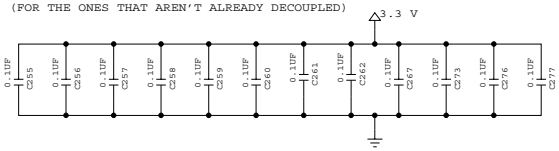
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



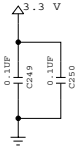
DECOUPLING FOR SPECTRA-622.
PLACE ONE 0.1UF CAP AS CLOSE AS POSSIBLE
TO EACH VDD PIN



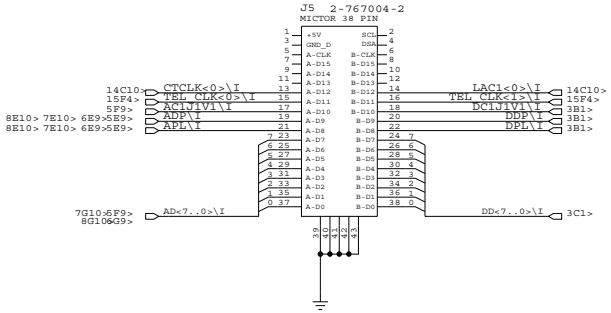
DECOUPLING FOR SPECTRA-622.
PLACE ONE 0.1UF CAP AS CLOSE AS POSSIBLE
TO EACH OF THE ANALOG AVD PINS
(FOR THE ONES THAT AREN'T ALREADY DECOUPLED)



DECOUPLING CAPS PLACED FOR
3.3V BIASING PINS



SPECTRA-622 TO TEMUX-84S
TELECOM BUS



DRAWING

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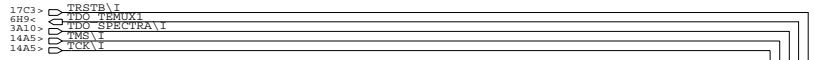
SPECTRA622-BLOCK
LAST_MODIFIED=Mon May 28 11:42:22 2001

PMC-Sierra, Inc.

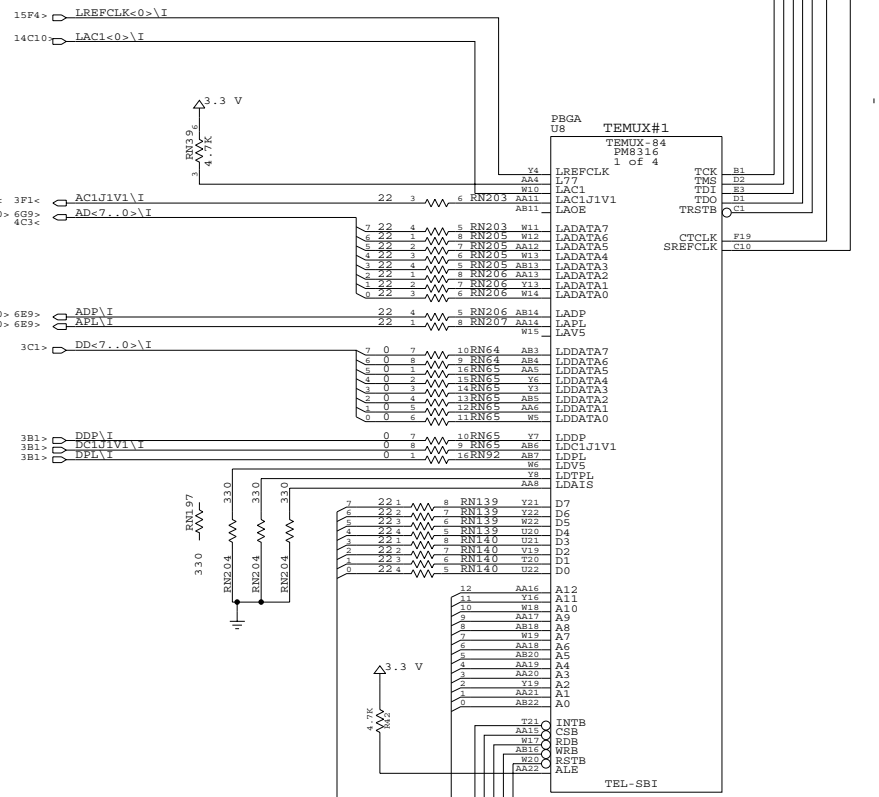
DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD SPECTRA POWER / CONNECTORS	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA (HS)	PAGE:4 OF 19

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

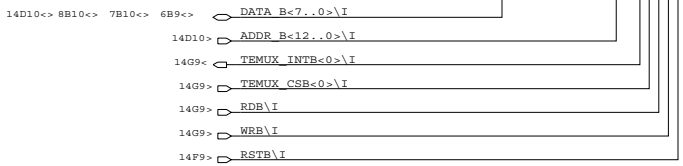
JTAG INTERFACE



TELECOM BUS



MICROPROCESSOR INTERFACE



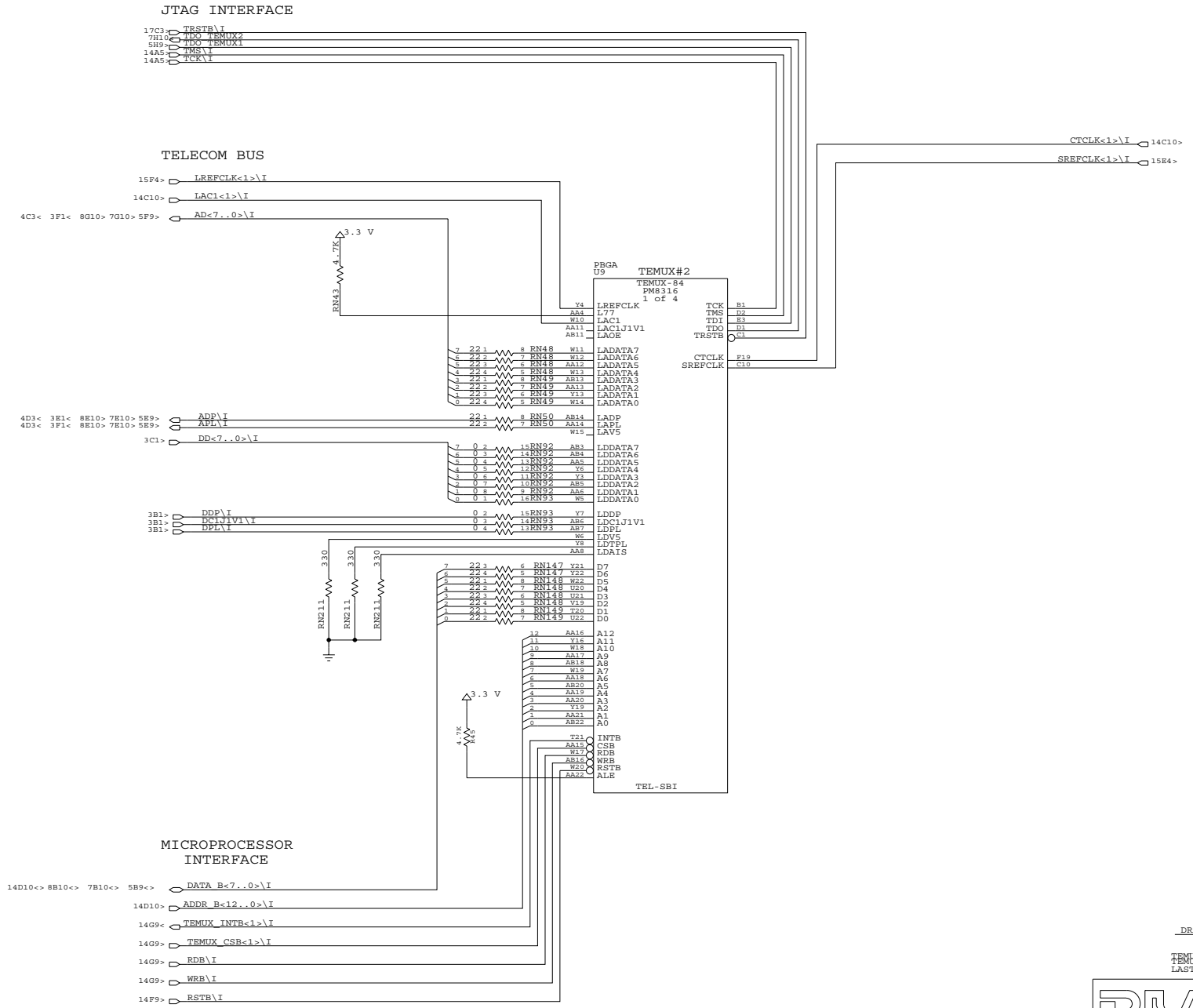
DRAWING

TEMUX84_BLOCK
TEMUX84_BLOCK
LAST_MODIFIED=Mon May 28 11:42:25 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD TEMUX-84 #1 TELECOM / MICRO	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA (HS)	PAGE:5 OF 19

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DRAWING

TEMUX84_BLOCK
TEMUX84-BLOCK
LAST_MODIFIED=Mon May 28 11:42:27 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD TEMUX-84 #2 TELECOM / MICRO	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA (HS)	PAGE:6 OF 19

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

JTAG INTERFACE

17C3> TRSTB\I
8H10> TDO_TEMUX3
6H9> TDO_TEMUX2
14A5> TMS\I
14A5> TCK\I

CTCLK<2>\I 14C10>
SREFCLK<2>\I 15E4>

TELECOM BUS

15F4> LREFCLK<2>\I
14C10> LAC1<2>\I
4C3< 3F1< 8G10>6G9> 5F9> AD<7..0>\I

3.3 V
RN54 4.7K

PBGA
U10 TEMUX#3
TEMUX-84
PM8316
1 of 4

		Y4	LREFCLK	TCK	B1
		AA4	L77	TMS	D2
		W10	LAC1	TDI	E3
		AA11	LAC1J1V1	TDO	D1
		AB11	LAOE	TRSTB	C1
				CTCLK	F19
				SREFCLK	C10
7	22 4 5	RN53	W11	LADATA7	
6	22 1 8	RN55	W12	LADATA6	
5	22 2 7	RN55	AA12	LADATA5	
4	22 3 6	RN55	W13	LADATA4	
3	22 4 5	RN55	AB13	LADATA3	
2	22 1 8	RN56	AA13	LADATA2	
1	22 2 7	RN56	Y13	LADATA1	
0	22 3 6	RN56	W14	LADATA0	

4D3< 3E1< 8E10>6E9> 5E9 ADP\I
4D3< 3F1< 8E10>6E9> 5E9 APL\I

22 4	5	RN56	AB14	LADP
22 1	8	RN57	AA14	LAPL
			W15	LAV5

3C1> DD<7..0>\I

7	0 5	12	RN93 AB3	LDDATA7
6	0 6	11	RN93 AB4	LDDATA6
5	0 7	10	RN93 AA5	LDDATA5
4	0 8	9	RN93 Y6	LDDATA4
3	0 1	16	RN144 Y3	LDDATA3
2	0 2	15	RN144 AB5	LDDATA2
1	0 3	14	RN144 AA6	LDDATA1
0	0 4	13	RN144 W5	LDDATA0

3B1> DDP\I
3B1> DC1J1V1\I
3B1> DPL\I

0	5	12	RN144 Y7	LDDP
0	6	11	RN144 AB6	LDC1J1V1
0	7	10	RN144 AB7	LDPL
			W6	LDV5
			Y9	LDTPL
			AA8	LDAIS

330 RN211
330 RN224
330 RN224

7	22 4 5	RN152	Y21	D7
6	22 1 8	RN153	Y22	D6
5	22 2 7	RN153	W22	D5
4	22 1 6	RN153	U20	D4
3	22 4 5	RN153	U21	D3
2	22 1 8	RN154	V19	D2
1	22 2 7	RN154	T20	D1
0	22 3 6	RN154	U22	D0

12	AA16	A12	
11	Y16	A11	
10	W18	A10	
9	AA17	A9	
8	AB18	A8	
7	W19	A7	
6	AA18	A6	
5	AB20	A5	
4	AA19	A4	
3	AA20	A3	
2	Y19	A2	
1	AA21	A1	
0	AB22	A0	

3.3 V
4.7K R48

T21		INTB
AA15		CSB
W17		RDB
AB15		WRB
W20		RSTB
AA22		ALE

TEL-SBI

MICROPROCESSOR INTERFACE

14D10<> 8B10<> 6B9<> 5B9<> DATA_B<7..0>\I
14D10> ADDR_B<12..0>\I
14G9< TEMUX_INTB<2>\I
14G9> TEMUX_CSB<2>\I
14G9> RDB\I
14G9> WRB\I
14F9> RSTB\I

DRAWING

TEMUX84_BLOCK
TEMUX84_BLOCK
LAST_MODIFIED=Mon May 28 11:42:29 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINECARD TEMUX-84 #3 TELECOM / MICRO	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA (HS)	PAGE:7 OF 19

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

JTAG INTERFACE

17C3> TRSTB\I
13B1> TDO_TEMUX4\I
7H10> TDO_TEMUX3
14A5> TMS\I
14A5> TCK\I

CTCLK<3>\I 14C10>
SREFCLK<3>\I 15E4>

TELECOM BUS

15F4> LREFCLK<3>\I
14C10> LAC1<3>\I
4C3< 3F1< 7G10>6G9> 5F9> AD<7..0>\I
4D3< 3E1< 7E10>6E9> 5E9> ADP\I
4D3< 3F1< 7E10>6E9> 5E9> APL\I
3C1> DD<7..0>\I
3B1> DDP\I
3B1> DC1J1V1\I
3B1> DPL\I

3.3 V
RN61 4.7K

PBGA
U11 TEMUX#4
TEMUX-84
PM8316
1 of 4

Y4	LREFCLK	TCK	B1
AA4	L77	TMS	D2
W10	LAC1	TDI	E3
AA11	LAC1J1V1	TDO	D1
AB11	LAOE	TRSTB	C1
W11	LADATA7		
W12	LADATA6	CTCLK	F19
AA12	LADATA5	SREFCLK	C10
W13	LADATA4		
AB13	LADATA3		
AA13	LADATA2		
Y13	LADATA1		
W14	LADATA0		
AB14	LADP		
AA14	LAPL		
W15	LAV5		
AB3	LDDATA7		
AB4	LDDATA6		
AA5	LDDATA5		
Y6	LDDATA4		
Y3	LDDATA3		
AB5	LDDATA2		
AA6	LDDATA1		
W5	LDDATA0		
Y7	LDDP		
AB6	LDC1J1V1		
AB7	LDPL		
W6	LDV5		
Y8	LDTPL		
AA8	LDAIS		
Y21	D7		
Y22	D6		
W22	D5		
U20	D4		
U21	D3		
V19	D2		
T20	D1		
U22	D0		
AA16	A12		
Y16	A11		
W18	A10		
AA17	A9		
AB18	A8		
W19	A7		
AA18	A6		
AB20	A5		
AA19	A4		
AA20	A3		
Y19	A2		
AA21	A1		
AB22	A0		
T21	INTB		
AA15	CSB		
W17	RDB		
AB16	WRB		
W20	RSTB		
AA22	ALE		

TEL-SBI

RN224 330
RN224 330
RN228 330

3.3 V
4.7K RS1

MICROPROCESSOR INTERFACE

14D10<> 7B10<> 6B9<> 5B9<> DATA_B<7..0>\I
14D10> ADDR_B<12..0>\I
14G9< TEMUX_INTB<3>\I
14G9> TEMUX_CSB<3>\I
14G9> RDB\I
14G9> WRB\I
14F9> RSTB\I

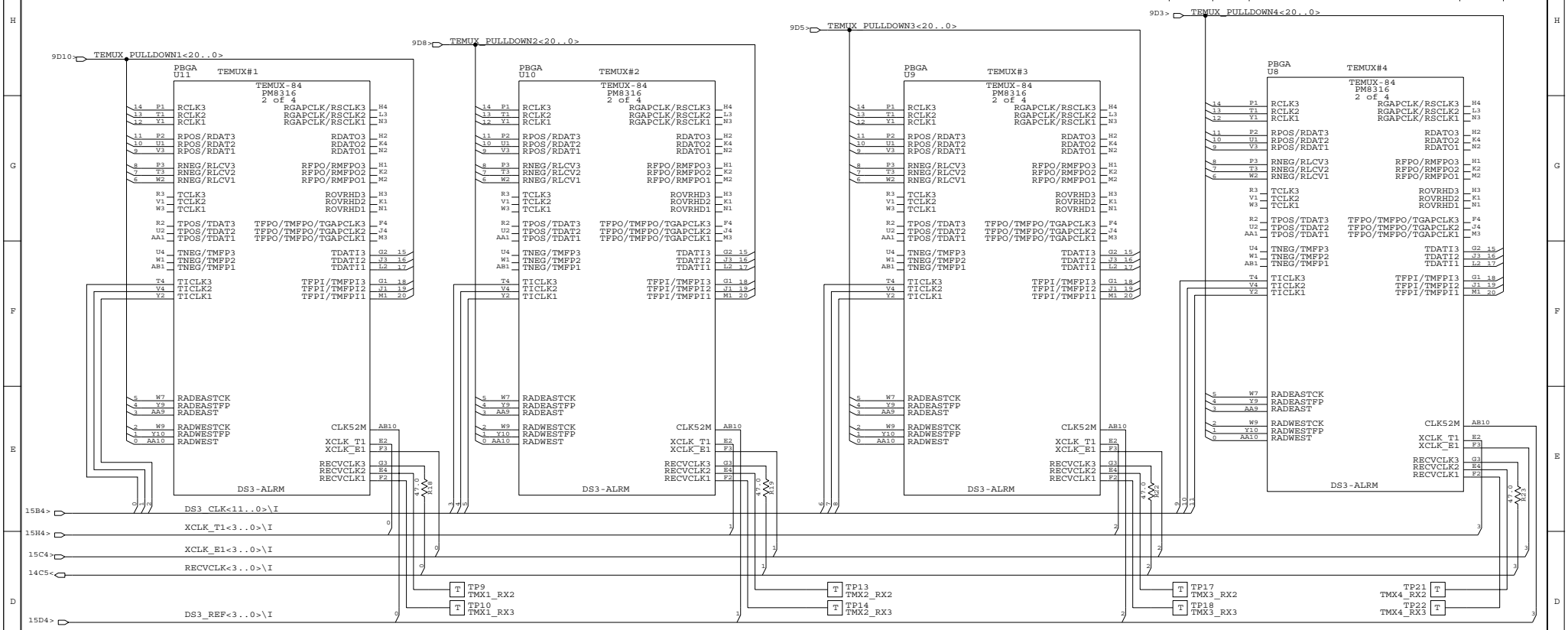
DRAWING

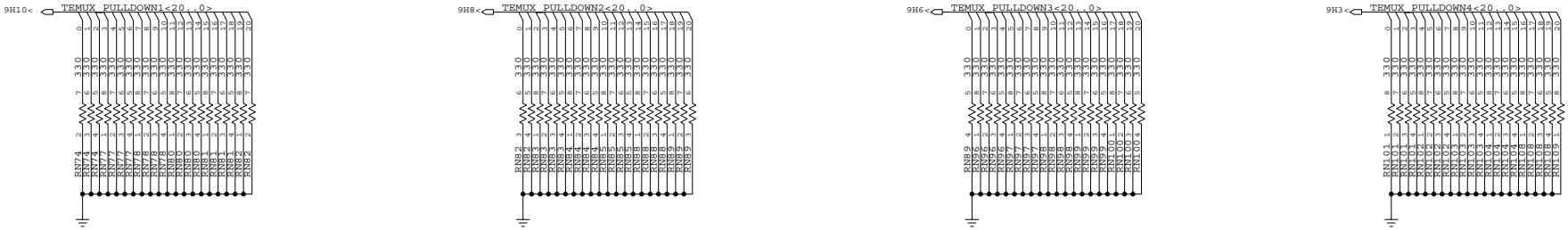
TEMUX84_BLOCK
TEMUX84-BLOCK
LAST_MODIFIED=Mon May 28 11:42:31 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD TEMUX-84 #4 TELECOM / MICRO	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA (HS)	PAGE:8 OF 19

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR





DRAWING

ABBREV=TEMUX84_BLOCK
TITLE=TEMUX84 BLOCK
LAST_MODIFIED=Mon May 28 11:42:34 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD TEMUX-84 DS3	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA INC (HS)	PAGE:9 OF 19

SBI DROP

SDV5\I
SDPL\I
SDDP\I
SDDATA<7..0>\I
AJUST_REQ\I
SDC1FP\I

PBGA
U11
TEMUX#1
TEMUX-84
PM8316
3 of 4

CMV8MCLK
CMVFPC
CMVFPB
MVID21
MVID20
MVID19
MVID18
MVID17
MVID16
MVID15
MVID14/SDV5
MVID13/SDPL
MVID12/SDDP
MVID11/SDDATA7
MVID10/SDDATA6
MVID9/SDDATA5
MVID8/SDDATA4
MVID7/SDDATA3
MVID6/SDDATA2
MVID5/SDDATA1
MVID4/SDDATA0
MVID3/SAJUST_REQ
MVID2/SBIACT
MVID1/SDC1FP
CASID21
CASID20
CASID19
CASID18
CASID17
CASID16/EFBWDAT3
CASID15/EFBWEN3
CASID14
CASID13
CASID12
CASID11
CASID10
CASID9/EFBWDAT2
CASID8/EFBWEN2
CASID7
CASID6
CASID5
CASID4
CASID3
CASID2/EFBWDAT1
CASID1/EFBWEN1
CCSID3
CCSID2
CCSID1
TS0ID
MVED21
MVED20
MVED19
MVED18
MVED17/SBIDET1
MVED16/SBIDET0
MVED15/SAV5
MVED14/SAPL
MVED13/SADP
MVED12/SADATA7
MVED11/SADATA6
MVED10/SADATA5
MVED9/SADATA4
MVED8/SADATA3
MVED7/SADATA2
MVED6/SADATA1
MVED5/SADATA0
MVED4/SAC1FP
MVED3/S77
MVED2
MVED1
CASED21
CASED20
CASED19/EFBWDREQ3
CASED18/EFBWCLK3
CASED17/IFBWEN3
CASED16/IFBWDAT3
CASED15/IFBWCLK3
CASED14
CASED13
CASED12/EFBWDREQ2
CASED11/EFBWCLK2
CASED10/IFBWEN2
CASED9/IFBWDAT2
CASED8/IFBWCLK2
CASED7
CASED6
CASED5/EFBWDREQ1
CASED4/EFBWCLK1
CASED3/IFBWEN1
CASED2/IFBWDAT1
CASED1/IFBWCLK1
CCSED3
CCSED2
CCSED1

RN154 RN147 RN147 RN53 RN53 RN57 RN57 RN152 RN152 RN152 RN149 — 22

H-MVIP

3.3 V
4.7K
RN44

H-MVIP_PULLDOWN1<34..0>

SBI ADD
SAV5\I
SAPL\I
SADP\I
SADATA<7..0>\I
SAC1FP\I
13D10>

SBI DROP

SDV5\I
SDPL\I
SDDP\I
SDDATA<7..0>\I
AJUST_REQ\I
SDC1FP\I

PBGA
U10
TEMUX#2
TEMUX-84
PM8316
3 of 4

RN58 RN59 RN51 RN52 RN52 RN58 RN59 — 22

H-MVIP

3.3 V
4.7K
RN44

H-MVIP_PULLDOWN2<34..0>

RN184 RN184 RN194 RN194 RN194 RN194 RN200 RN200 — 0

SBI ADD
SAV5\I
SAPL\I
SADP\I
SADATA<7..0>\I
SAC1FP\I
13D10>

REVISIONS

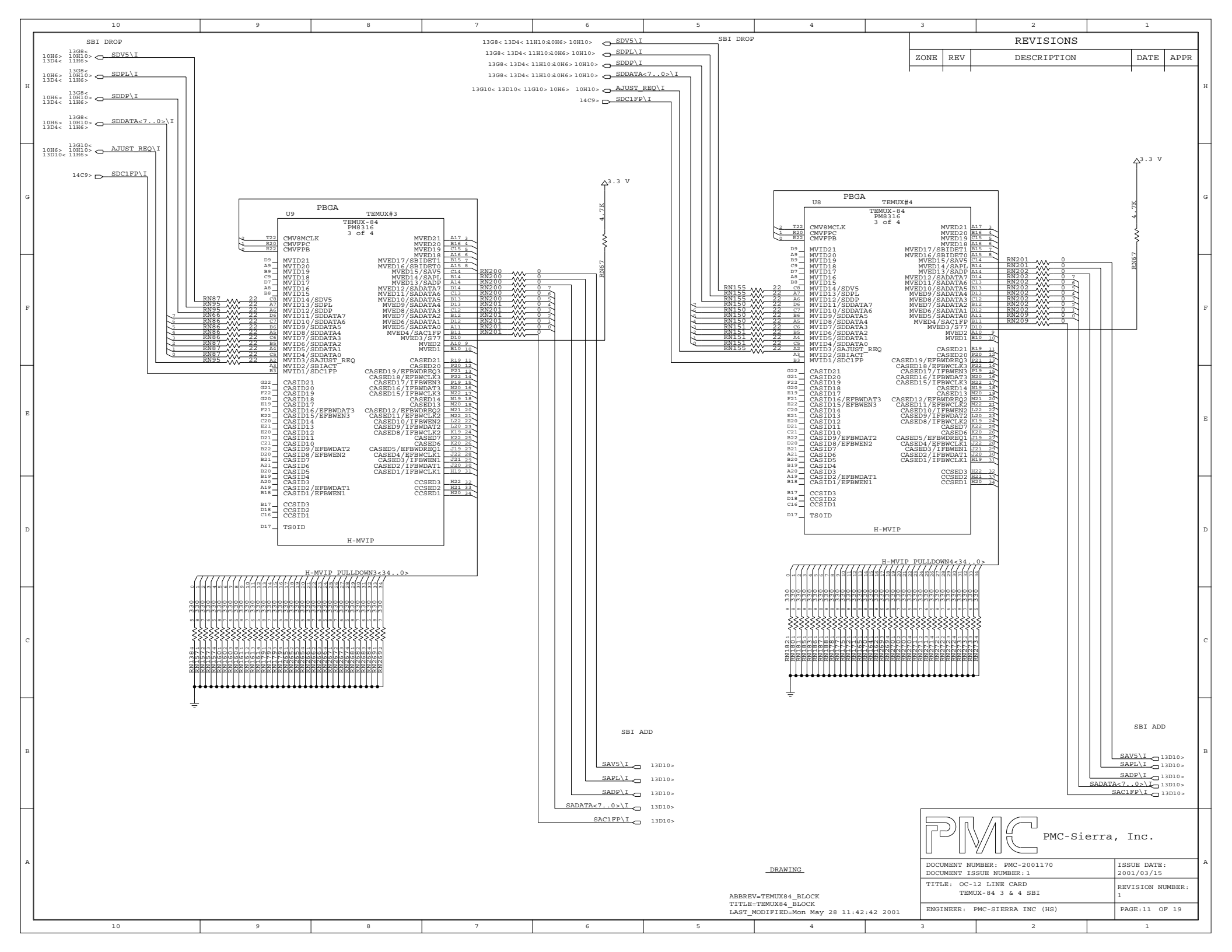
ZONE	REV	DESCRIPTION	DATE	APPR

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD TEMUX-84 1 & 2 SBI	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA (HS)	PAGE:10 OF 19

DRAWING

ABBREV=TEMUX84_BLOCK
TITLE=TEMUX84_BLOCK
LAST_MODIFIED=Mon May 28 11:42:38 2001



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

DRAWING

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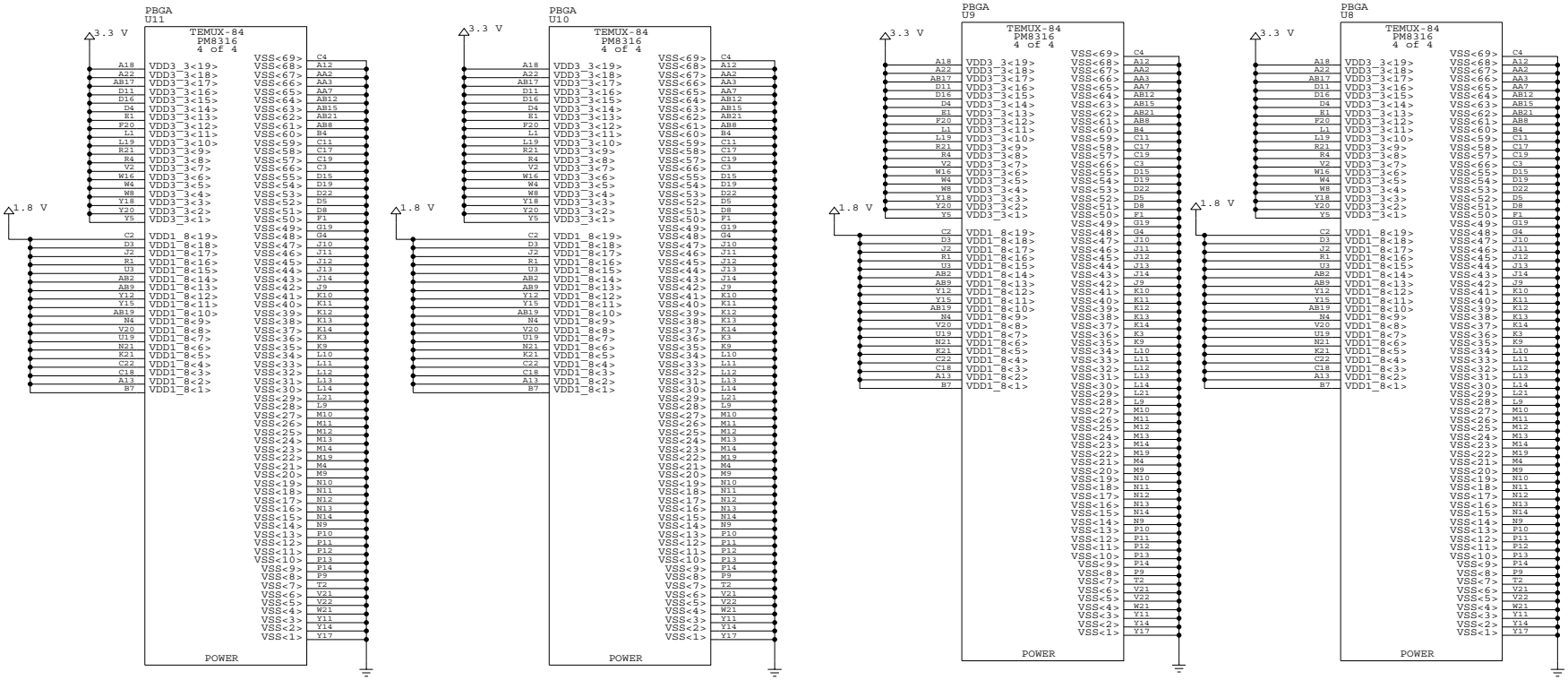
LAST_MODIFIED=Mon May 28 11:42:42 2001

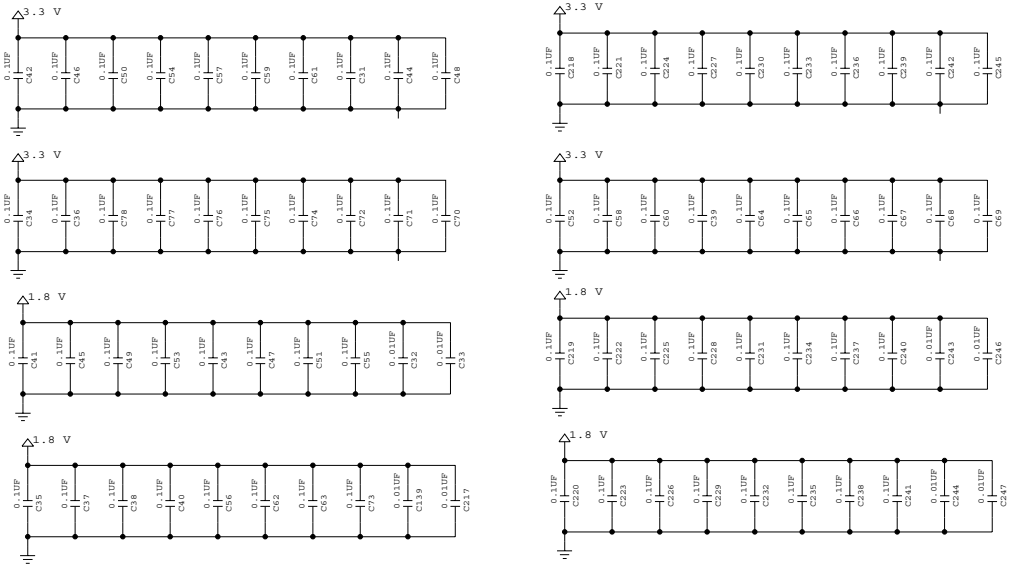
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD TEMUX-84 3 & 4 SBI	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA INC (HS)	PAGE:11 OF 19

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



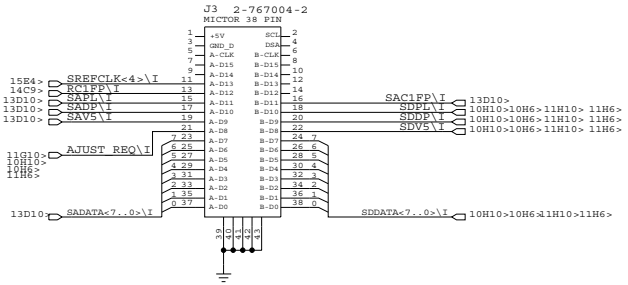
DECOUPLING FOR TEMUX-84 DEVICES.
PLACE ONE CAP FOR EVERY TWO POWER PINS.



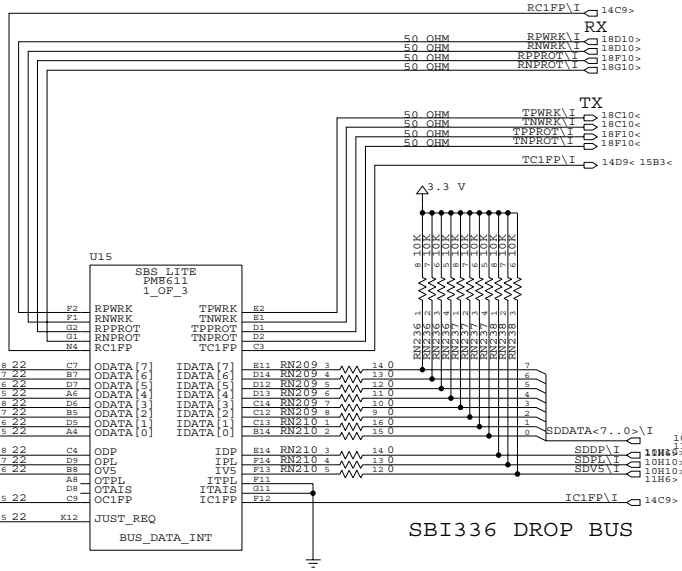
PMC-Sierra, Inc.	
DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 00/12/05
TITLE: OC12 DESIGN POWER	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA INC. (HS)	PAGE:12 OF 19

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

SBI BUS MICTOR CONNECTOR

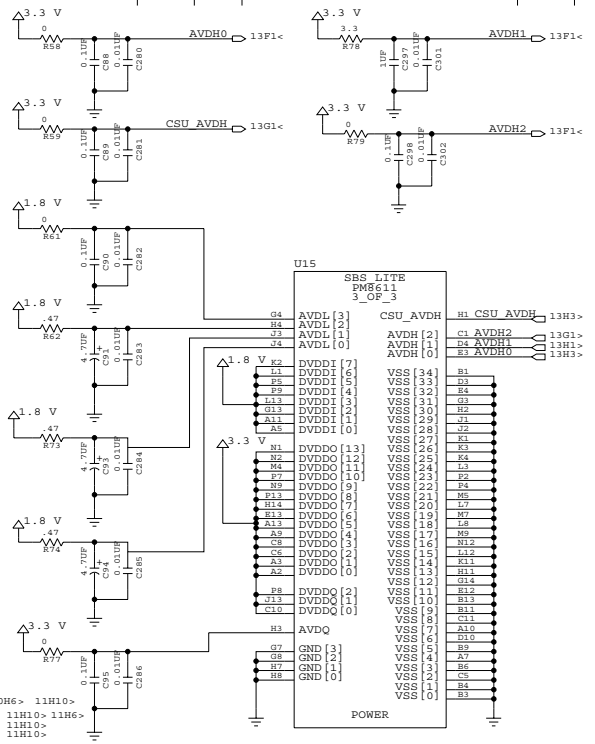


LVDS LINKS

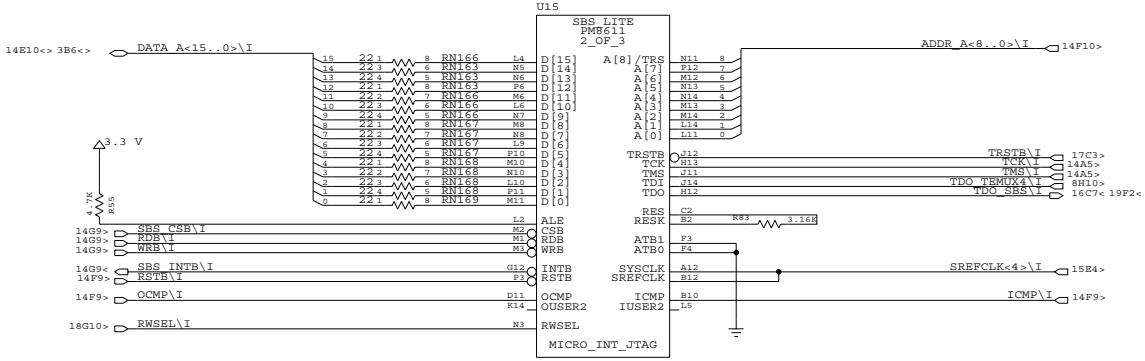


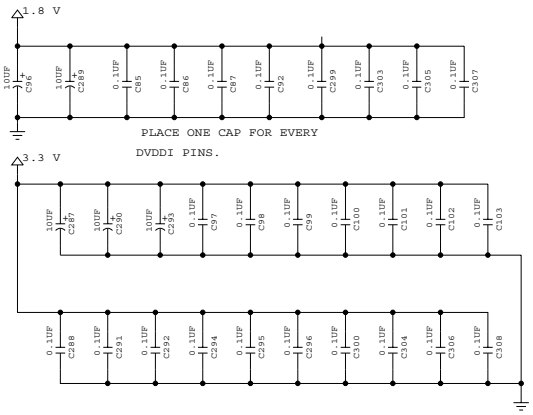
SBI336 ADD BUS

SBI336 DROP BUS



MICROPROCESSOR / JTAG INTERFACE





DRAWING

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TITLE=SBS BLOCK
LAST_MODIFIED=Mon May 28 11:42:52 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD SBS-LITE SECTION	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA INC (HS)	PAGE:13 OF 19

NOTE: (DEPENDS ON POSITION OF CONNECTOR)

LCLK IS CHOSEN FROM EITHER LCKLN\I OR LCLK_P\I
OUTPUT_INTB ROUTES TO EITHER OUTPUT_INTBN\I OR OUTPUT_INTB_P\I
CPLD_CSB IS CHOSEN FROM EITHER CPLD_CSB_P\I OR CSB_0N\I
OUTPUT_INTB SHOULD BE INVERTED BY CPLD BEFORE GOING TO LED

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

XC95288XL CPLD - 288 MICROCELLS 2 OF 2

DECOUPLING FOR XC95288XL.
PLACE ONE CAP FOR EACH VCC PIN.

XC95288XL CPLD 1 OF 2 288 MICROCELLS

CPLD ISP PORT 100MIL J12

JTAG DEBUG PORT 100MIL J13

J15 1441P VERTICAL

J11 1442P VERTICAL

J10 HEADER 8X2

NOTE:
SEE THE REF DESIGN FOR FURTHER DETAILS REGARDING THE CONNECTION OF THE PINS ON THE HEADER

DRAWING

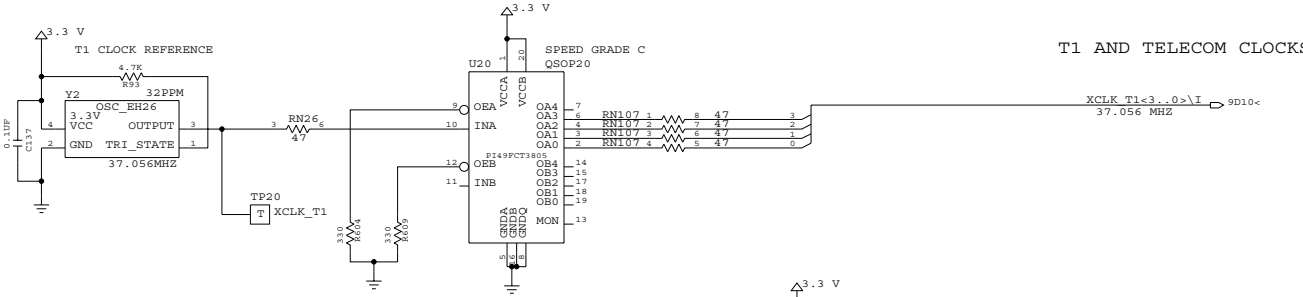
ABBREV=CPLD
TITLE=CPLD
LAST_MODIFIED=Mon May 28 11:42:59 2001

PMC-Sierra, Inc.

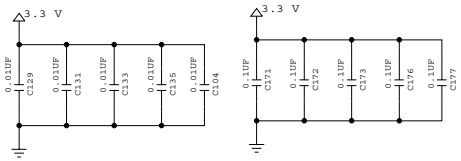
DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD CPLD	REVISION NUMBER: 1
ENGINEER: PMC-SEIRRA (HS)	PAGE:14 OF 19

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

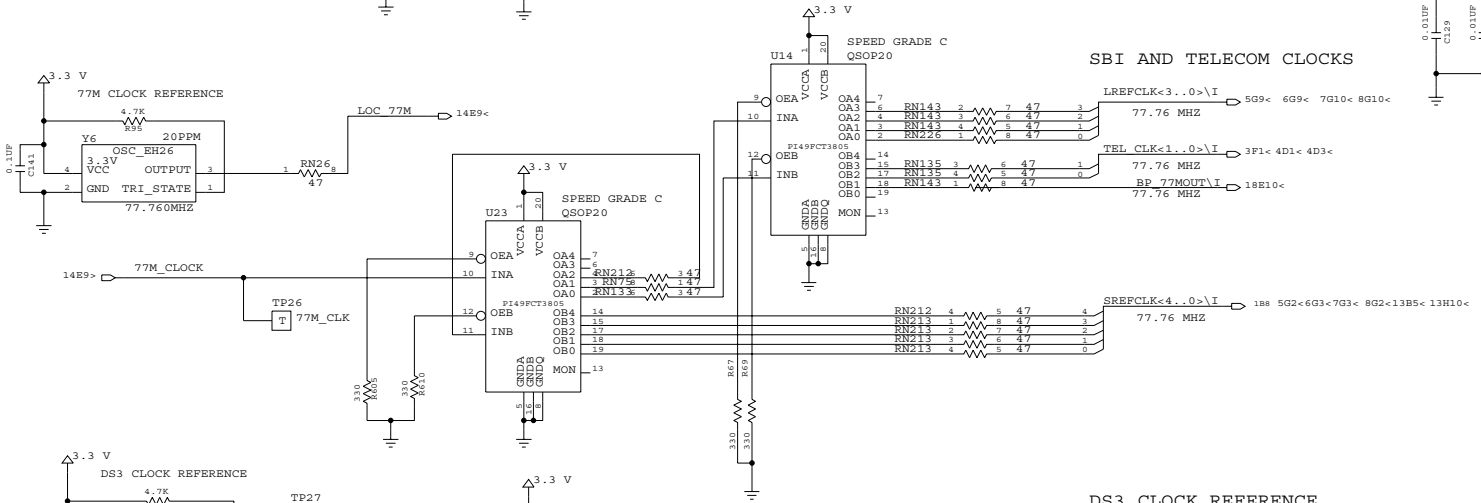
T1 AND TELECOM CLOCKS



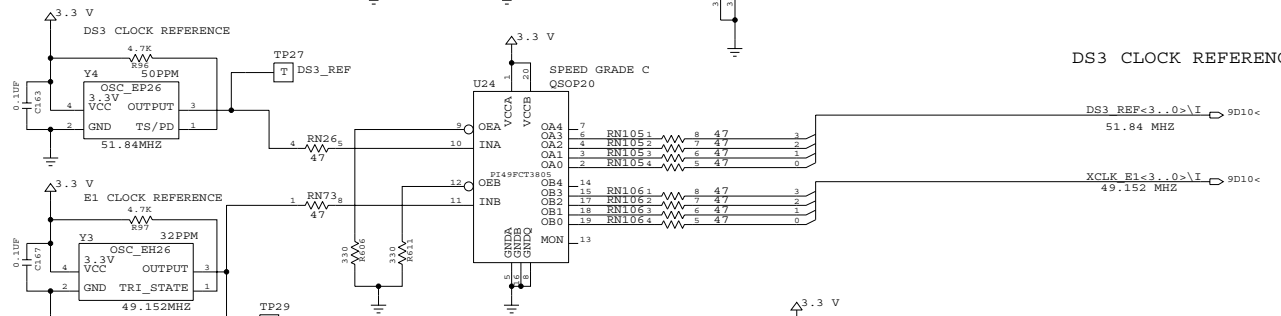
DECOUPLING FOR PI49FCT3805 DEVICES.
PLACE ONE OF EACH TYPE OF CAP PER CHIP.



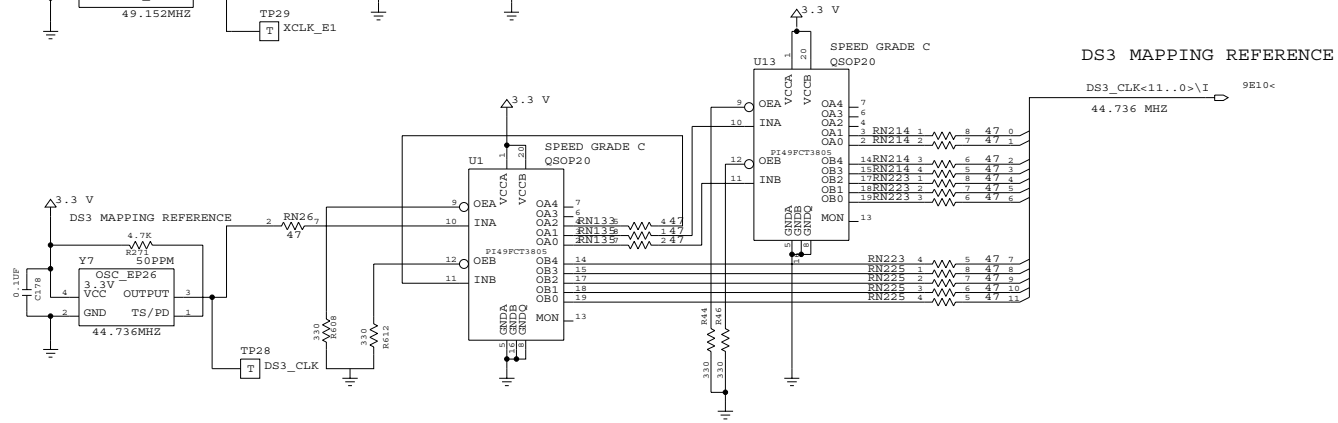
SBI AND TELECOM CLOCKS

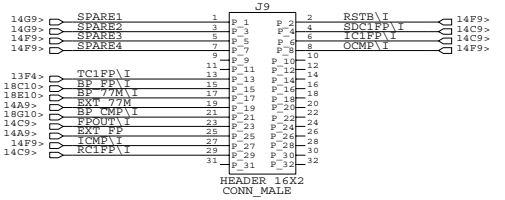


DS3 CLOCK REFERENCE



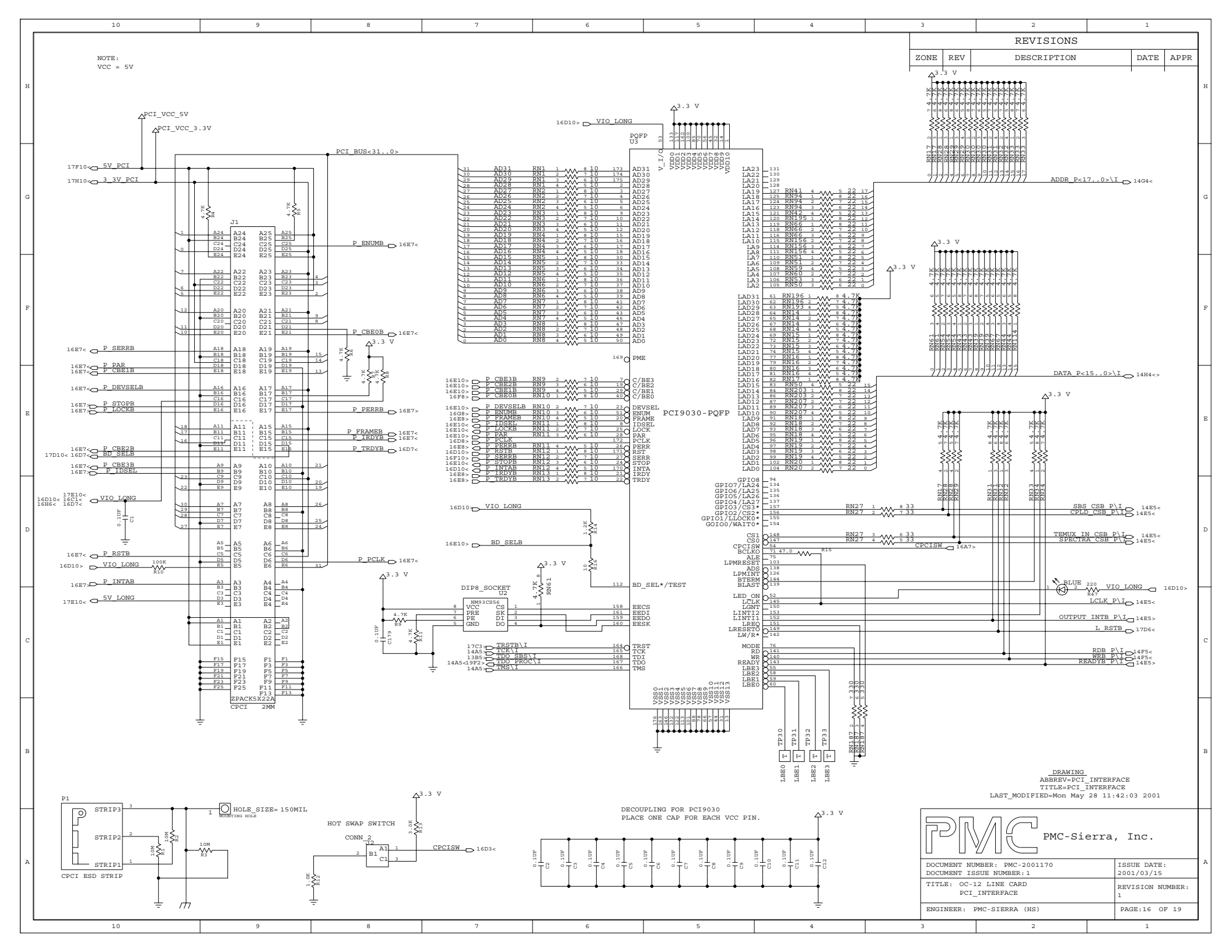
DS3 MAPPING REFERENCE





PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD CLOCK BUFFERS	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA (HS)	PAGE:15 OF 19


REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPR
NOTE:
VCC = 5V
PCI_VCC_5V
PCI_VCC_3.3V
5V_PCI
3_3V_PCI
PCI_BUS<31..0>
J1
ZPACK5X22A
CPCI 2MM
PCI9030-PQFP
PQFP
U3
P_ENUMB
P_CBE0B
P_SERRB
P_PAR
P_CBE1B
P_DEVSELB
P_STOPB
P_LOCKB
P_PERRB
P_FRAMEB
P_IRDYB
P_TRDYB
P_CBE2B
BD_SELB
P_CBE3B
P_IDSEL
P_RSTB
P_PCLK
P_INTAB
5V_LONG
VIO_LONG
3.3 V
ADDR_P<17..0>\I
DATA_P<15..0>\I
SBS_CSB_P\I
CPLD_CSB_P\I
TEMUX_IN_CSB_P\I
SPECTRA_CSB_P\I
LCLK_P\I
OUTPUT_INTB_P\I
L_RSTB
RDB_P\I
WRB_P\I
READYB_P\I
BLUE
DIP8_SOCKET
U2
NM93CS56
TRSTB\I
TCK\I
TDO_SBS\I
TDO_PROC\I
TMS\I
CPCISW
BCLKO
ALE
LPMRESET
ADS
LPMINT
BTERM
BLAST
LED_ON
LCLK
LGNT
LINTI2
LINTI1
LREQ
LRESETO
LW/R*
MODE
RD
WR
READY
LBE3
LBE2
LBE1
LBE0
TP30
TP31
TP32
TP33
P1
STRIP3
STRIP2
STRIP1
HOLE_SIZE= 150MIL
MOUNTING HOLE
CPCI ESD STRIP
HOT SWAP SWITCH
CONN_2
J2
DECOUPLING FOR PCI9030
PLACE ONE CAP FOR EACH VCC PIN.
DRAWING
ABBREV=PCI_INTERFACE
TITLE=PCI_INTERFACE
LAST_MODIFIED=Mon May 28 11:42:03 2001
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-2001170
DOCUMENT ISSUE NUMBER:1
ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD PCI_INTERFACE
REVISION NUMBER: 1
ENGINEER: PMC-SIERRA (HS)
PAGE:16 OF 19

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

NOTE:
VCC = 5V

3.3-1.8 BOARD U5
CONTROL
TPM
NOTE: THIS IS A BOARD
VOUT GND VIN

5.0-3.3 BOARD U7
CONTROL
TPM
NOTE: THIS IS A BOARD
VOUT GND VIN

NOTE:
CONTROL PIN IS HANGING SO VOUT
IS SET TO THE SPECIFIED DEVICE OUTPUT

16G10> 3_3V_PCI
16G10> 5V_PCI
16D10> VIO_LONG
16C10> 5V_LONG
16E10> BD_SELB

IRL3502S Q5
IRL3502S Q4
1N4148W D3
MMBT3904
LTC1422 SOIC
TC74LVX08FN U6
VERT_6MM SW1

RSTB_IN\I 14E5< 17A8<
L_RSTB 16C1>
RSTBN\I 19C5>
TRSTB_IN\I 14E5> 14A5>
TRSTB\I 3A10<5H9< 6H9< 7H10< 8H10< 13B5<16C7<19F2<

POWER SUPPLY TEST POINTS
DISTRIBUTE THROUGOUT THE BOARD

TP51 TP52 TP53 TP1 TP2 TP54 +5V
TP39 TP40 TP41 TP42 TP43 TP44 TP3 TP4 TP5 TP6 TP7 TP8 TP55 +3_3V
TP45 TP46 TP47 TP48 TP49 TP50 TP11 TP12 TP15 TP16 TP19 TP23 TP56 +1_8V
3_3V_PCI TP24 3_3V_PCI
5V_PCI TP25 5V_PCI
TP34 TP35 TP36 TP37 TP57 TP58 TP59 TP60 TP61 TP62 TP63 TP64 GND

POWER / RESET INDICATORS

GREEN D2
SSP-LXH5147
SOT23 MMBT3904
~20MA ->
RSTB_IN\I 17D3>

DRAWING

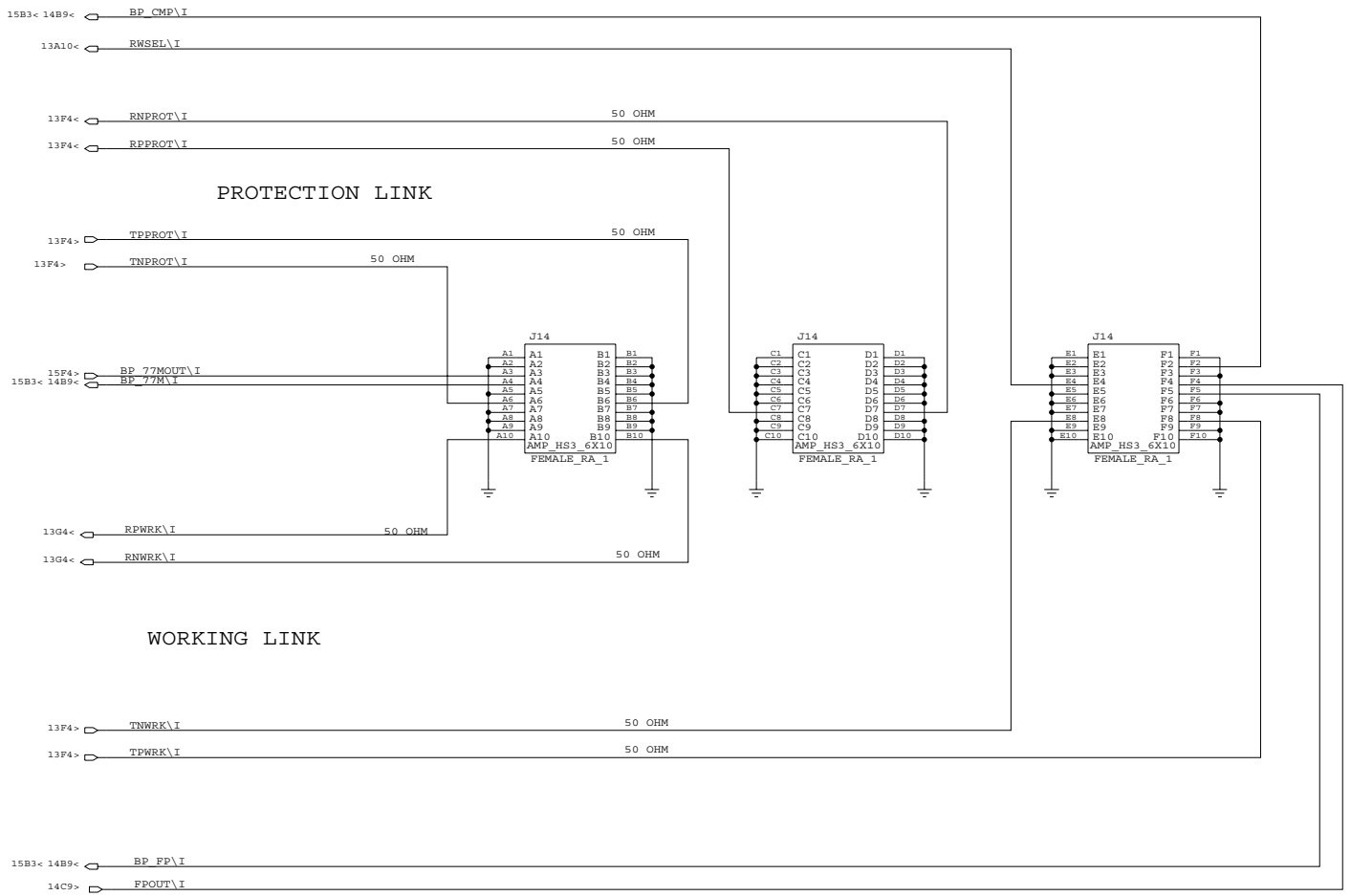
PCI_INTERFACE
PCI_INTERFACE
LAST_MODIFIED=Mon May 28 11:42:08 2001

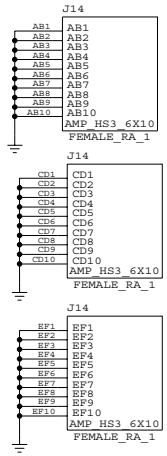
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD POWER SUPPLY / HOT SWAP CONTROL	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA (HS)	PAGE:17 OF 19

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

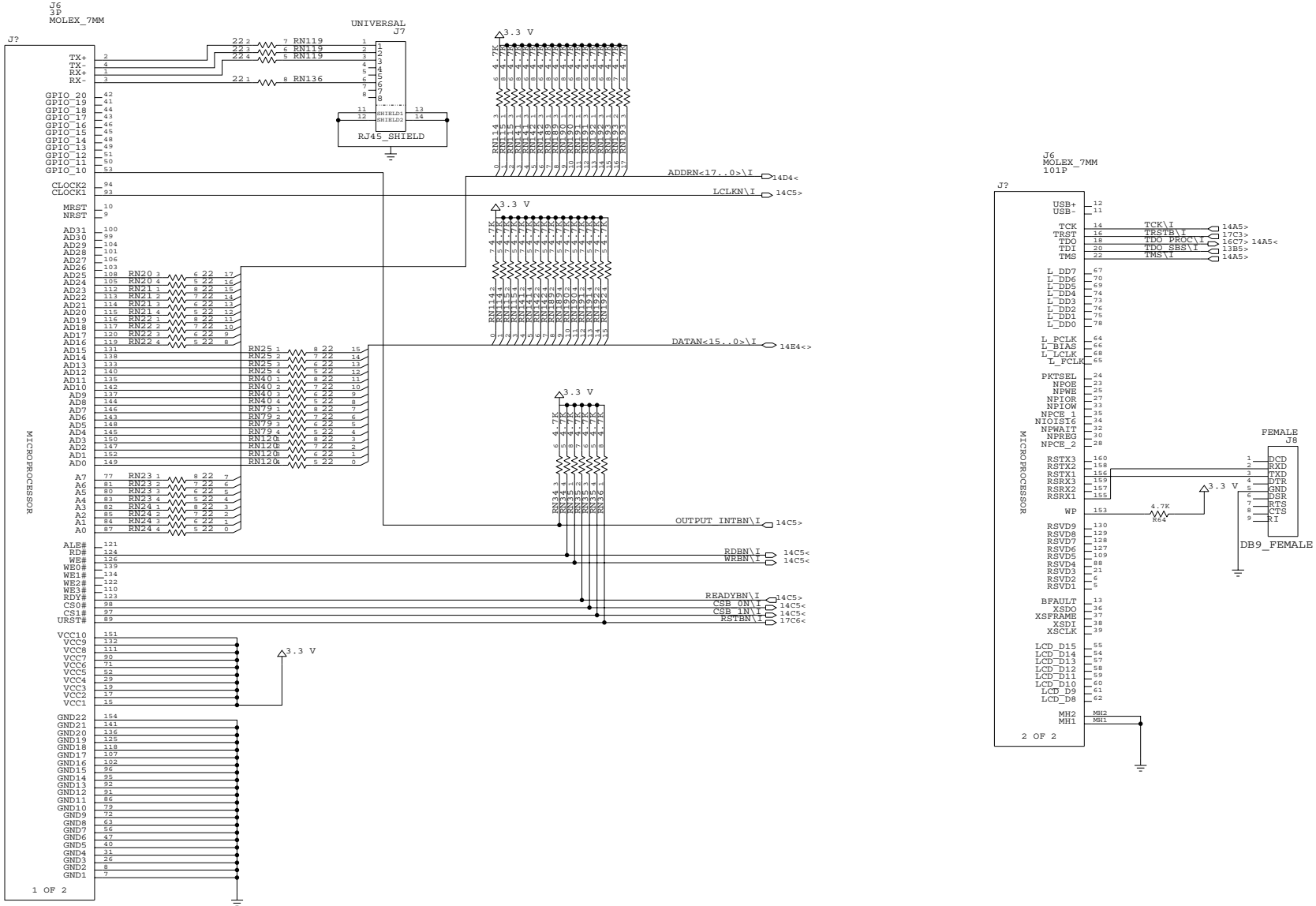
NOTE: ALL LVDS LINES ARE 50 OHMS





PMC-Sierra, Inc.	
DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD LVDS_INTERFACE	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA INC (HS)	PAGE:18 OF 19

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2001170 DOCUMENT ISSUE NUMBER:1	ISSUE DATE: 2001/03/15
TITLE: OC-12 LINE CARD PROCESSOR_INTERFCACE	REVISION NUMBER: 1
ENGINEER: PMC-SIERRA INC (HS)	PAGE:19 OF 19

NOTES

CONTACTING PMC-SIERRA, INC.

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Web Site: http://www.pmc-sierra.com

PMC-2001170 (P1) Issue date: June 2001