MX29L8100T/B

8M-BIT [1M x 8/512K x 16] CMOS SINGLE VOLTAGE 3V ONLY FLASH EEPROM

FEATURES

- Extended single-supply voltage range 2.7V to 3.6V for read and write
- JEDEC-standard EEPROM commands
- Endurance 100,000 cycles
- Fast access time: 120ns
- Optimized block architecture
  - One 16 Kbyte protected block(16K-block)
  - Two 8 Kbyte parameter blocks
  - One 96 Kbyte main block
  - Seven 128 Kbyte main blocks
- Hardware and software data protection
  - Hardware Write Protection pin ($\overline{WP}$)
  - Hardware Lockout bit for 16K-block
  - Software command data protection
- Software EEPROM emulation with parameter blocks
- Status register
  - For detection of program or erase cycle completion
- Auto Erase operation
  - Automatically erases any one of the sectors or the whole chip
  - Erase suspend capability
  - Fast erase time: 50ms typical for chip erase
- Auto Page Program operation
  - Automatically programs and verifies data at specified addresses
  - Internal address and data latches for 128 bytes per page
- Low power dissipation
  - 20mA active current
  - 20uA standby current
  - 1uA deep power-down current
- Hardware Reset pin (RP)
  - Reset internal state machine, and put the device into deep power-down mode
- Built-in 128 Bytes/64 words Page Buffer
  - Work as SRAM for temporary data storage
  - Fast access to temporary data
- Low Vcc write inhibit £1.8V
- Industry standard surface mount packaging
  - 48-Lead TSOP Type I
  - 48-Lead CSP (9mm x 11mm)
  - Ball pitch : 0.75mm/0.8mm/1.0mm

1.0 GENERAL DESCRIPTION

The MX29L8100T/B is a 8 Mbit, 3 V-only Flash memory organized as a either 1 Mbytesx8 or 512K word x16. For flexible erase and program capability, the 8 Mbits of data is divided into 11 sectors of one 16 Kbyte protected block, two 8 Kbyte parameter blocks, one 96 Kbyte main block, and seven 128 Kbyte main blocks. To allow for simple in-system operation, the device can be operated with a single 2.7 V to 3.6 V supply voltage. Since many designs read from the flash memory a large percentage of the time, significant power saving is achieved with the 2.7 V VCC operation. Manufactured with MXIC's advanced nonvolatile memory technology, the device offers access times of 120 ns, and a low 1uA typical deep power-down current.

The MX29L8100T/B command set is compatible with the JEDEC single-power-supply flash standard. Commands are written to the command register using standard microprocessor write timings. MXIC's flash memory augments EPROM functionality with an internal state machine which controls the erase and program circuitry. The device Status Register provides a convenient way to monitor when a program or erase cycle is complete, and the success or failure of that cycle.

Programming the MX29L8100T/B is performed on a page basis; 128 bytes of data are loaded into the device and then programmed simultaneously. The typical Page Program time is 5ms.The device can also be reprogrammed in standard EPROM programmers. Reading data out of the device is similar to reading from an EPROM or other flash.

Erase is accomplished by executing the Erase command sequence. This will invoke the Auto Erase algorithm which is an internal algorithm that automatically times the erase pulse widths and verifies proper cell margin. This device features both chip erase and block erase. Each block can be erased and programmed without affecting other blocks. Using MXIC's advanced design technology, no preprogram is required (internally or externally). As a result, the whole chip can be typically erased and verified in as fast as 50 ms.

A combined feature of Write Protection pin ($\overline{WP}$), Reset pin ($\overline{RP}$), 16K-block lockout bit, and software command sequences provides complete data protection. First, software data protection protects the device from inadvertent program or erase. Two "unlock" write cycles must be presented to the device before the program or erase command can be accepted by the device. For hardware data protection, the $\overline{WP}$ pin and $\overline{RP}$ pin provide protection against unwanted command writes due to invalid system bus condition that may occur during system reset and power-up/down sequence. Finally, with 16K-block lockout bit feature, the device provides complete core security for the kernel code required for system initialization.

The device has 128 Bytes built-in page buffer, which can serve as SRAM. This feature provides a convenient way to store temporary data for fast read and write.

MXIC's Flash technology reliably stores memory contents after 100,000 cycles. The MXIC's cell is designed to optimize the erase and program mechanism. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produce reliable cycling.

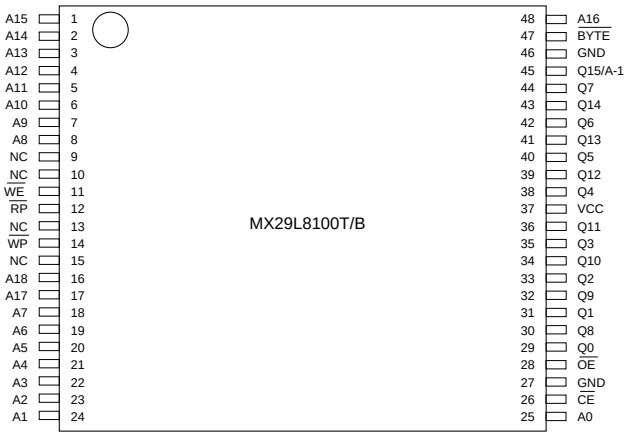
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC +1V.

PIN CONFIGURATIONS

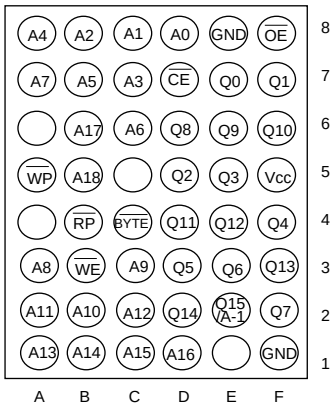
SYMBOL	PIN NAME
A0 - A18	Address Input
Q0 - Q14	Data Input/Output
Q15/A-1	Q15(word mode)/LSB addr(Byte mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable
$\overline{RP}$	Reset/Deep Power-down
$\overline{WP}$	Write Protect
$\overline{BYTE}$	Word/Byte Selection Input
VCC	Power Supply Pin (2.7V - 3.6V)
GND	Ground Pin

1.1 PINOUTS

48-TSOP (TPYE 1) 12 x 20mm



48-CSP(9mm x 11mm, BGA, Ball Pitch : 0.75mm)



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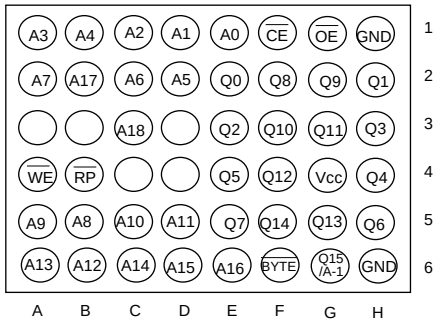
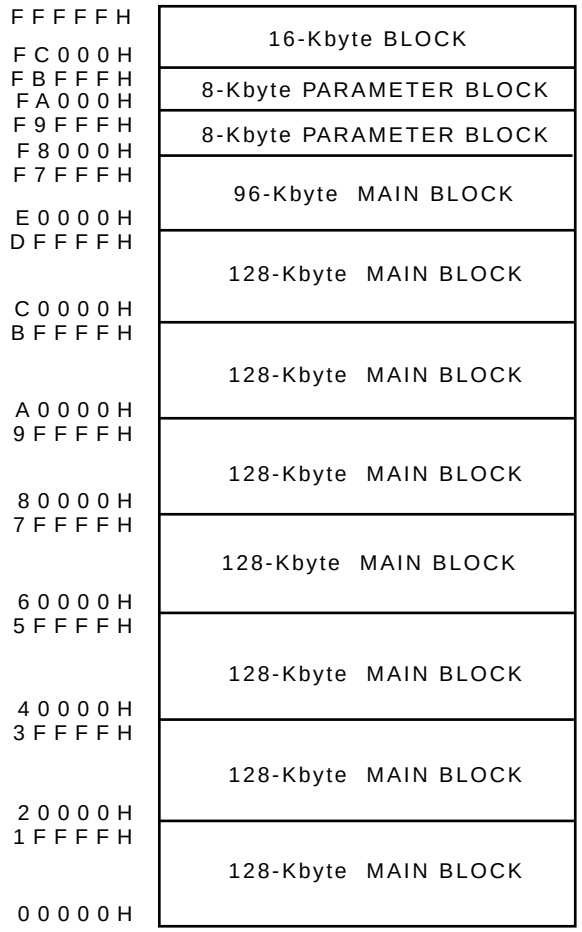
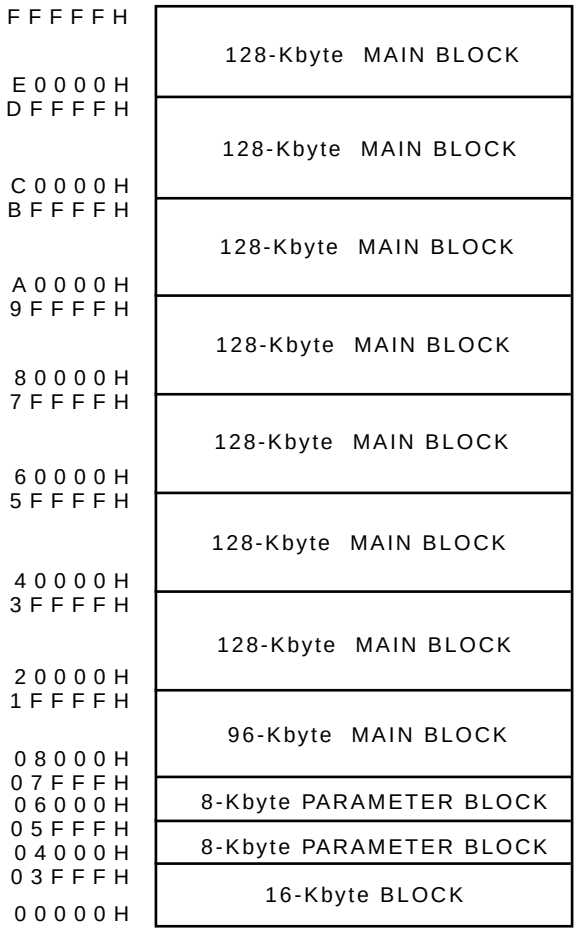


1..2-1 MX29L8100T/B SECTOR ARCHITECTURE (Byte Mode Addr. A-1 ~ A18)

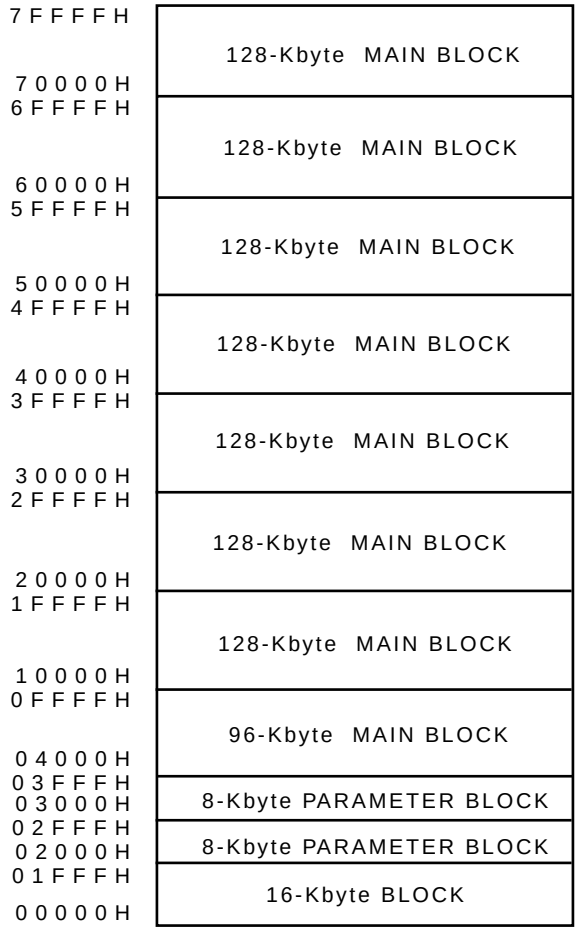


MX29L8100T Memory Map

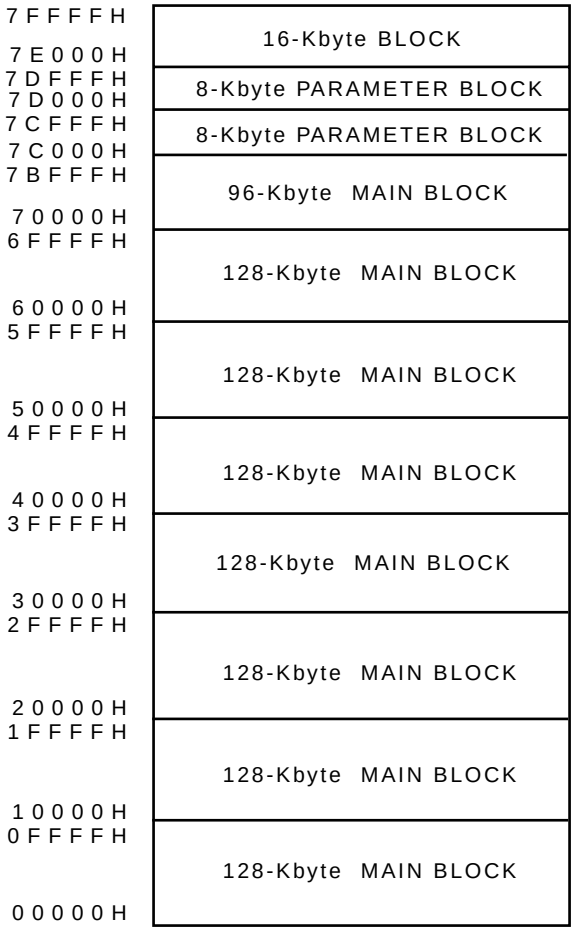


MX29L8100B Memory Map

1..2-2 MX29L8100T/B SECTOR ARCHITECTURE (Word Mode Addr. A0 ~ A18)



MX29L8100T Memory Map



MX29L8100B Memory Map

BLOCK DIAGRAM

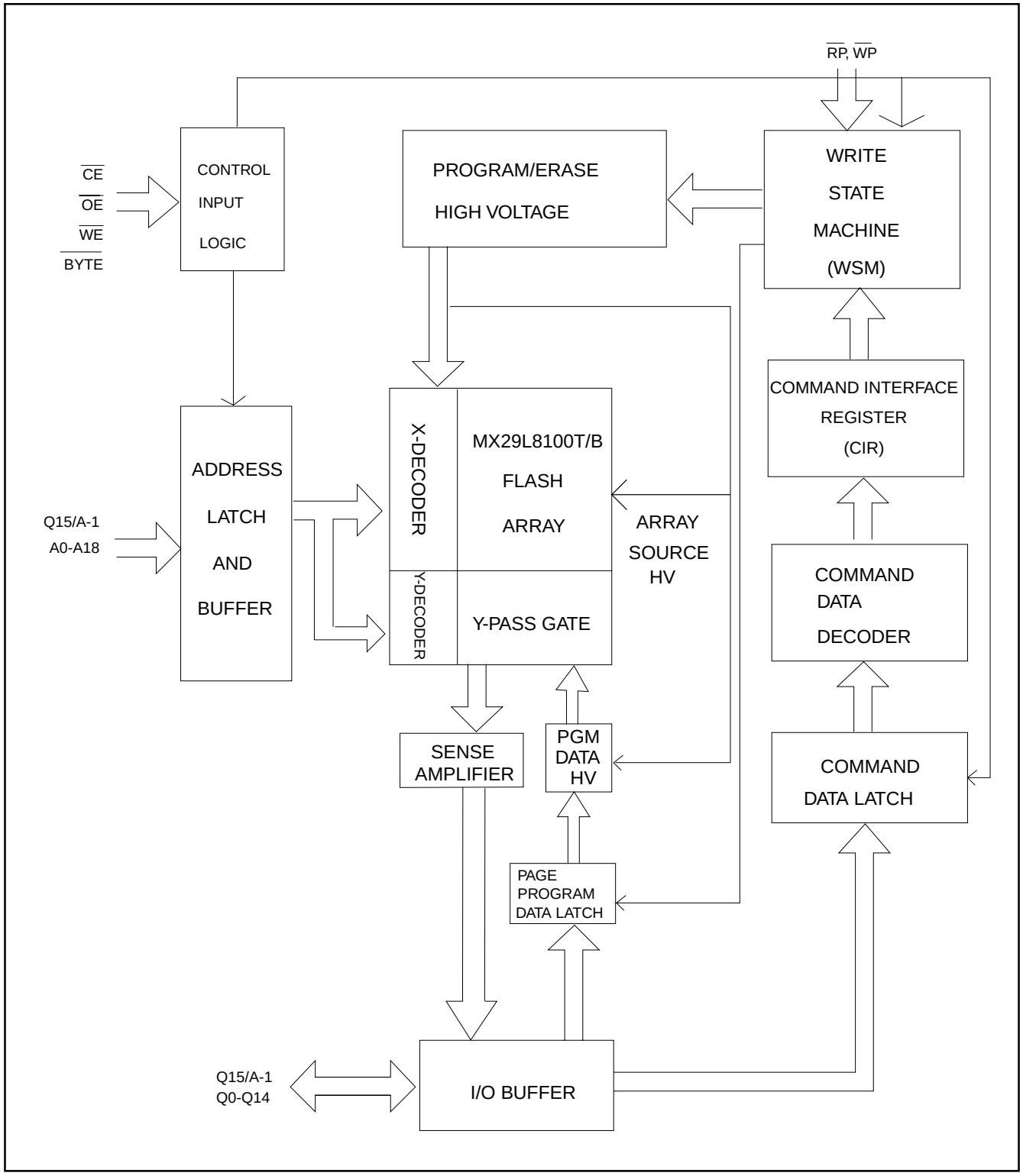


Table 1 .PIN DESCRIPTIONS

SYMBOL	TYPE	NAME AND FUNCTION
A0 - A18	INPUT	ADDRESS INPUTS: for memory addresses. Addresses are internally latched during a write cycle.
Q0 - Q7	INPUT/OUTPUT	LOW-BYTE DATA BUS: Input data and commands during Command Interface Register(CIR) write cycles. Outputs array, status, identifier data, and page buffer in the appropriate read mode. Float to tri-state when the chip is deselected or the outputs are disabled.
Q8-Q14	INPUT/OUTPUT	HIGH-BYTE DATA BUS:Input data during x16 Data-Write operations. Outputs array, identifier data in the appropriate read mode; not used for status register reads. Floated when the chip is de-selected or the outputs are disabled.
Q15/A-1	INPUT/OUTPUT	Selectes between high-byte data INPUT/OUTPUT ($\overline{BYTE}$=HIGH) and LSB ADDRESS ($\overline{BYTE}$=LOW)
$\overline{BYTE}$	INPUT	BYTE ENABLE:$\overline{BYTE}$ Low places device in x8 mode. All data is then input or output on Q0~7 and Q8~14 float. Address Q15/A-1 selectes between the high and low byte. $\overline{BYTE}$ high places the device in x16 mode, and turns off the Q15/A-1 input buffer. Address A0, then becomes the lowest order address.
$\overline{CE}$	INPUT	CHIP ENABLE INPUTS: Activate the device's control logic, input buffers, decoders and sense amplifiers. With $\overline{CE}$ high, the device is deselected and power consumption reduces to Standby level upon completion of any current program or erase operations. $\overline{CE}$ must be low to select the device.
$\overline{OE}$	INPUT	OUTPUT ENABLES: Gates the device's data through the output buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	WRITE ENABLE: Controls writes to the Command Interface Register(CIR). $\overline{WE}$ is active low.
$\overline{RP}$	INPUT	RESET/DEEP POWER-DOWN: When $\overline{RP}$ is low, the device is in reset/deep power-down mode. When $\overline{RP}$ is high, the device is in standard operation.
$\overline{WP}$	INPUT	WRITE PROTECTION: Provides a method for locking the 16K-block, using three voltage levels (VIL, VIH, and VHH). When $\overline{WP}$ is low, the 16K-block is locked. When $\overline{WP}$ is high the 16K-block is unlocked, if the 16K-block lockout bit is disabled. When $\overline{WP}$ is at VHH, the 16K-block is unlocked. This overrides the status of the lockout bit. See Section3 for details of data-protection
VCC		DEVICE POWER SUPPLY(2.7V - 3.6V)
GND		GROUND

1.3 BUS OPERATION

Flash memory reads, erases and writes in-system via the local CPU . All bus cycles to or from the flash memory conform to standard microprocessor bus cycles. These bus operations are summarized below.

Table2-1 MX29L8100T/B Bus Operations for Byte-Wide Mode ($\overline{BYTE}$=VIL)

Mode	Notes	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RP}$	A0	A1	A9	Q0-Q7	Q8-Q14	Q15/A-1
Read		VIL	VIL	VIH	VIH	X	X	X	DOUT	HighZ	VIL/VIH
Output Disable		VIL	VIH	VIH	VIH	X	X	X	High Z	HighZ	X
Standby		VIH	X	X	VIH	X	X	X	High Z	HighZ	
Deep power down		X	X	X	VIL	X	X	X	HighZ	HighZ	X
Manufacturer ID		VIL	VIL	VIH	VIH	VIL	VIL	VHH	C2H	HighZ	VIL
Device ID		VIL	VIL	VIH	VIH	VIH	VIL	VHH	85H(Top Boot) 84H(Bottom Boot)	HighZ	VIL
Write		VIL	VIH	VIL	VIH	X	X	X	DIN	HighZ	VIL/VIH

NOTES :1. X can be VIH or VIL for address or control pins.
2. VHH = 11.5V- 12.5V.
3. Q15/A-1=VIL, Q0~Q7=D0~D7 out, Q15/A-1=VIH, Q0~Q7=D8~D15 out

Table2-2 MX29L8100T/B Bus Operations for Word-Wide Mode ($\overline{BYTE}$=VIH)

Mode	Notes	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RP}$	A0	A1	A9	Q0-Q7	Q8-Q14	Q15/A-1
Read		VIL	VIL	VIH	VIH	X	X	X	DOUT	DOUT	DOUT
Output Disable		VIL	VIH	VIH	VIH	X	X	X	High Z	HighZ	HighZ
Standby		VIH	X	X	VIH	X	X	X	High Z	HighZ	HighZ
Deep power down		X	X	X	VIL	X	X	X	HighZ	HighZ	HighZ
Manufacturer ID		VIL	VIL	VIH	VIH	VIL	VIL	VHH	C2H	00H	0B
Device ID		VIL	VIL	VIH	VIH	VIH	VIL	VHH	85H(Top Boot) 84H(Bottom Boot)	00H	0B
Write		VIL	VIH	VIL	VIH	X	X	X	DIN	DIN	DIN

NOTES :1.X can be VIH or VIL for address or control pins.
2. VHH = 11.5V- 12.5V.

1.4 WRITE OPERATIONS

The Command Interface Register (CIR) is the interface between the microprocessor and the internal chip controller. Device operations are selected by writing specific address and data sequence into the CIR, using standard microprocessor write timings. Writing incorrect data value or writing them in improper sequence will reset the device to the read mode.(read array or read buffer) Table 3 defines the valid command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) are valid only while an erase operation is in progress and will be ignored in other circumstance. There are four read modes: Read Array, Read Silicon ID, Read Status Register, and Read Page Buffer. For Program and Erase inform the internal state machine that a program or erase sequence has been requested. During the execution of program or erase operation, the state machine will control the program /erase sequence. After the state machine has completed its task, it will set bit 7 of the Status Register (SR. 7) to a "1", which indicates that the CIR can respond to the full command set.

TABLE 3. COMMAND DEFINITIONS

Command Sequence		Read/ Reset	Silicon ID Read	Page/Byte Program	Chip Erase	Block Erase	Erase Suspend	Erase Resume	Sleep Mode
Bus Write Cycles Required		1	4	4	6	6	1	1	3
First Bus Write Cycle	Addr	XXXXH	5555H	5555H	5555H	5555H	XXXXH	XXXXH	5555H
	Data	F0H	AAH	AAH	AAH	AAH	B0H	30H	AAH
Second Bus Write Cycle	Addr	RA	2AAAH	2AAAH	2AAAH	2AAAH			2AAAH
	Data	RD	55H	55H	55H	55H			55H
Third Bus Write Cycle	Addr		5555H	5555H	5555H	5555H			5555H
	Data		90H	A0H	80H	80H			C0H
Fourth Bus Read/Write Cycle	Addr		00H/01H	PA	5555H	5555H			
	Data		C2H/84H C2H/85H	PD	AAH	AAH			
Fifth Bus Write Cycle	Addr				2AAAH	2AAAH			
	Data				55H	55H			
Sixth Bus Write Cycle	Addr				5555H	SA			
	Data				10H	30H			

COMMAND DEFINITIONS(continue Table 3.)

Command Sequence		Lock 16K-block	Lock Status Read	Read Page Buffer	Write Page Buffer	Read Status Register	Clear Status Register	Clear Buffer
Bus Write Cycles Required		6	4	4	4	3	3	3
First Bus	Addr	5555H	5555H	5555H	5555H	5555H	5555H	5555H
Write Cycle	Data	AAH	AAH	AAH	AAH	AAH	AAH	AAH
Second Bus	Addr	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH
Write Cycle	Data	55H	55H	55H	55H	55H	55H	55H
Third Bus	Addr	5555H	5555H	5555H	5555H	5555H	5555H	5555H
Write Cycle	Data	60H	90H	75H	E0H	70H	50H	04H
Fourth Bus	Addr	5555H	SA02H	PA	PA			
Read/Write Cycle	Data	AAH	C2H/00H	PD	PD			
Fifth Bus	Addr	2AAAH						
Write Cycle	Data	55H						
Sixth Bus	Addr	SA						
Write Cycle	Data	20H						

Notes:

1.Address bit A15 -- A18 = X = Don't care for all address commands except for Program Address(PA) and Sector Address(SA).
5555H and 2AAAH address command codes stand for Hex number starting from A0 to A14.

2. Bus operations are defined in Table 2.

3. RA = Address of the memory location to be read.
PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
SA = Address of the block to be erased. The combination of A12 -- A18 will uniquely select any block.

4. RD = Data read from location RA during a read operation.
PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.

5. Erase can be suspended during sector erase with Addr = don't care, Data = B0H

6. Erase can be resumed after suspend with Addr = don't care, Data = 30H.

7. Clear Buffer set all buffer data to 1.

8. Only Q0~Q7 command data is taken, Q8~Q15=Don't care

9. In Lock Status Read, SA02H = 00002H for BOTTOM BOOT(Word/Byte Modes)
SA02H = FFF02H for TOP BOOT(Byte mode)
SA02H = 7FF02H for TOP BOOT(Word Mode)

2.0 DEVICE OPERATION

2.1 SILICON ID READ

The Silicon ID Read mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force VHH (11.5V~12.5V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from VIL to VIH. All addresses are don't cares except A0 and A1.

The manufacturer and device codes may also be read via the command register, for instances when the MX29L8100T/B is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 3.

Following the command write, a read cycle with A0 = VIL retrieves the manufacturer code of C2H. A read cycle with A0 = VIH returns the device code . MX29L8100T Device Code =85H, MX29L8100B Device Code = 84H

To terminate the operation, it is necessary to write the Read/Reset command sequence into the CIR.

Table 4. MX29L8100T/B Silion ID Codes and Verify Sector Protect Code

Type	A_{18}~A_2	A_1	A_0	Code(HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	X	VIL	VIL	C2H	1	1	0	0	0	0	1	0
MX29L8100T Device Code	X	VIL	VIH	85H	1	0	0	0	0	1	0	1
MX29L8100B Device Code	X	VIL	VIH	84H	1	0	0	0	0	1	0	0
Verify 16K-Block Protect**	SA	VIH	VIL	C2H*	1	1	0	0	0	0	1	0

* Outputs C2H if 16K-block is protected (lockout bit is enabled), 00H otherwise.
** Only the 16K-Block has protect-bit feature.

MX29L8100B Manufacter Code=C2H, Device Code=84H when $\overline{BYTE}$=VIL.
MX29L8100T Manufacter Code=C2H, Device Code=85H when $\overline{BYTE}$=VIL.
MX29L8100B Manufacter Code=00C2H, Device Code=0084H when $\overline{BYTE}$=VIH.
MX29L8100T Manufacter Code=00C2H, Device Code=0085H when $\overline{BYTE}$=VIH.

2.2 READ/RESET COMMAND

The read or reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains ready for reads until the CIR contents are altered by a valid command sequence.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

The MX29L8100T/B is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

Note that the Read/Reset command is not valid when program or erase is in progress.

2.3 PAGE PROGRAM

To initiate Page program mode, a three-cycle command sequence is required. There are two " unlock" write cycles. These are followed by writing the page program command A0H. Any attempt to write to the device without the three-cycle command sequence will not start the internal Write State Machine(WSM), no data will be written to the device.

After three-cycle command sequence is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Maximum of 128 bytes of data may be loaded into each page.

2.3.1 BYTE-WIDE LOAD/WORD-WIDE LOAD

Byte(word) loads are used to enter the 128 bytes (64 words) of a page to be programmed or the software codes for data protection. A byte load (word load) is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

Either byte-wide load or word-wide load is determinded ($\overline{BYTE}$=VIL or VIH is latched) on the falling edge of the $\overline{WE}$ (or $\overline{CE}$) during the 3rd command write cycle.

2.3.2 PROGRAM

Any page to be programmed should have the page in the erased state first, i.e. performing sector erase is suggested before page programming can be performed.

The device is programmed on a page basis. If a byte of data within a page is to be changed, data for the entire page can be loaded into the device. Any byte that is not loaded during the programming of its page will be still in the erased state (i.e. FFH). Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 30us of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. A6 to A18 specify the page address, i.e., the device is page-aligned on 128 bytes boundary. The page address must be valid during each high to low transition of $\overline{WE}$ or $\overline{CE}$. A-1 to A5 specify the byte address within the page The byte may be loaded in any order; sequential loading is not required. If a high to low transition of $\overline{CE}$ or $\overline{WE}$ is not detected whithin 100us of the last low to high transition, the load period will end and the internal programming period will start. The load period will also end if the same address is consecutively loaded twice. The first data and address will be treated as normal data to be progammed. The second data needs to be "00" to terminate the load cycle. Other numbers besides "00" are reserved for future use.

The status of program can be determined by checking the Status Register. While the program operation is in progress, bit 7 of the Status Register (SR. 7) is "0". When the Status Register indicates that program is complete (when SR. 7 = 1), the Program Status bit should bechecked to verify that the program operation was successful. If the program operation was unsuccessful, SR. 4 of the Status Register will be set to "1" to indicate a program failure. The Status Register should be cleared before attempting the next operation.

2.4 CHIP ERASE

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command-80H. Two more "unlock" write cycles are then followed by the Chip Erase command 10H. Chip erase does not require the user to program the device prior to erase. The 16K-Block will not be erased if it is protected (16K-Block Lockout bit enabled).

The Auto Chip Erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the status on SR.7 is "1". While the erase sequence is in progress, SR.7 of the Status Register is "0". When erase is complete, the Erase Status bit should be checked. If the erase operation was unsuccessful, SR.5 of the Status Register is set to a "1" to indicate an erase failure. Clear the Status Register before attempting the next operation.

2.5 BLOCK ERASE

Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command-30H. The sector address is latched on the falling edge of $\overline{WE}$, while the command (data) is latched on the rising edge of $\overline{WE}$. Only one sector can be erased at a time.

Sector erase does not require the user to program the device prior to erase. The system is not required to provide any controls or timings during these operations.

The AutomaticBlock Erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on SR.7 is "1". When erasing a block, the remaining unselected blocks are unaffected.During the execution of the Block Erase command, only the Erase Suspend and Erase Resume commands are allowed. The Erase Suspend/Resume command may be issued as many time as required. Similar to the Chip Erase mode, the Status Register should be checked when erase is complete.

2.6 ERASE SUSPEND AND RESUME

The Erase Suspend command is provided to allow the user to interrupt an erase sequence and then read data from a block other than that which is being erased. This command is applicable only during the erase operation. During the erase operation, writing the Erase Suspend command to the CIR will cause the internal state machine to pause the erase sequence at a predetermined point. The Status Register will indicate when the erase operation has been suspended.

Once in erase suspend, a Read Array command can be written to the CIR in order to read data from blocks not being erase suspended. The only other valid commands during erase suspend are Erase Resume and Read Status Register commands. Read Page Buffer command, however, is not applicable during erase suspend.

To resume the erase operation, the Erase Resume command 30H should be written to the CIR. Another Erase Suspend command can be written after the chip has resumed erasing.

Table5. Status Register Bit Definition

WSMS	ESS	ES	PS	SLP	SLK
7	6	5	4	2	1

SR.7 = WRITE STATE MACHINE STATUS(WSMS)
1 = Ready
0 = Busy

SR.6 = ERASE-SUSPEND STATUS (ESS)
1 = Erase Suspended
0 = Erase in Progress/Completed

SR.5 = ERASE STATUS
1 = Error in Erase
0 = Successful Erasure

SR.4 = PROGRAM STATUS
1 = Error in Page/Byte Program
0 = Successful Page/Byte Program

SR.2 = SLEEP STATUS
1 = Device in sleep mode
0 = Device not in sleep mode

SR.3 = 0

SR.1 = Boot sector lock status 1: lock, 0: unlock

Others = Reserved for future enhancements

NOTE :
State machine bit must first be checked to determine Program or Erase completion, before the Program or Erase Status bits are checked for success.

When Erase Suspend is issued, state machine halts execution and sets both WSMS and ESS bits to "1," ESS bit remains set to "1" until an Erase Resume command is issued.

When this bit set to "1," state machine has applied the maximum number of erase pulses to the device and is still unable to successfully verify erasure.

When this bit is set to "1," state machine has attempted but failed to program page data.

When this bit is set to "1", the device is in sleep mode(deep power-down). Writing the Read Array command will wake up the device, and the device will return to standby.

2.7 STATUS REGISTER

The device contains a Status Register which may be read to determine when a Program or Erase operation is complete, and whether that operation completed successfully. The Status Register may be read at any time by writing the Read Status command to the command interface. After writing this command, all subsequent Read operations output data from the Status Register until another command is written to the command interface. A Read Array command must be written to the command interface to return to the read array mode. The Status Register bits are output on DQ[0:7].

In the word-wide(x16) mode the upper byte, DQ(8:15) is set to 00H during a Read status command, in the byte-wide mode, DQ(8:14) are tri-stated and DQ15/A-1 retains the low order address function.

The contents of the Status Register are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs last in the read cycle. This prevents possible bus errors which might occur if the contents of the Status Register change while reading the Status Register. $\overline{CE}$ or $\overline{OE}$ must be toggled with each subsequent status read, or the completion of a Program or Erase operation will not be evident from the Status Register.

When the state machine is active, this register will indicate the status of the state machine, and will also hold the bits indicating whether or not the state machine was successful in performing the desired operation.

2.7.1 CLEARING THE STATUS REGISTER

The state machine sets status bits 4 through 7 to "1", and clears bits 6 and 7 to "0", but cannot clear status bits 4 and 5 to "0". Bits 4 and 5 can only be cleared by the controlling CPU through the use of the Clear Status Register command. These bits can indicate various error conditions. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several bytes or erasing multiple blocks in sequence). The Status Register may then be read to determine if an error occurred during that programming or erasure series. This adds flexibility to the way the device may be programmed or erased. Once an error occurred, the command Interface only responds to clear Status Register, Read Status Register and Read Array. To clear the Status Register, the Clear Status Register command is written to the command interface. Then, any other command may be issued to the command interface. Note, again, that before read cycle can be initiated, a Read Array command must be written to the command interface to specify whether the read data is to come from the Memory Array, Status Register, Page Buffer, or silicon ID.

2.8 SLEEP MODE

The MX29L8100T/B features a sofware controlled low power modes: Sleep modes. Sleep mode is allowed during any current operations except that once Suspend command is issued, Sleep command is ignored. To activate Sleep mode, a three-bus cycle operation is required. The C0H command (Refer to Table 3) puts the device in the Sleep mode. Once in the Sleep mode and with CMOS input level applied, the power of the device is reduced to deep power-down current levels. The only power consumed is diffusion leakage, transistor subthreshold conduction, input leakage, and output leakage.

The Sleep command allows the device to complete its current operations before going into Sleep mode. During Sleep mode, Silicon ID codes remain valid and can still be read. The Device Sleep Status bit SR.2 will indicate that the device in the sleep mode. The device is in read SR. mode during sleep mode.

Writing the Read Array command wakes up the device out of sleep mode. SR.2 is reset to "0" and device returns to standby current level.

2.9 PAGE BUFFER READ AND WRITE

The MX29L8100T/B has 128 Bytes of page buffers, which can work as SRAM to store temporary data for fast access purpose. To write data into page buffers, the Write Page Buffer command is written to the CIR. There are two "unlock"write cycles, followed by the command E0H. Loading data to page buffer is similar to that in Page Program. Sequential loading is not required. (A-1 to A5 in byte mode, or A0 to A5 in word mode) must be valid to specify byte address within the page buffers during each high-to-low transition of $\overline{WE}$ or $\overline{CE}$. Each new byte to be stored must have its high-to-low transition of $\overline{WE}$ or $\overline{CE}$ within 30 us of the low-to-high transition of $\overline{WE}$ or $\overline{CE}$ of the preceding byte. Otherwise, the Write Page Buffer mode is terminated automatically.

To read data from the page buffer, the Read Page Buffer command is written to the CIR. There are two "unlock" write cycles, which are followed by the command 75H. Each subsequent toggle of address (or $\overline{OE}$, $\overline{CE}$) will read data from the specified byte address of the page buffer (A-1 to A5 in byte mode or A0 to A5 in word mode). To terminate the operation, it is necessary to write the Read/Reset command sequence into the CIR.

2.9.1 BYTE-WIDE LOAD/WORD-WIDE LOAD

Byte(word) loads are used to enter the 128 bytes (64 words) of a page to be programmed or the software codes for data protection. A byte load (word load) is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$.

Either byte-wide load or word-wide load is determinded ($\overline{BYTE}$=VIL or VIH is latched) on the falling edge of the $\overline{WE}$ (or $\overline{CE}$) during the 3rd command write cycle.

3.0 DATA PROTECTION

The MX29L8100T/B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read Array mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transitions or system noise.

3.1 16K-BLOCK LOCKING

The MX29L8100T/B features hardware 16K-Block protection. This feature will disable both program and erase operations in the 16K-Block. The block protection feature is enabled using system software by the user (Refer to Table 3). The device is shipped with 16K-Block unprotected. Alternatively, MXIC may protect 16K-Block in the factory prior to shipping the device.

3.1.1 LOCK BLOCK

To active this mode, a six-bus cycle operation is required. There are two "unlock" write cycles. These are followed by writting the "set-up" command. Two more "unlock" write cycles are then followed the Lock Sector command 20H. The automatic Lock operation begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the status on SR.7 is "1" at which time the device stays at the read mode.

3.1.2 LOCK STATUS READ

To verify the Protect status of the 16K-Block, operation is initiated by writing Silicon ID read command into the command register. Following the command write, a read cycle from addressSA02H(See Table3) retrieves the Manufacturer code of (C2H in byte mode, 00C2H in word mode) if the 16K-Block is protected. If the 16K-Block is unprotected, (00H in byte mode, 0000H in word mode) will be read instead. To terminate the operation, it is necessary to write the Read/Reset command sequence into the CIR.

The lock status information can also be retrieved by reading SR. . The SR.1 ="1" if 16K-Block is locked. The SR.1 ="0" if 16K-Block is unlocked.

A few retries are required if Protect status can not be verified successfully after each operation.

Execute lock bit protection operation three additional times after protect bit is verified successfully to guarantee lock bit status under all conditions.

3.2 HARDWARE PROTECTION

Protection for parameter blocks and main blocks can be achieved using combinations of $\overline{RP}$ and $\overline{WP}$ pins.

3.2.1 $\overline{RP}$ = VIL FOR COMPLETE PROTECTION

For complete data protection of all blocks, the $\overline{RP}$ can be held low.

3.2.2 $\overline{WP}$ = VIL FOR 16K-BLOCK LOCKING

When $\overline{WP}$ = VIL, the 16K-block is locked, while all other blocks remain unlocked in this condition and can be programmed or erased normally.

3.2.3 $\overline{WP}$ = VHH FOR 16K-BLOCK UNLOCKING

If $\overline{WP}$ = VHH, the 16K-Block is unlocked and can be programmed or erased. Note that this feature will override the 16K-Block Lock bit protection.

3.2.4 $\overline{WP}$ = VIH FOR REGULAR BLOCK UNLOCKING

If $\overline{WP}$ = VIH and $\overline{RP}$ = VIH, all the regular blocks (parameter blocks and main blocks) are unlocked and can be programmed or erased. In this condition, whether the 16K-Block is locked is dependent on the 16K-Block Lock bit. If the 16K-Block Lock bit is enabled, then the 16K-Block is still protected; otherwise, it is unlocked. The following truth table clearly defines the write protection methods.

Table 5. WRITE PROTECTION TRUTH TABLE FOR MX29L8100T/B

$\overline{RP}$	$\overline{WP}$	16K-Block	Write Protection Provided	
		Lockout bit	16K-Block	Regular Block
VIH	VHH	X	unlocked	unlocked
VIL	X	X	locked	locked
VIH	VIL	X	locked	unlocked
VIH	VIH	1	locked	unlocked
VIH	VIH	0	unlocked	unlocked

3.3 LOW VCC WRITE INHIBIT

To avoid initiation of a write cycle during VCC power-up and power-down, a write cycle is locked out for VCC less than VLKO(typically 1.8V). If VCC < VLKO, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the VCC level is greater than VLKO. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional write when VCC is above VLKO.

3.4 WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns (typical) on $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

3.5 LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE}$ = VIL,$\overline{CE}$ = VIH or $\overline{WE}$ = VIH. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Figure 1. AUTO PAGE PROGRAM FLOW CHART

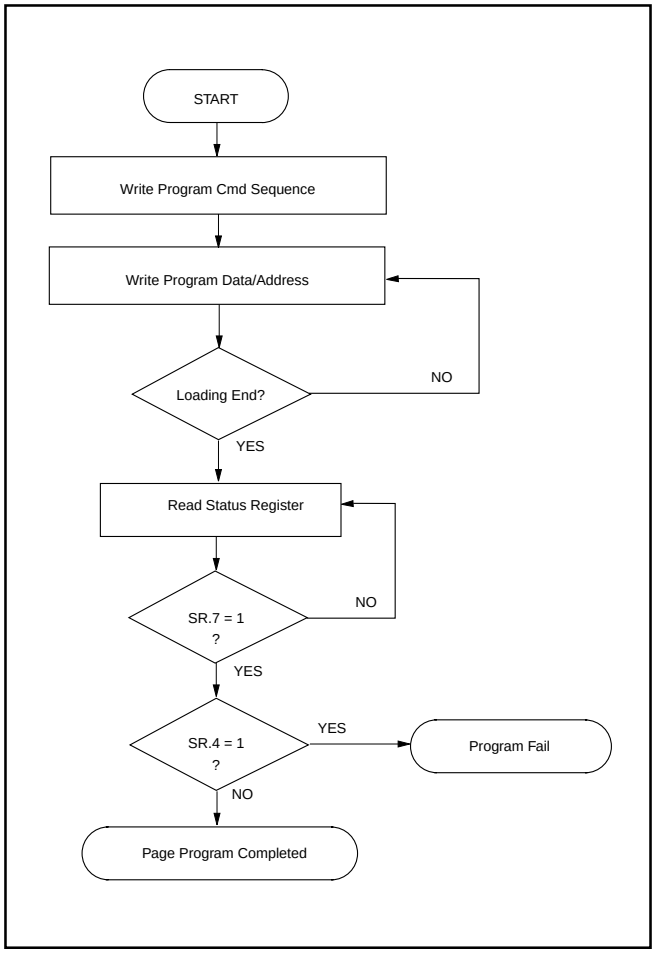


Figure 2. AUTO ERASE FLOW CHART

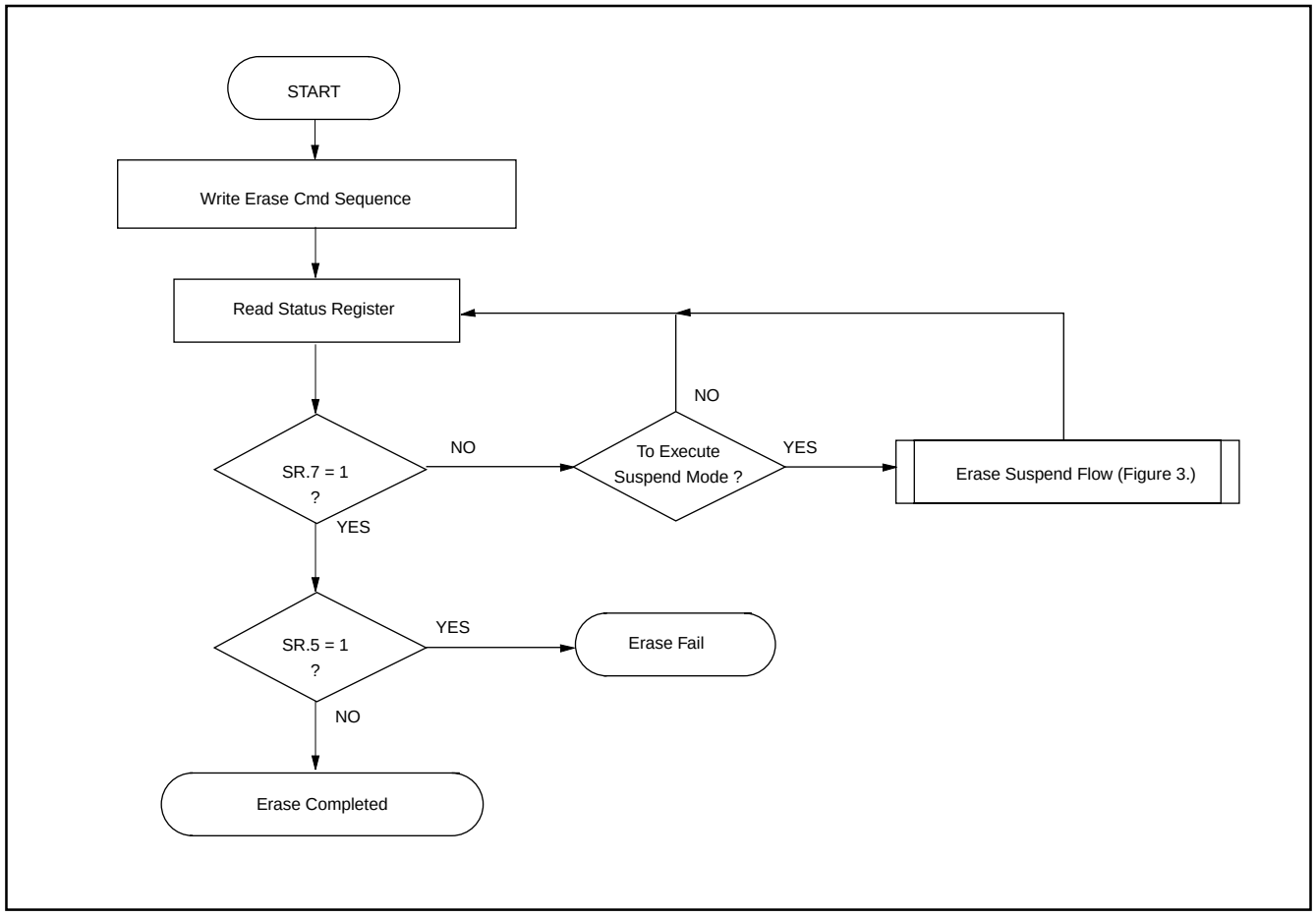


Figure 3. ERASE SUSPEND/ERASE RESUME FLOW CHART

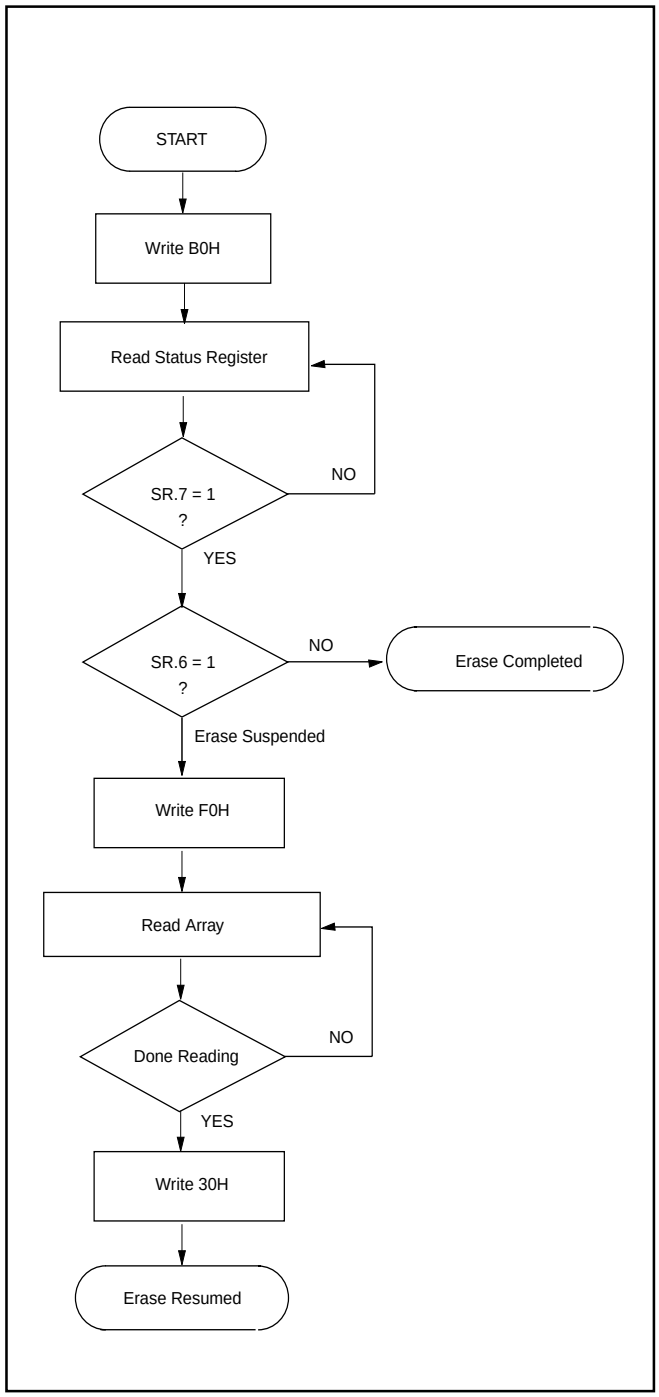


Figure 4. 16K-BLOCK PROTECTION FLOW CHART

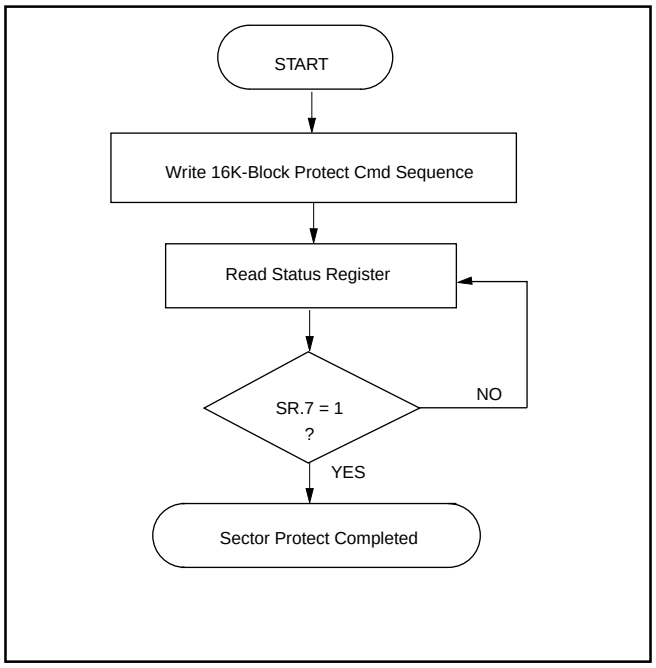
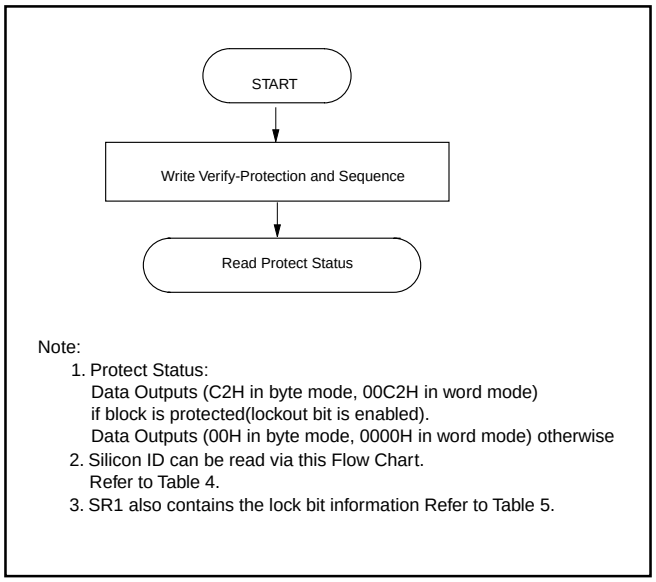


Figure 5. VERIFY 16K-BLOCK PROTECT FLOW CHART



Note:
1. Protect Status:
   Data Outputs (C2H in byte mode, 00C2H in word mode)
   if block is protected(lockout bit is enabled).
   Data Outputs (00H in byte mode, 0000H in word mode) otherwise
2. Silicon ID can be read via this Flow Chart.
   Refer to Table 4.
3. SR1 also contains the lock bit information Refer to Table 5.

5.0 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Temperature	-40℃ to 85℃
Storage Temperature	-65℃ to 125℃
Applied Input Voltage	-0.5V to VCC + 4.5
Applied Output Voltage	-0.5V to VCC + 0.6
VCC to Ground Potential	-0.5V to 5.5V
A9, $\overline{WP}$	-0.5V to 13.0V

OPERATING RANGES

RATING	VALUE
Ambient Temperature	0℃ to 70℃ (Comm.)
	-40℃ to 85℃ (Ind.)
Vcc Supply Voltage	2.7V to 3.6V

NOTICE:

1.This document contains information on product in the dsign phase of development. Revised information will be published when the product is available.

2.Specifications contained within the following tables are subject to change.

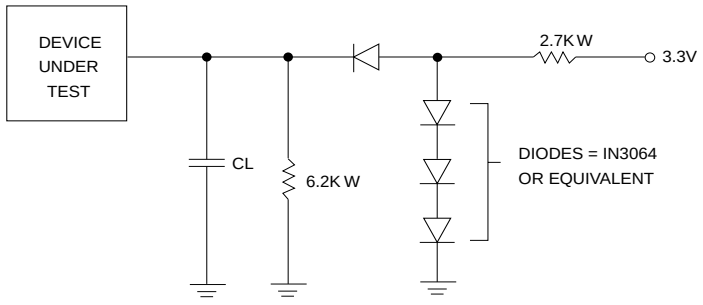
WARNING:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

CAPACITANCE TA = 25℃, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			14	pF	VIN = 0V
COUT	Output Capacitance			16	pF	VOUT = 0V

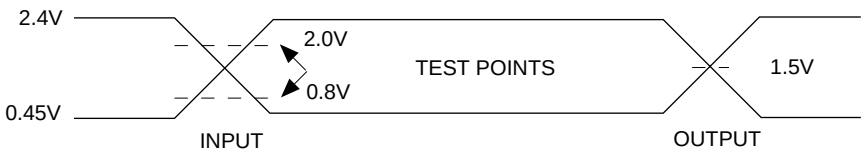
SWITCHING TEST CIRCUITS



CL = 100 pF Including jig capacitance for 150/200ns

CL = 50 pF for 120ns

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".

Input pulse rise and fall times are 5ns.

5.1 DC CHARACTERISTICS Vcc = 2.7V to 3.6V

SYMBOL	PARAMETER	NOTES	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
IIL	Input Load Current	1			±1	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current	1			±10	uA	VCC = VCC Max VIN = VCC or GND
ISB1	VCC Standby Current(CMOS)	1		20	30	uA	VCC = VCC Max $\overline{CE}$ = VIH
ISB2	VCC Standby Current(TTL)			1	2	mA	VCC = VCC Max $\overline{CE}$ = VIH
ICC1	VCC Read Current	1		20	35	mA	VCC = VCC Max f = 10MHz, IOUT = 0 mA
ICC2	VCC Erase Suspend Current	1,2			5	mA	$\overline{CE}$ = VIH Block Erase Suspended
ICC3	VCC Program Current	1		15	30	mA	Program in Progress
ICC4	VCC Erase Current	1		15	30	mA	Erase in Progress
IPPD	VCC Deep Power-down Current			1	8	uA	VCC = VCC Max $\overline{RP}$ = VIL
VIL	Input Low Voltage	3	-0.3		0.6	V	
VIH	Input High Voltage	4	2.0		VCC+0.3	V	
VOL	Output Low Voltage				0.45	V	IOL = 2.1mA, Vcc = Vcc Min
VOH	Output High Voltage		2.4			V	IOH = -100uA, Vcc = Vcc Min

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at VCC = 3.0V, T = 25℃. These currents are valid for all product versions (package and speeds).
2. ICC2 is specified with the device de-selected. If the device is read while in erase suspend mode, current draw is the sum of ICC2 and ICC1.
3. VIL min. = -1.0V for pulse width£50ns.
   VIL min. = -2.0V for pulse width£20ns.
4. VIH max. = VCC + 1.5V for pulse width£20ns. If VIH is over the specified maximum value, read operation cannot be guaranteed.

5.2 AC CHARACTERISTICS --- READ OPERATIONS

		29L8100T/B-12		29L8100T/B-15		29L8100T/B-20			
SYMBOL	DESCRIPTIONS	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		120		150		200	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		120		150		200	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		60		75		100	ns	$\overline{CE}$=VIL
tDF(1)	$\overline{OE}$ High to Output Delay	0	55	0	55	0	55	ns	$\overline{CE}$=VIL
tOH	Address to Output hold	0		0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL
tBACC	$\overline{BYTE}$ to Output Delay		120		150		200	ns	$\overline{CE}$=$\overline{OE}$=VIL
tBHZ	$\overline{BYTE}$ Low to Output in HighZ		55		55		70	ns	$\overline{CE}$=VIL

TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V
- Input rise and fall times: 5ns
- Output load: 1TTL gate+100pF(Including scope and jig) (100pF loading for 150ns, 200ns read speed.) (50pF loading for 120ns read speed.)
- Reference levels for measuring timing: 1.5V

NOTE:

1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Figure 6.1 READ TIMING WAVEFORMS

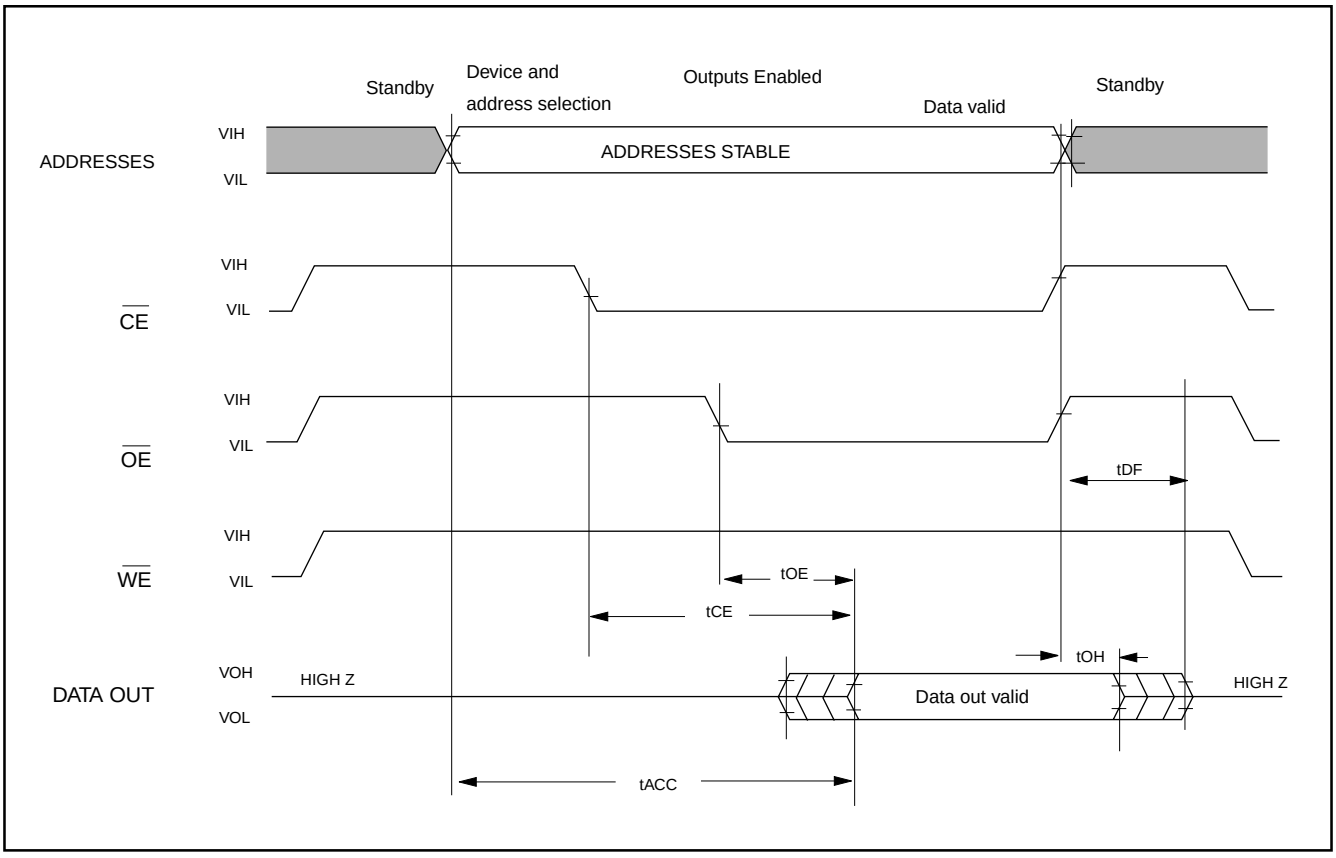
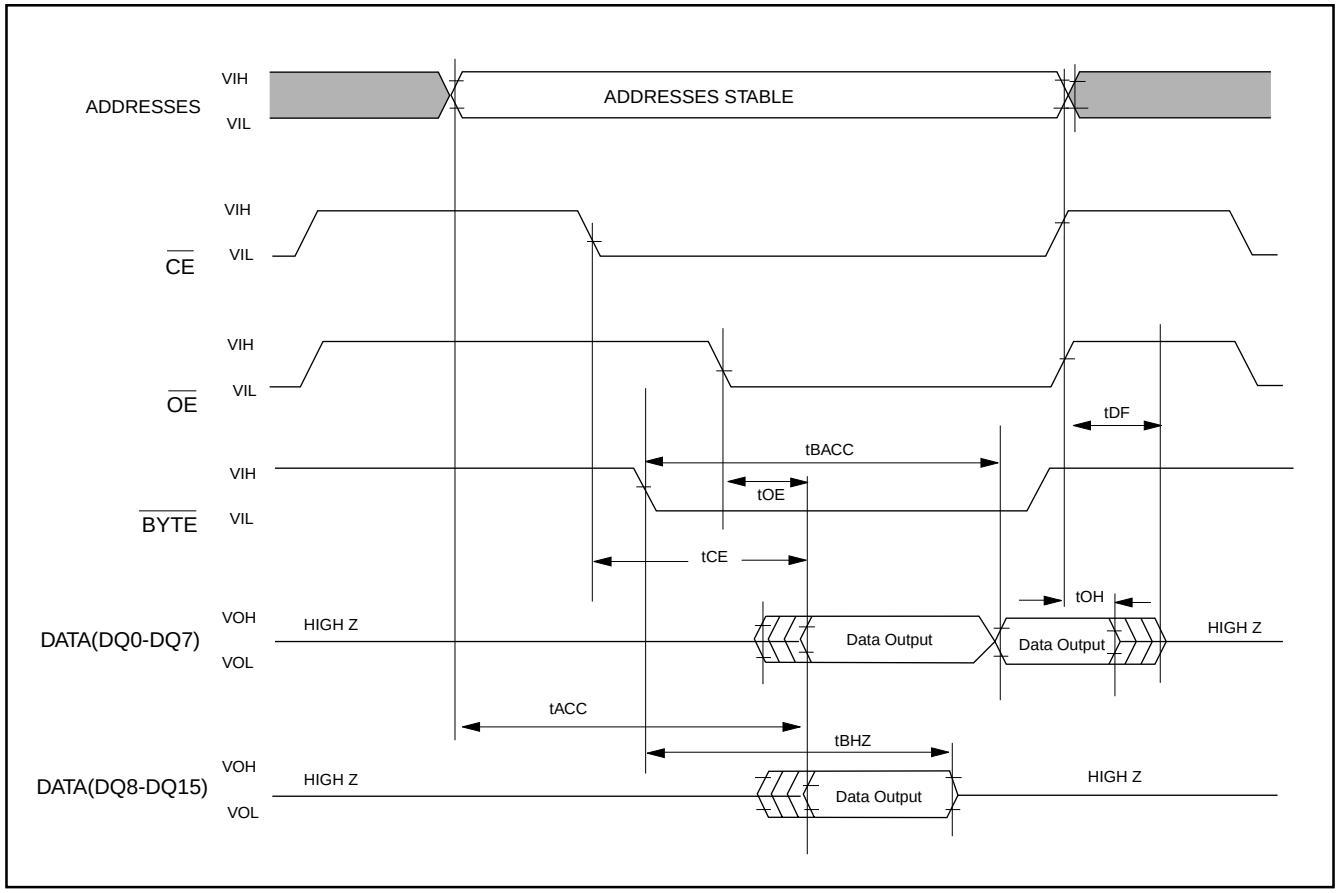


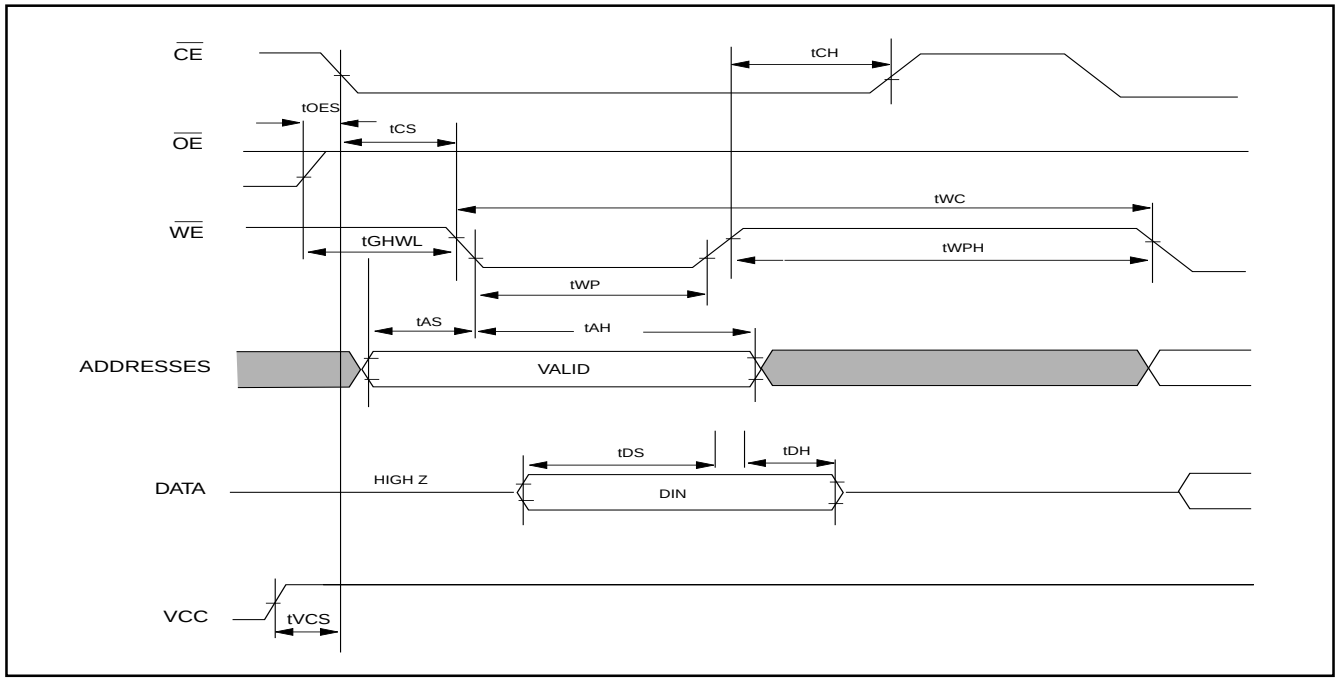
Figure 6.2 BYTE TIMING WAVEFORMS



5.3 AC CHARACTERISTICS --- WRITE/ERASE/PROGRAM OPERATIONS

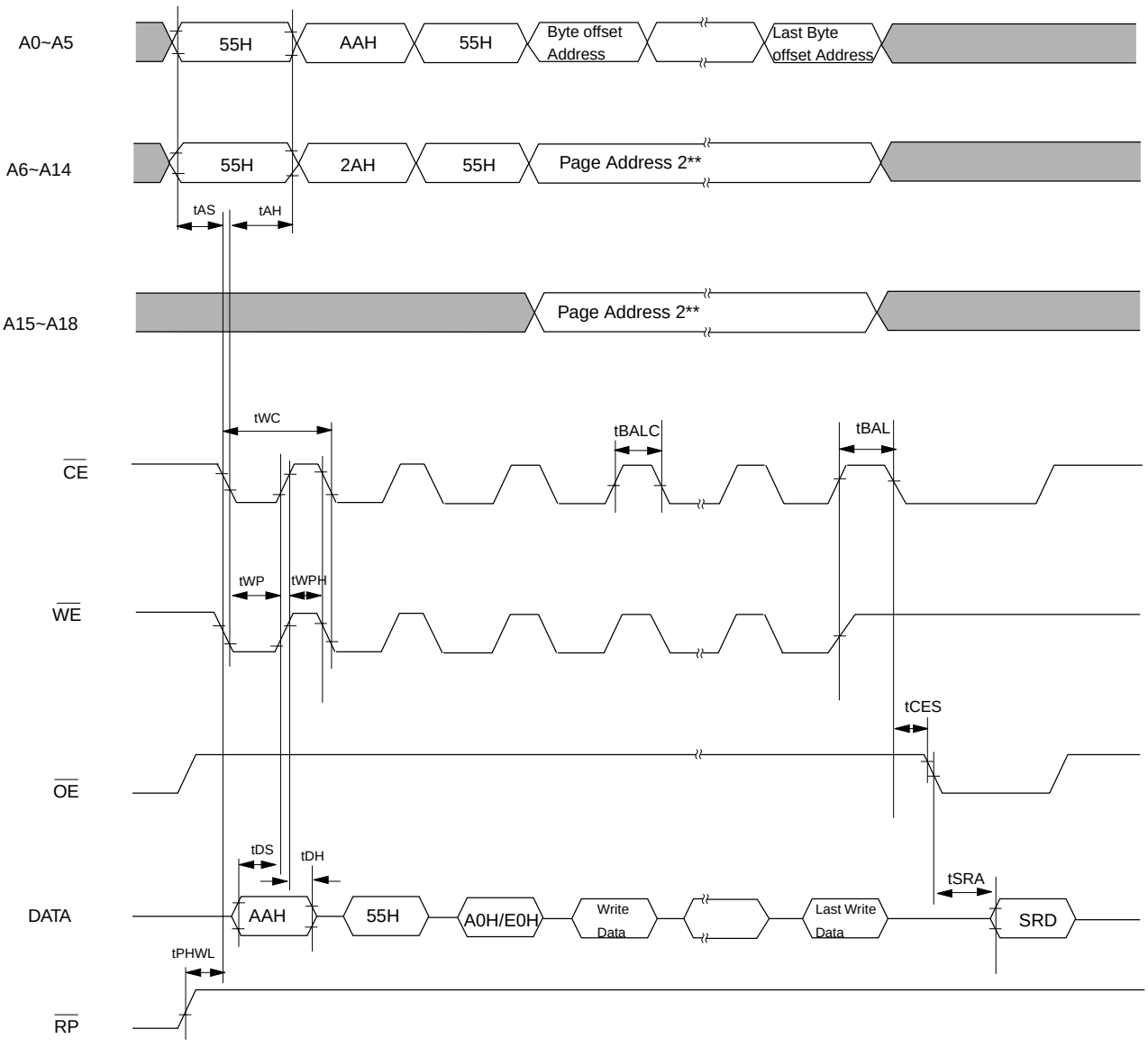
		29L8100T/B-12		29L8100T/B-15		29L8100T/B-20		
SYMBOL	**DESCRIPTIONS**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**UNIT**
tWC	Write Cycle Time	120		150		200		ns
tAS	Address Setup Time	0		0		0		ns
tAH	Address Hold Time	60		60		60		ns
tDS	Data Setup Time	50		50		50		ns
tDH	Data Hold Time	10		10		10		ns
tOES	Output Enable Setup Time	0		0		0		ns
tCES	$\overline{CE}$ Setup Time	0		0		0		ns
tGHWL	Read Recover Time Before Write	0		0		0		ns
tCS	CE Setup Time	0		0		0		ns
tCH	$\overline{CE}$ Hold Time	0		0		0		ns
tWP	$\overline{Write}$ Pulse Width	60		60		60		ns
tWPH	Write Pulse Width High	40		40		40		ns
tBALC	Byte Address Load Cycle	0.2	30	0.2	30	0.2	30	us
tBAL	Byte Address Load Time	100		100		100		us
tSRA	Status Register Access Time	120		150		200		ns
tCESR	$\overline{CE}$ Setup before S.R. Read	100		100		100		ns
tPHWL	$\overline{RP}$ High Recovery to $\overline{WE}$ Going Low	1		1		1		us
tVCS	VCC Setup Time	2		2		2		us

Figure 7. COMMAND WRITE TIMING WAVEFORMS



NOTE:$\overline{BYTE}$ pin is treated as Address pin. All timing specifications for $\overline{BYTE}$ pin are the same as those for address pin.

Figure 8. AUTOMATIC PAGE PROGRAM/WRITE PAGE BUFFER TIMING WAVEFORMS

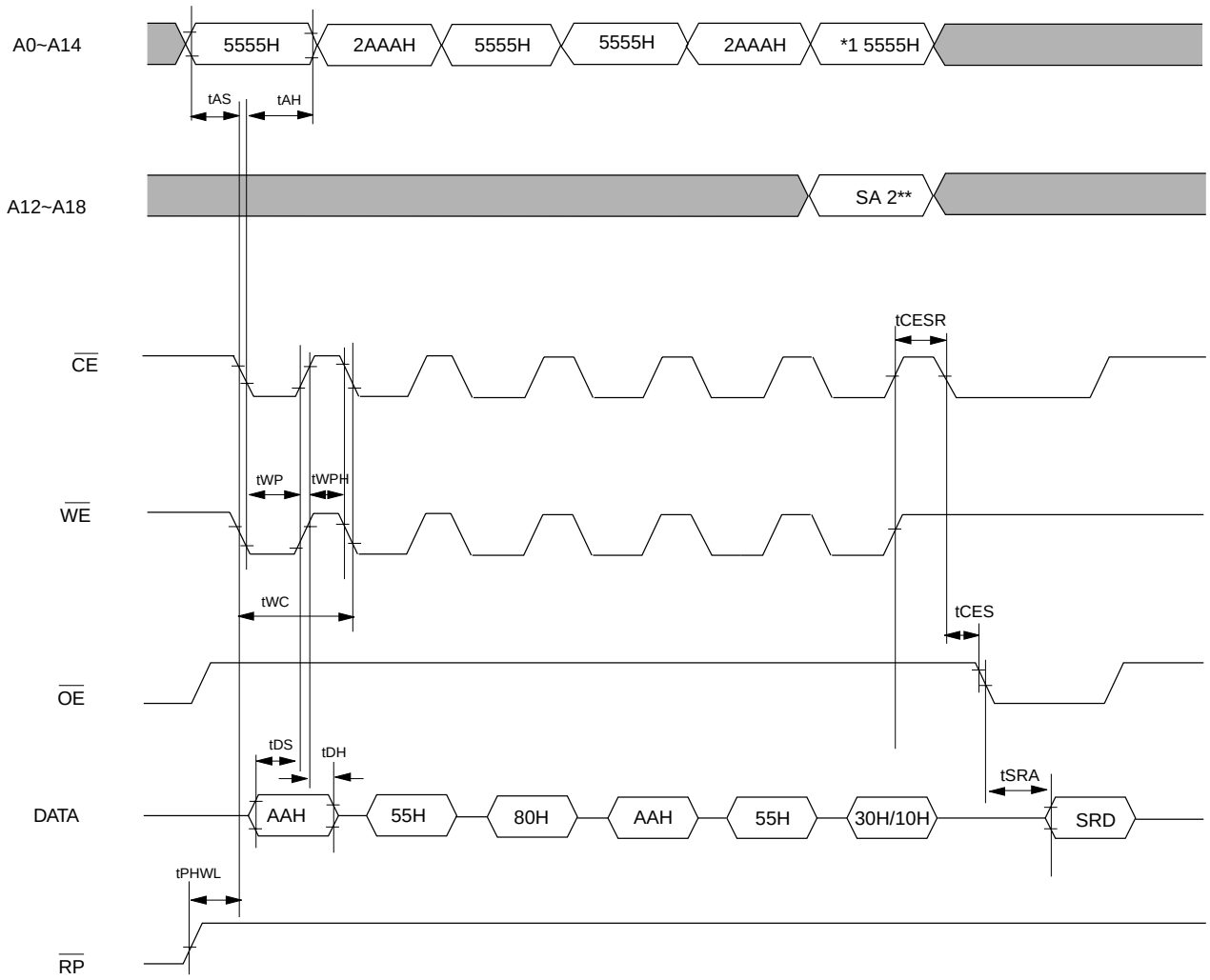


NOTE:

1.Please refer to SECTION 2.3 for detail page program operation.

**2.Page address is not required for Write Page Buffer

Figure 9. AUTOMATIC BLOCK/CHIP ERASE TIMING WAVEFORMS



NOTES:

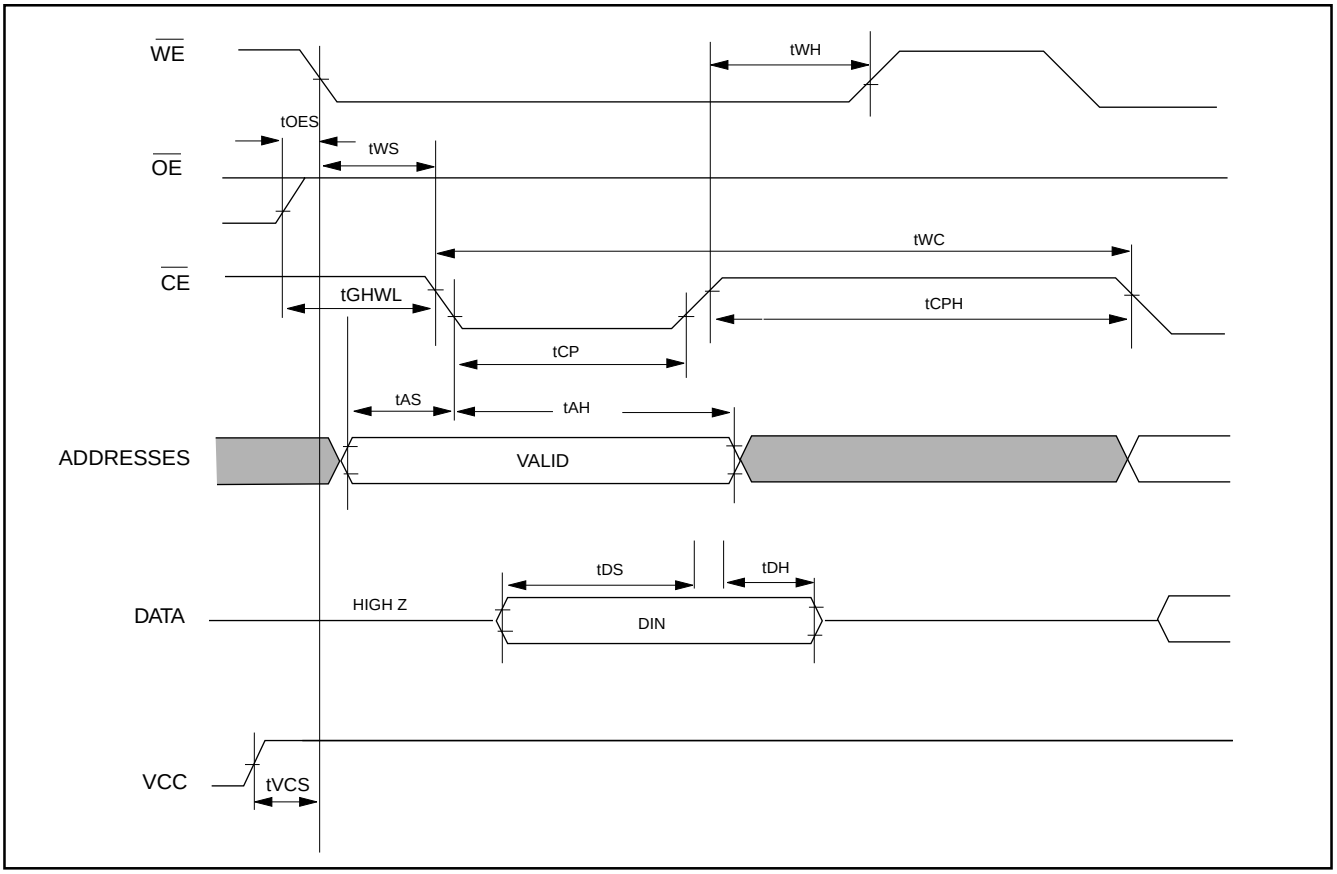
*1. "X" means "don't care" in this diagram

**2."SA" means "Block Address"(required for Block Erase only)

5.4 AC CHARACTERISTICS --- WRITE/ERASE/PROGRAM OPERATIONS (Alternate $\overline{CE}$ Controlled)

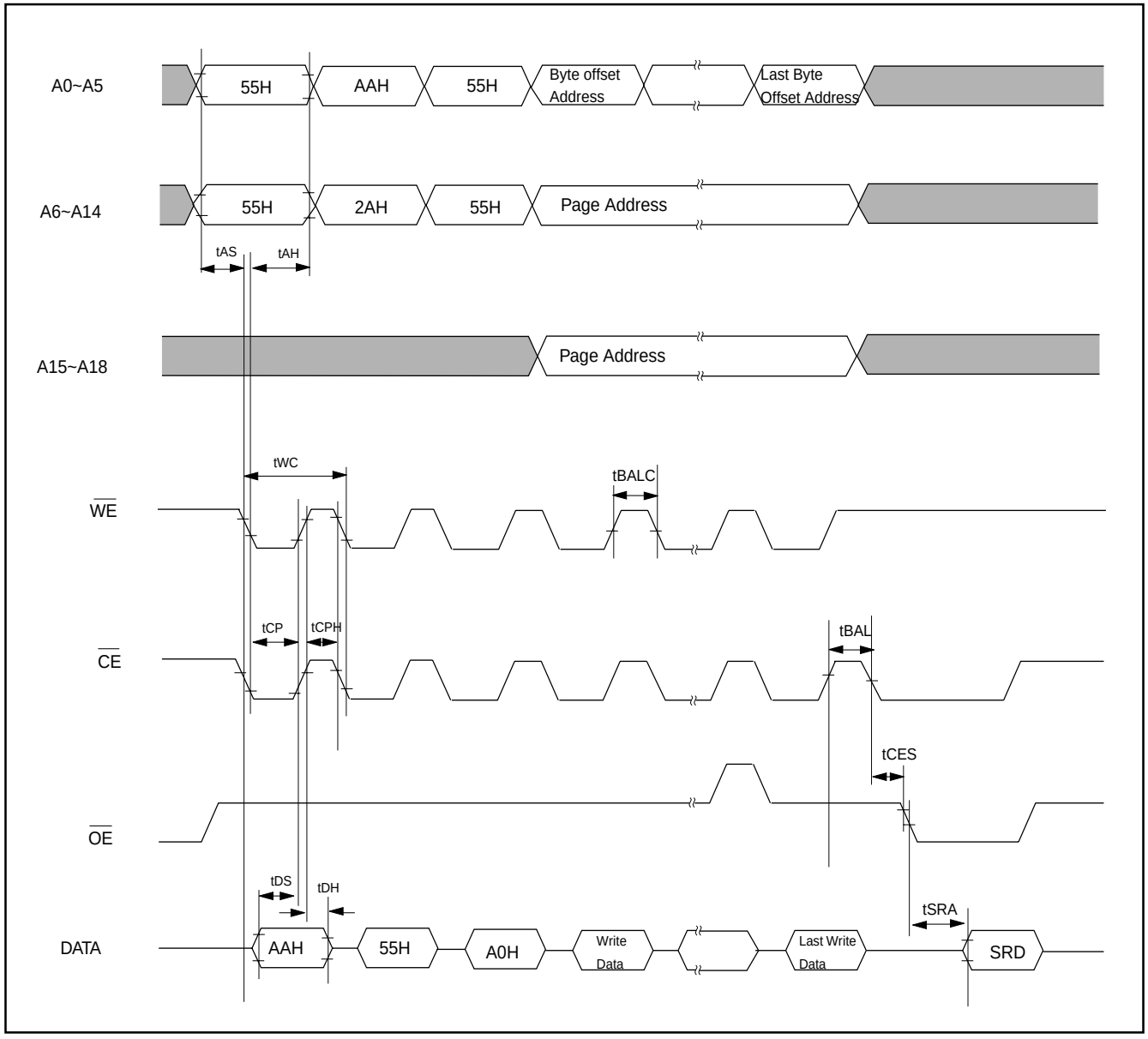
		29L8100T/B-12		29L8100T/B-15		29L8100T/B-20		
SYMBOL	DESCRIPTIONS	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT
tWC	Write Cycle Time	120		150		200		ns
tAS	Address Setup Time	10		10		10		ns
tAH	Address Hold Time	60		60		60		ns
tDS	Data Setup Time	50		50		50		ns
tDH	Data Hold Time	10		10		10		ns
tOES	Output Enable Setup Time	0		0		0		ns
tCES	$\overline{CE}$ Setup Time	0		0		0		ns
tGHWL	Read Recover TimeBefore Write	0		0		0		ns
tWS	$\overline{WE}$ Setup Time	0		0		0		ns
tWH	$\overline{WE}$ Hold Time	0		0		0		ns
tCP	$\overline{CE}$ Pulse Width	60		60		60		ns
tCPH	$\overline{CE}$ Pulse Width High	40		40		40		ns
tVCS	VCC Setup Time	2		2		2		uA

Figure 10. COMMAND WRITE TIMING WAVEFORMS(Alternate $\overline{CE}$ Controlled)



NOTE:$\overline{BYTE}$ pin is treated as Address pin. All timing specifications for $\overline{BYTE}$ pin are the same as those for address pin.

Figure 11. AUTOMATIC PAGE PROGRAM TIMING WAVEFORM(Alternate $\overline{CE}$ Controlled)



5.5 ERASE AND PROGRAMMING PERFORMANCE

		LIMITS		
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Chip/Sector Erase Time		50		ms
Page Programming Time		5		ms
Chip Programming Time		40		sec
Byte Program Time(average)		40		us
Erase/Program Cycles	100,000			Cycles

5.6 LATCHUP CHARACTERISTICS

	MIN.	**MAX.**
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 3.0V, one pin at a time.		

REVISION HISTORY

Revision	Description	Page	Date
1.1	Adding status register "SLK" column.(page 13)		APR/14/1997
1.2	Change Program/Erase cycle from 1,000 to 1,000/10,000. Page 10:Table 4 "Verify 16K-block protect" : A18~A2 X--->SA.		AUG/22/1997
1.3	Write-Erase cycles change from 1,000/10,000 to 100,000.		OCT/29/1997
1.4	Adding CSP Package		JAN/12/1998
1.5	Taa:150ns@2.7V -->Taa:120ns @2.7V		MAY/27/1998
1.6	Corrected Pin-assignment of the CSP.		AUG/24/1998
1.7	Add in new CSP with 0.8mm ball pitch.		SEP/24/1998

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