FEB 1 9 1991

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

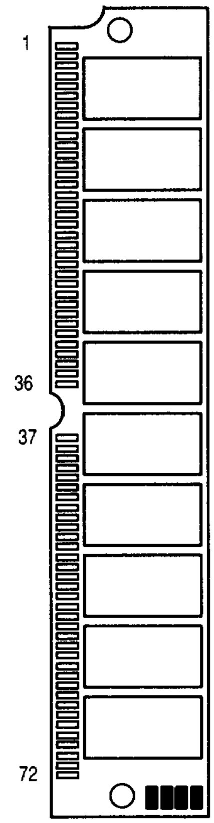
Order this data sheet
by MCM40512/D

MCM40512
MCM40L512

Product Preview
512K × 40 Bit Dynamic Random Access Memory Module
for Error Correction Applications

The MCM40512S and MCM40L512S are 20M, dynamic random access memory (DRAM) modules organized as 524,288 × 40 bits. The module is a double-sided 72-lead single-in-line memory module (SIMM) consisting of twenty MCM514256A DRAMs housed in 20/26 J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM514256A is a 1.0 µ CMOS high speed, dynamic random access memory organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM40512 = 8 ms (Max)
  MCM40L512 = 64 ms (Max)
- Consists of Twenty 256K × 4 DRAMs, and Twenty 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM40512S-70 = 70 ns (Max)
  MCM40512S-80 = 80 ns (Max)
  MCM40512S-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM40512S-70 = 4.51 W (Max)
  MCM40512S-80 = 3.96 W (Max)
  MCM40512S-10 = 3.41 W (Max)
- Low Standby Power Dissipation:
  TTL Levels = 220 mW (Max)
  CMOS Levels (MCM40512) = 110 mW (Max)
  (MCM40L512) = 22 mW (Max)



PIN OUT

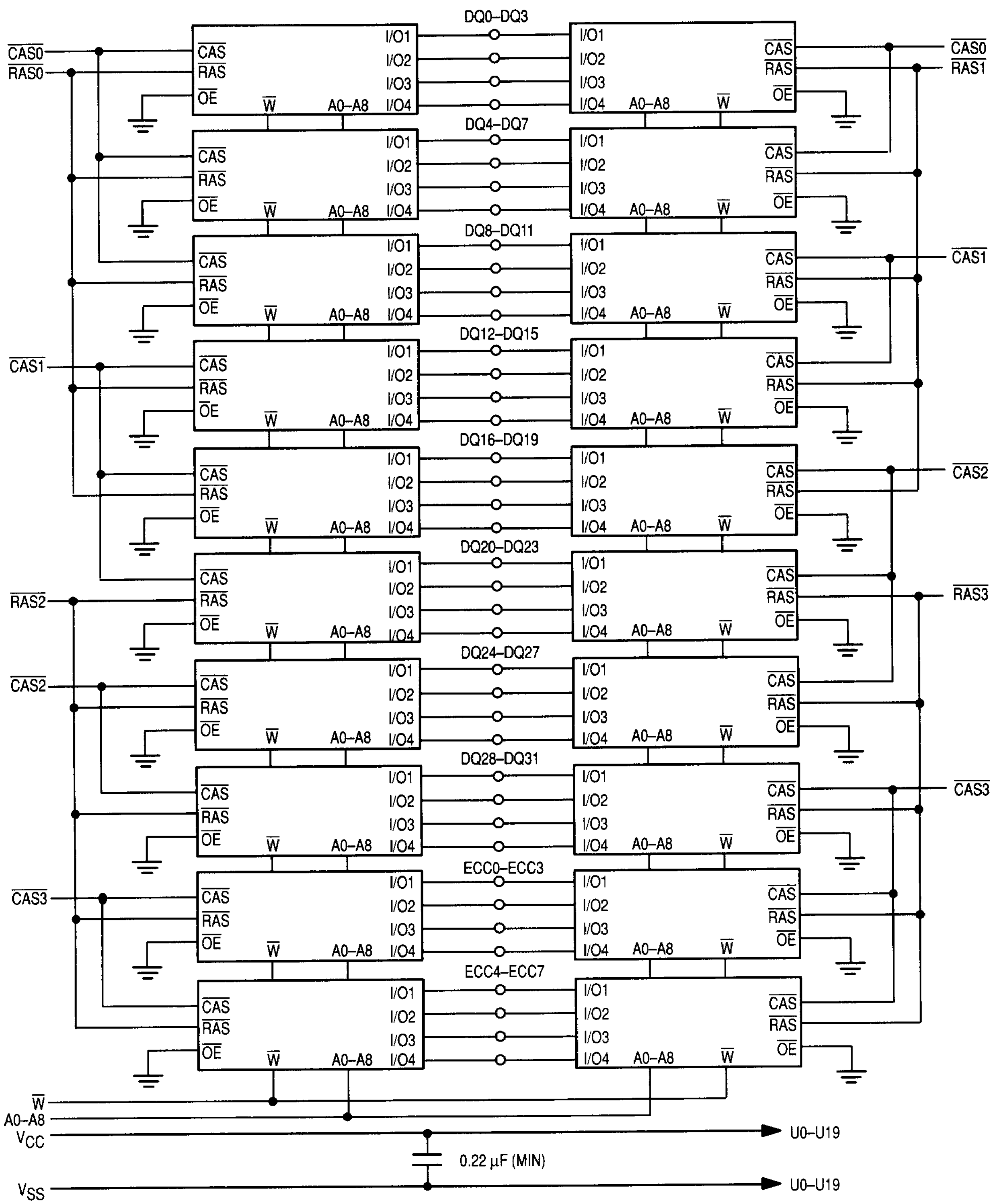
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ22	37	ECC3	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	ECC4	50	DQ24	62	DQ20
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	ECC0	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	ECC6
7	DQ18	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ11	67	PD1
8	DQ3	20	DQ4	32	NC	44	$\overline{RAS0}$	56	DQ27	68	PD2
9	DQ19	21	DQ20	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ12	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	ECC5	58	DQ28	70	PD4
11	NC	23	DQ21	35	ECC1	47	$\overline{W}$	59	V_{CC}	71	ECC7
12	A0	24	DQ6	36	ECC2	48	CD	60	DQ29	72	V_{SS}

PIN NAMES	
A0–A8	Address Inputs
DQ0–DQ31	Data Input/Output
ECC0–ECC7	Error Correction Data I/O
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
PD1–PD4	Presence Detect
$\overline{RAS0}$–$\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
CD	Configuration Detection
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

512K × 40 BLOCK DIAGRAM



Presence Detect Pin Out			
Pin Name	**70 ns**	**80 ns**	**100 ns**
PD1	NC	NC	NC
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	V_{SS}	NC	V_{SS}
PD4	NC	V_{SS}	V_{SS}
CD	V_{SS}	V_{SS}	V_{SS}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC})	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	6.15	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedence circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V	1

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM40512-70, t_{RC} = 130 ns		—	820		
MCM40512-80, t_{RC} = 150 ns		—	720		
MCM40512-10, t_{RC} = 180 ns		—	620		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	40	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles	I_{CC3}			mA	2
MCM40512-70, t_{RC} = 130 ns		—	820		
MCM40512-80, t_{RC} = 150 ns		—	720		
MCM40512-10, t_{RC} = 180 ns		—	620		
V_{CC} Power Supply Current During Fast Page Mode Cycle	I_{CC4}			mA	2
MCM40512-70, t_{RC} = 40 ns		—	620		
MCM40512-80, t_{RC} = 45 ns		—	520		
MCM40512-10, t_{RC} = 55 ns		—	420		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM40512	I_{CC5}	—	20	mA	
MCM40L512		—	4		
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM40512-70, t_{RC} = 130 ns		—	820		
MCM40512-80, t_{RC} = 150 ns		—	720		
MCM40512-10, t_{RC} = 180 ns		—	620		
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 200	200	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Max	Unit	Notes
Input Capacitance (A0–A8)	C_{I1}	—	110	pF	1
Input Capacitance ($\overline{W}$)	C_{I2}	—	150	pF	1
Input Capacitance ($\overline{RAS0}$–$\overline{RAS3}$)	C_{I3}	—	45	pF	1
Input Capacitance ($\overline{CAS0}$–$\overline{CAS3}$)	C_{I4}	—	45	pF	1
I/O Capacitance (DQ0–DQ31)	C_{DQ1}	—	24	pF	1
I/O Capacitance (ECC0–ECC7)	C_{DQ2}	—	24	pF	1

NOTE:

1. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = 1 Δ t / Δ V.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM40512-70		MCM40512-80		MCM40512-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	55	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	—	50	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	25	—	25	—	ns	
$\overline{CAS}$ Hold TIme	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	12

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively to t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

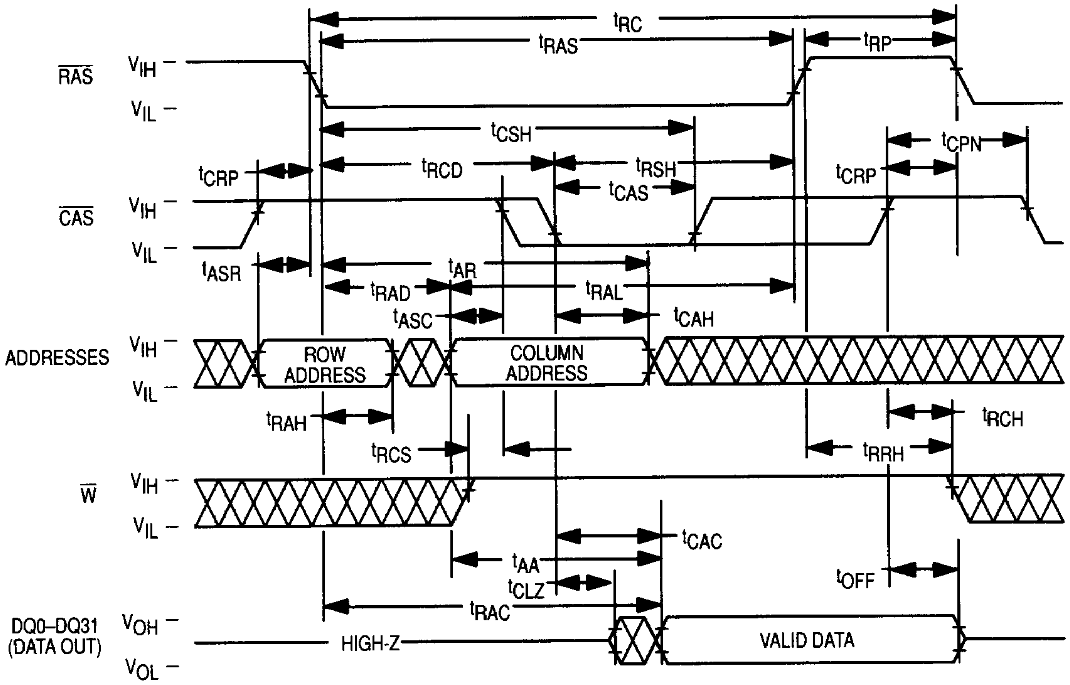
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM40512-70		MCM40512-80		MCM40512-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cyle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	—	60	—	75	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	50	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	—	60	—	75	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14, 15
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	14, 15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	—	60	—	75	—	ns	
Refresh Period MCM40512 MCM40L512	t_{RVRV}	t_{RFSH}	— —	8 64	— —	8 64	— —	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15, 16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	30	—	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	15	—	ns	

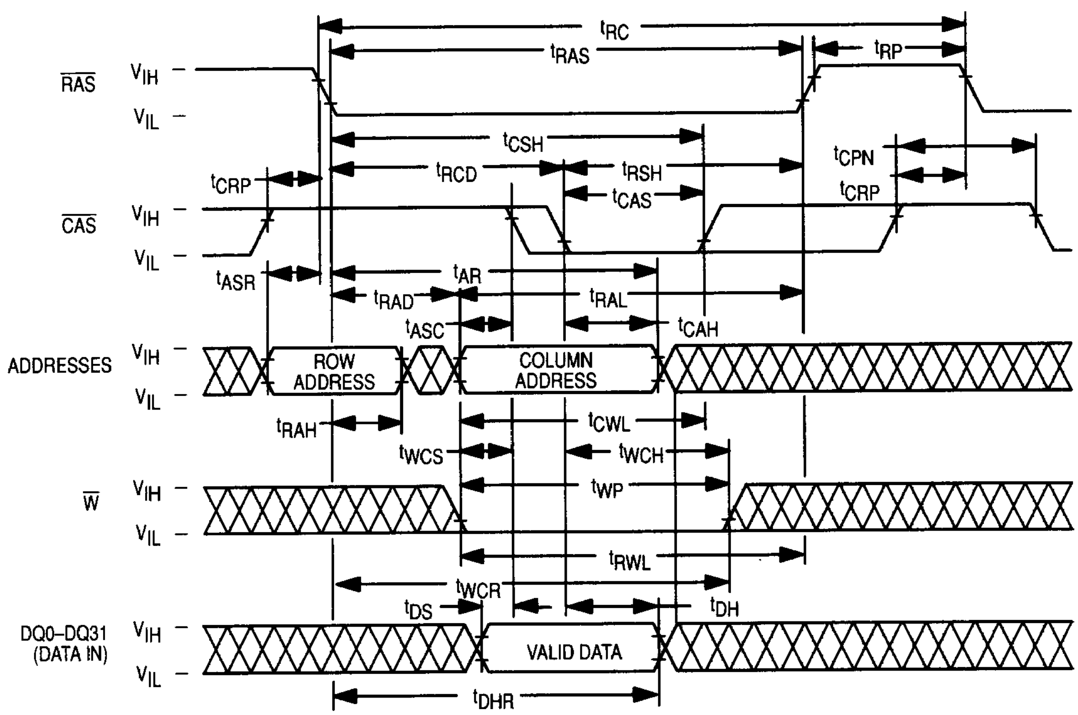
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles.
15. Early write only ($t_{WCS} \geq t_{WCS}$ (min)).
16. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.
17. To avoid bus contention and potential damage to the module, $\overline{RAS0}$ and $\overline{RAS1}$ may not be active low simultaneously. Similarly, $\overline{RAS2}$ and $\overline{RAS3}$ may not be simultaneously active low.

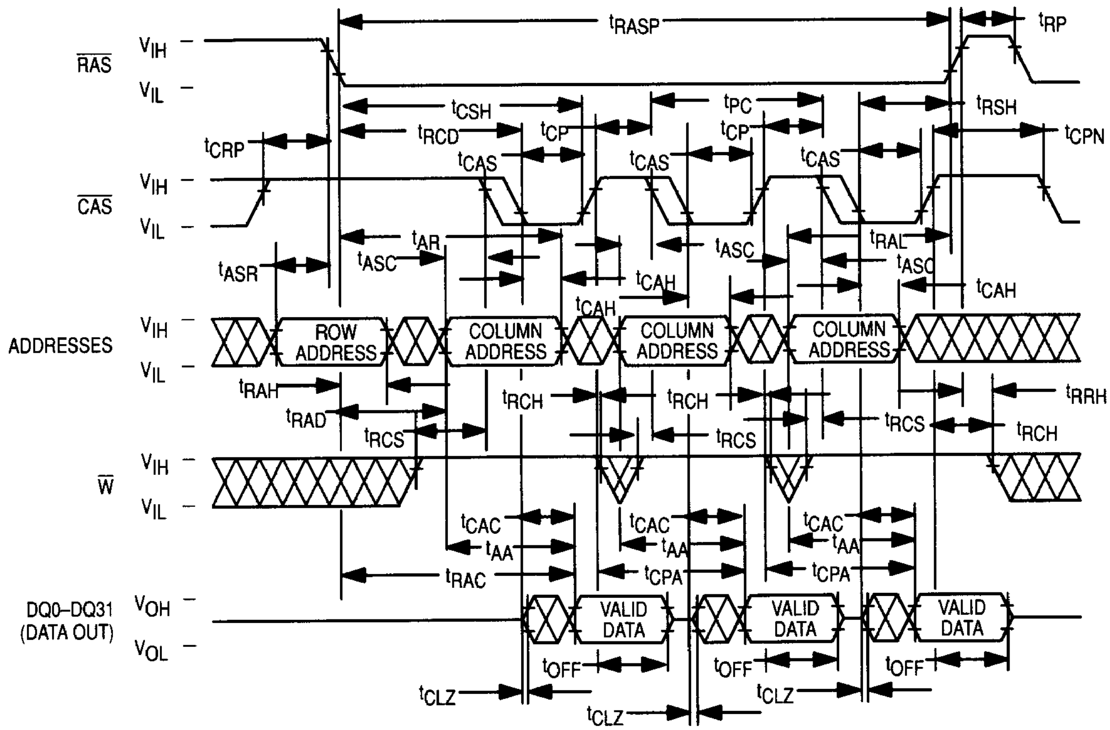
READ CYCLE



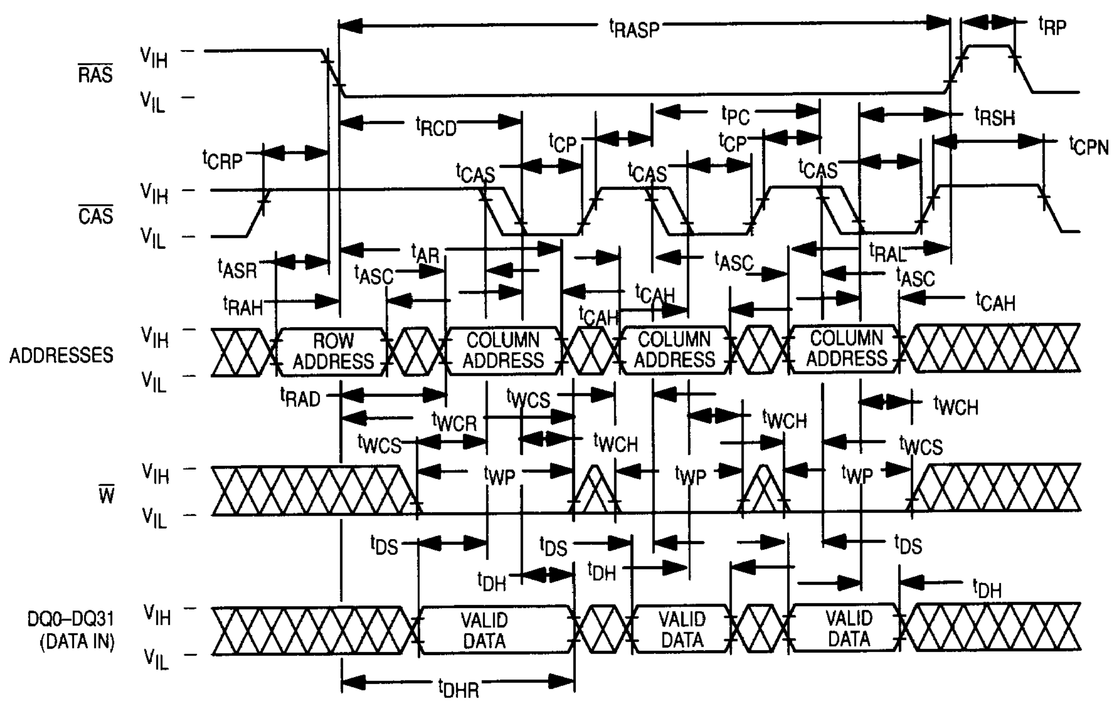
EARLY WRITE CYCLE



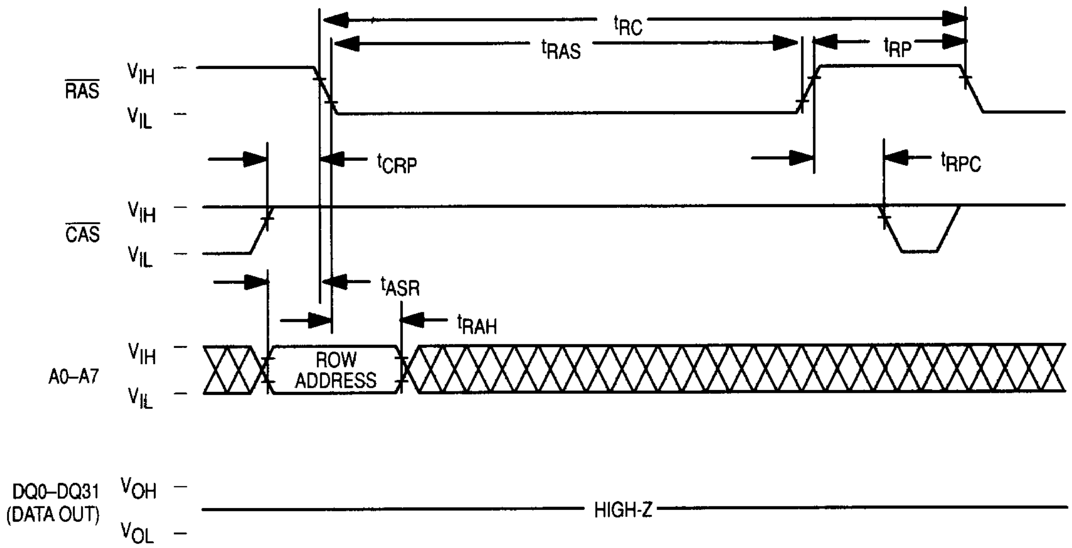
FAST PAGE MODE READ CYCLE



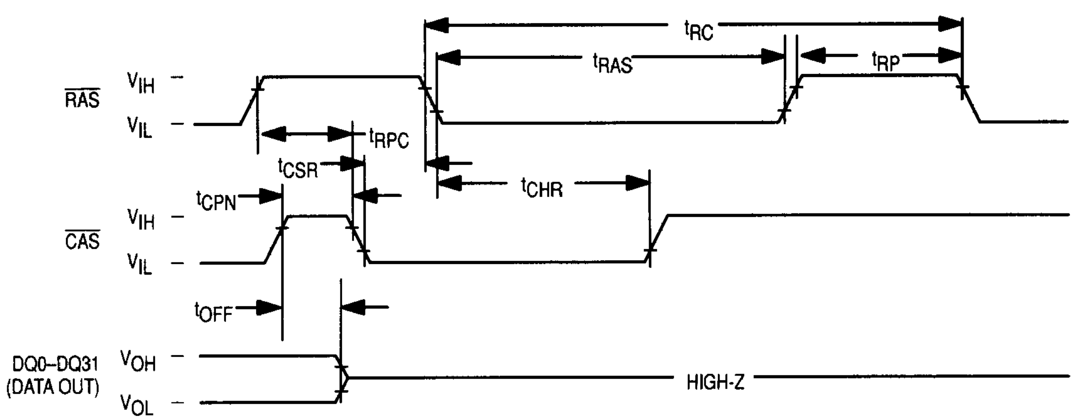
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



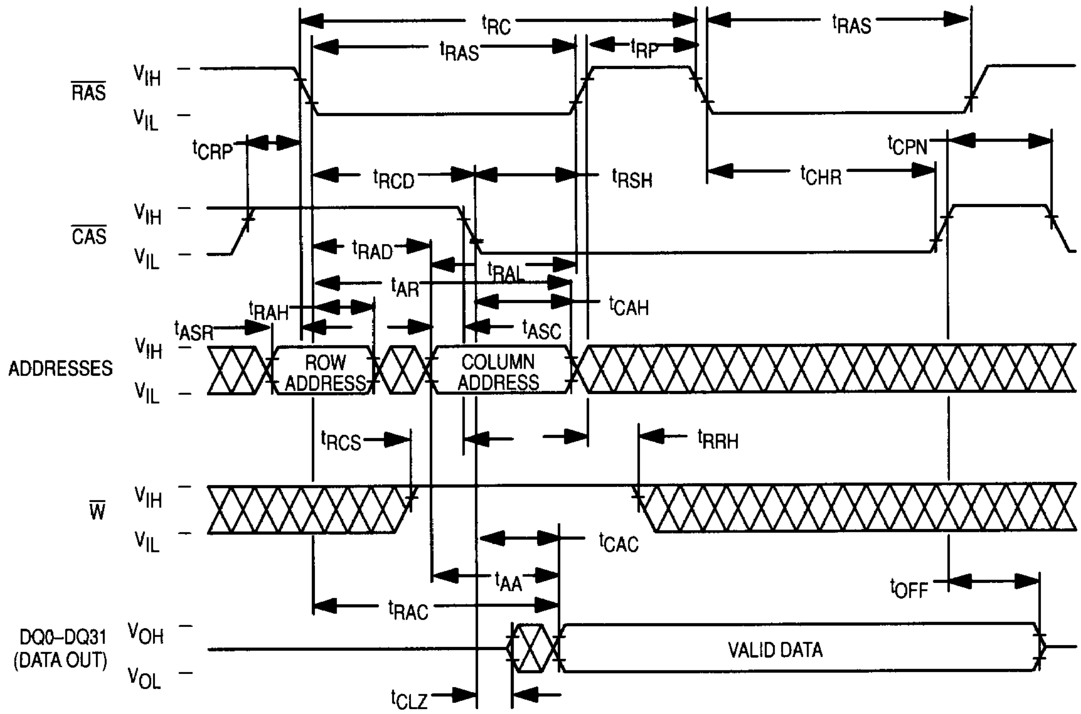
RAS ONLY REFRESH CYCLE (W and A8 are Don't Care)



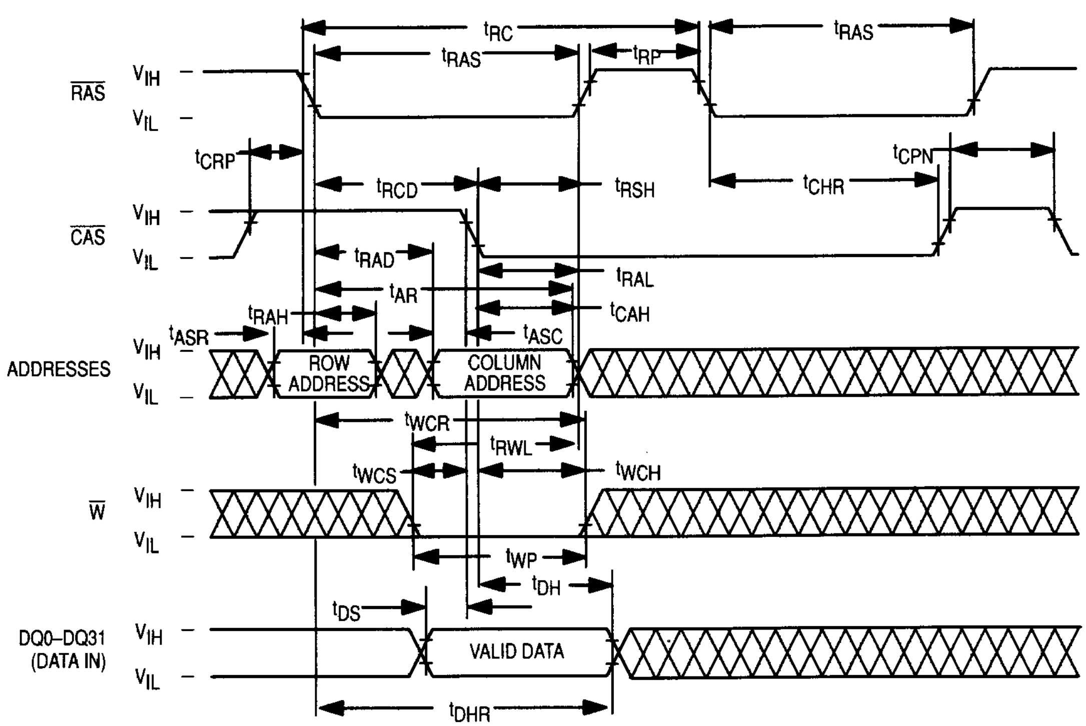
CAS BEFORE RAS REFRESH CYCLE (W and A0 to A8 are Don't Care)



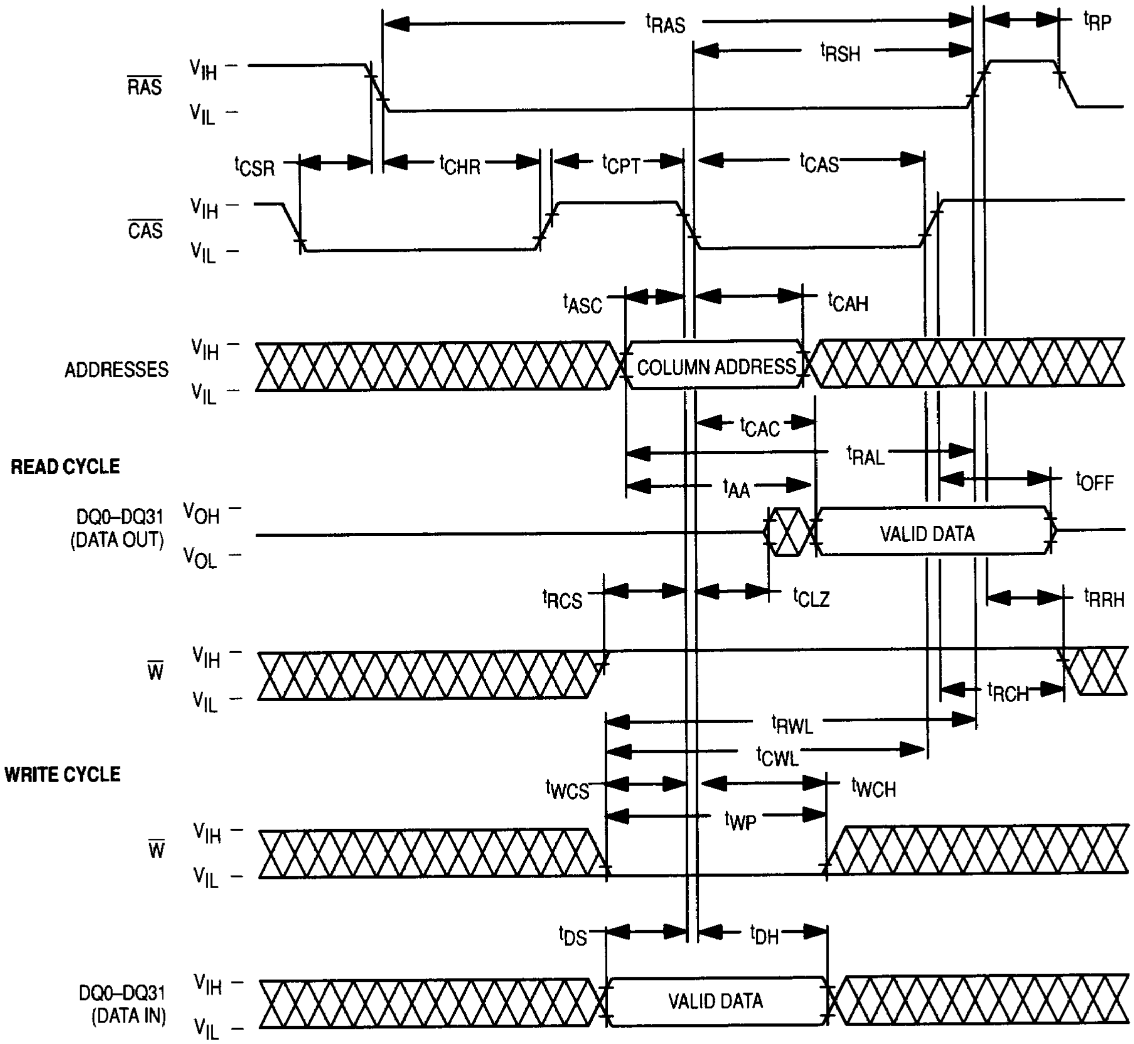
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the module. During an extended inactive state of the module (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address bus pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of eighteen address bits will decode one of the 524,288 word locations in the device. The column address strobe follows the row address strobe by a specified minimum and maxium time called t_{RCD}, which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up the external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. These are, however, other variations in addressing the module: the refresh modes ($\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh), and another mode called page mode which allows the user to column access all words within a selected row. The refresh mode and page mode operations are described in more detail in later sections.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, which is covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from the row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 512 column locations on a selected row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 10-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In practice, any combination of read and write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the module needs to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the module will also refresh all the words associated with the particular row(s) decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{CAS}$ before $\overline{RAS}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, and read "0" out of the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read cycle**. Repeat this operation 512 times.
3. Select a column address, and write "1" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, write cycle**. Repeat this operation 512 times.
4. Read "1"s (normal read mode), which were written at step 3.
5. Repeat steps 1 to 4 using complement data.

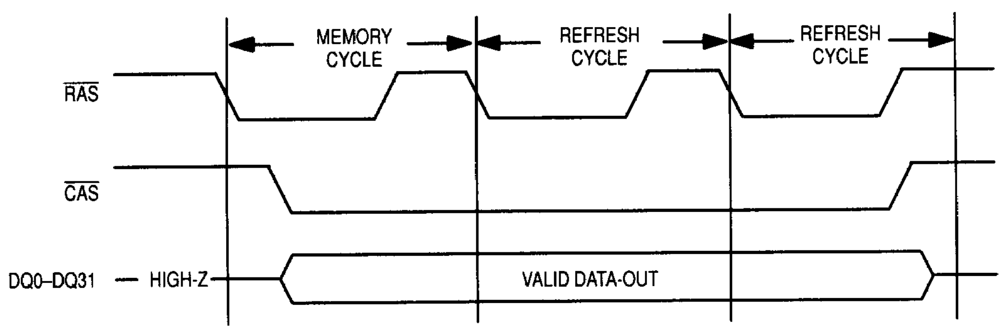
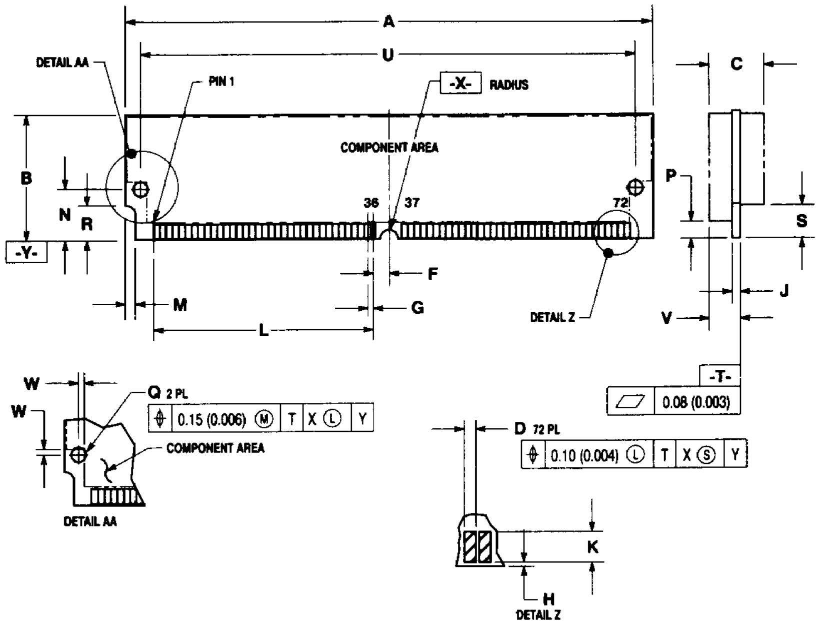


Figure 1. Hidden Refresh Cycle

PACKAGE DIMENSION

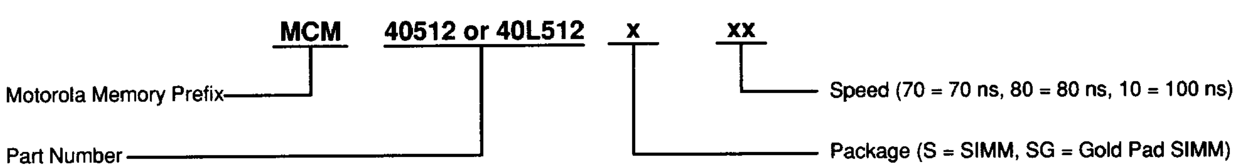
S PACKAGE
SIMM MODULE
CASE 866-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	107.82	108.08	4.245	4.255
B	25.27	25.53	0.995	1.005
C	—	9.14	—	0.360
D	1.02	1.07	0.040	0.042
F	3.18 BSC		0.125 BSC	
G	1.27 BSC		0.050 BSC	
H	—	0.25	—	0.010
J	1.19	1.37	0.047	0.054
K	0.25	—	0.100	—
L	44.45 REF		1.750 REF	
M	1.90	2.16	0.075	0.085
N	10.16 BSC		0.400 BSC	
P	3.18	—	0.125	—
Q	3.12	3.22	0.123	0.127
R	6.22	6.48	0.245	0.255
S	5.72	—	0.225	—
U	101.19 BSC		3.984 BSC	
V	—	5.28	—	0.208
W	1.12	—	0.044	—
X	1.52	1.63	0.060	0.064

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers – MCM40512S70 MCM40512SG70
MCM40512S80 MCM40512SG80
MCM40512S10 MCM40512SG10

MCM40L512S70 MCM40L512SG70
MCM40L512S80 MCM40L512SG80
MCM40L512S10 MCM40L512SG10