ICS84330-02

700MHz, Low Jitter, Crystal-to-3.3V Differential LVPECL Frequency Synthesizer

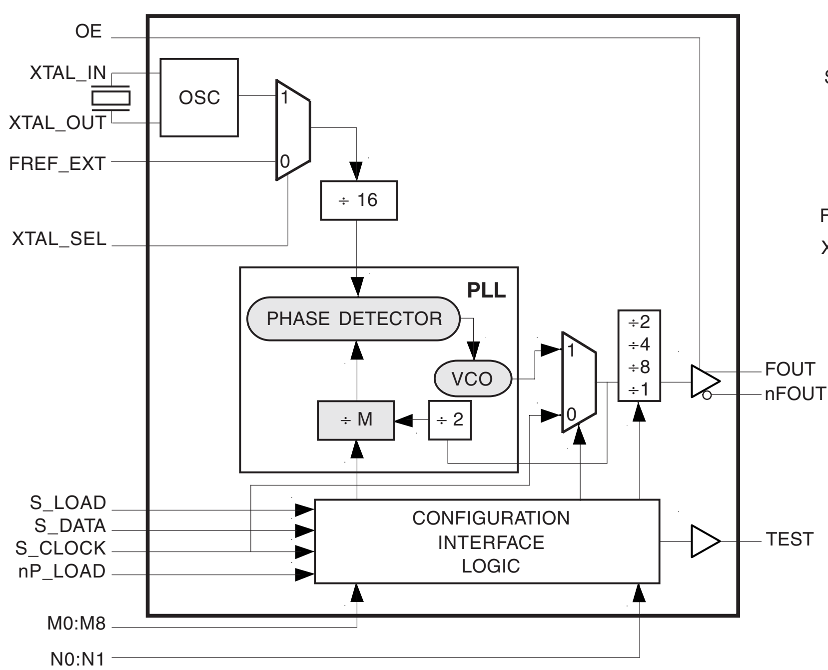
General Description

The ICS84330-02 is a general purpose, single output high frequency synthesizer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The VCO operates at a frequency range of 250MHz to 700MHz. The VCO and output frequency can be programmed using the serial or parallel interfaces to the configuration logic. The output can be configured to divide the VCO frequency by 1, 2, 4, and 8. Output frequency steps from 250kHz to 2MHz can be achieved using a 16MHz crystal depending on the output divider setting.

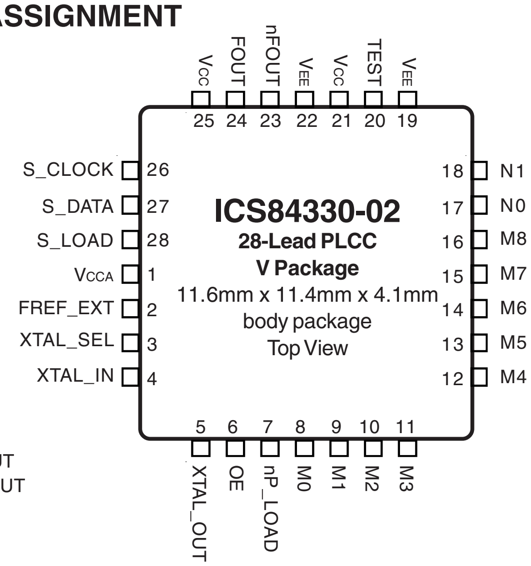
Features

- Fully integrated PLL, no external loop filter requirements
- 1 differential 3.3V LVPECL output
- Crystal oscillator interface: 10MHz to 25MHz
- Output frequency range: 31.25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- Parallel or serial interface for programming M and N dividers during power-up
- RMS Period jitter: 5ps (maximum)
- Cycle-to-cycle jitter: 40ps (maximum)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Lead-Free package fully RoHS compliant
- Industrial temperature information available upon request

Block Diagram



Pin Assignment



Functional Description

NOTE: The functional description that follows describes operation using a 16MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 6, NOTE 1.

The ICS84330-02 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A quartz crystal is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector. With a 16MHz crystal this provides a 1MHz reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be 2M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS84330-02 support two input modes to program the M divider and N output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode the nP_LOAD input is LOW. The data on inputs M0 through M8 and N0 through N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. The TEST output is Mode 000 (shift register out) when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows: $fVCO = \frac{fxtal}{16} \times 2M$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock are defined as $125 \leq M \leq 350$. The frequency out is defined as follows: $fout = \frac{fVCO}{N} = \frac{fxtal}{16} \times \frac{2M}{N}$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T2:T0. The internal registers T2:T0 determine the state of the TEST output as follows:

T2	T1	T0	TEST Output	fOUT
0	0	0	Shift Register Out	fOUT
0	0	1	High	fOUT
0	1	0	PLL Reference Xtal ÷ 16	fOUT
0	1	1	(VCO ÷ M) /2 (non 50% Duty Cycle M divider)	fOUT
1	0	0	fOUT LVCMOS Output Frequency < 200MHz	fOUT
1	0	1	Low	fOUT
1	1	0	(S_CLOCK ÷ M) /2 (non 50% Duty Cycle M divider)	S_CLOCK ÷ N divider
1	1	1	fOUT ÷ 4	fOUT

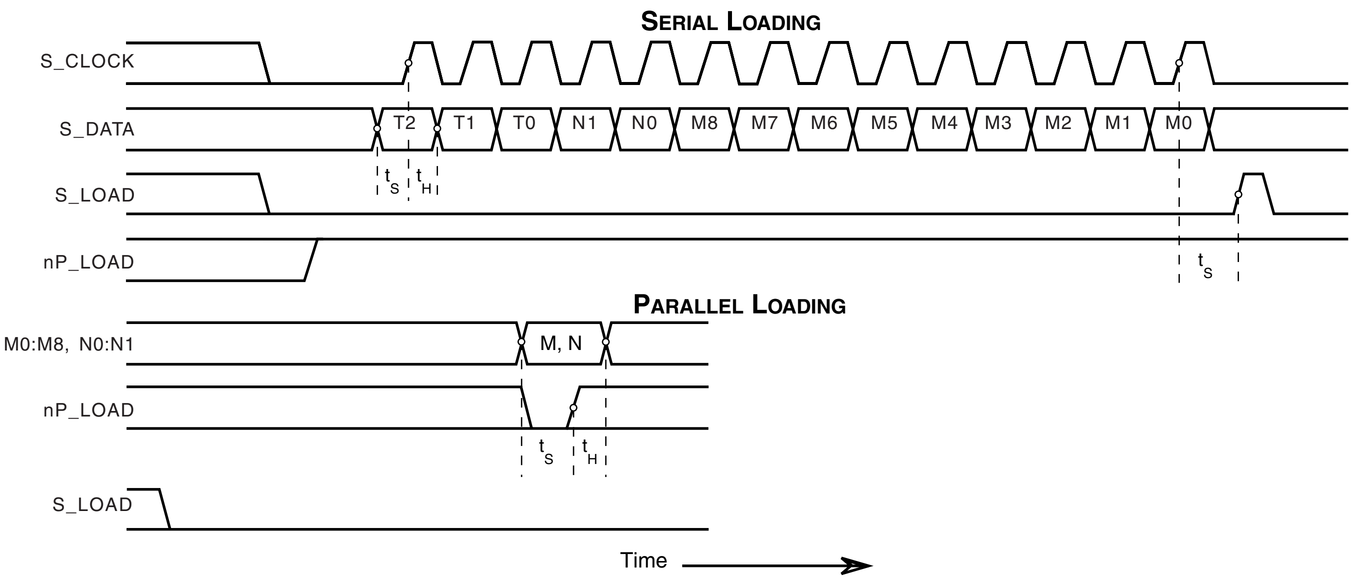


Figure 1. Parallel & Serial Load Operations

NOTE: nP_LOAD is designed to eliminate runt pulses when changing M and N bits.

Table 1. Pin Descriptions

Name	Type		Description
V_{CCA}	Power		Analog supply pin.
XTAL_IN, XTALOUT			Crystal oscillator interface. XTAL_IN is an oscillator input. XTAL_OUT is an oscillator output.
XTAL_SEL	Input	Pullup	Selects between the crystal oscillator or FREF_EXT inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects FREF_EXT when LOW. LVCMOS / LVTTL interface levels.
OE	Input	Pullup	Output enable. LVCMOS / LVTTL interface levels.
nP_LOAD	Input	Pullup	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divide value. LVCMOS / LVTTL interface levels.
M0, M1, M2 M3, M4, M5 M6, M7, M8	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS / LVTTL interface levels.
N0, N1	Input	Pullup	Determines N output divider value as defined in Table 3C Function Table. LVCMOS / LVTTL interface levels.
V_{EE}	Power		Negative supply pins.
TEST	Output		Test output which is used in the serial mode of operation. LVCMOS / LVTTL interface levels.
V_{CC}	Power		Core supply pins.
nFOUT, FOUT	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
nc	Unused		Do not connect.
FREF_EXT	Input	Pulldown	PLL reference input. LVCMOS / LVTTL interface levels.
S_CLOCK	Input	Pulldown	Clocks the serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
S_LOAD	Input	Pulldown	Controls transition of data from shift register into the M divider. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3A. Parallel and Serial Mode Function Table

Inputs						Conditions
nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
L	Data	Data	X	X	X	Data on M and N inputs passed directly to M divider and N output divider. TEST mode 000.
↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
H	X	X	↓	L	Data	M divide and N output divide values are latched.
H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

Table 3B. Programmable VCO Frequency Function Table

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	125	0	0	1	1	1	1	1	0	1
252	126	0	0	1	1	1	1	1	1	0
254	127	0	0	1	1	1	1	1	1	1
256	128	0	1	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
696	348	1	0	1	0	1	1	1	0	0
698	349	1	0	1	0	1	1	1	0	1
700	350	1	0	1	0	1	1	1	1	0

NOTE 1: These M divide values and the resulting frequencies correspond to a crystal frequency of 16MHz.

Table 3C. Programmable Output Divider Function Table

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Minimum	Maximum
0	0	2	125	350
0	1	4	62.5	175
1	0	8	31.25	87.5
1	1	1	250	700

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	37.8°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. DC Power Supply Characteristics, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current				130	mA
I_{CCA}	Analog Supply Current				15	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	M0-M8, N0, N1, OE, nP_LOAD, XTAL_SEL	$V_{CC} = V_{IN} = 3.465V$			5	µA
		S_LOAD, S_CLOCK FREF_EXT, S_DATA	$V_{CC} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	M0-M8, N0, N1, OE, nP_LOAD, XTAL_SEL	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
		S_LOAD, S_CLOCK FREF_EXT, S_DATA	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{CC}/2$.

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		25	MHz
Equivalent Series Resistance (ESR)				70	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

Table 6. Input Frequency Characteristics, $V_{CC} = V_{CCA}$ = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	XTAL; NOTE 1		10		25	MHz
		S_CLOCK				50	MHz
		FREF_EXT; NOTE 2		10		25	MHz

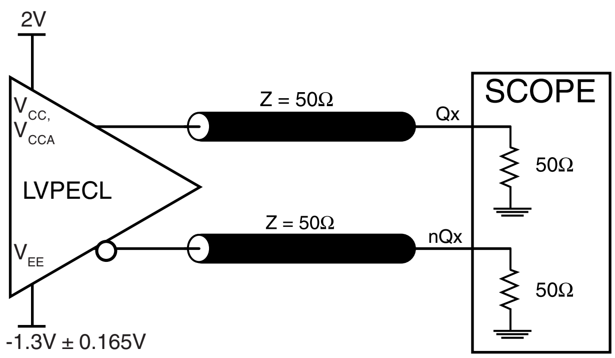
NOTE 1: For the crystal frequency range the M value must be set to achieve the minimum or maximum VCO frequency range of 250MHz to 700MHz. Using the minimum frequency of 10MHz, valid values of M are 200 ≤ M ≤ 511. Using the maximum frequency of 25MHz, valid values of M are 80 ≤ M ≤ 224.
NOTE 2: Maximum frequency on FREF_EXT is dependent on the internal M counter limitations. See Application Information Section for recommendations on optimizing the performance using the FREF_EXT input.

Table 7. AC Characteristics, $V_{CC} = V_{CCA}$ = 3.3V±5%, TA = 0°C to 70°C

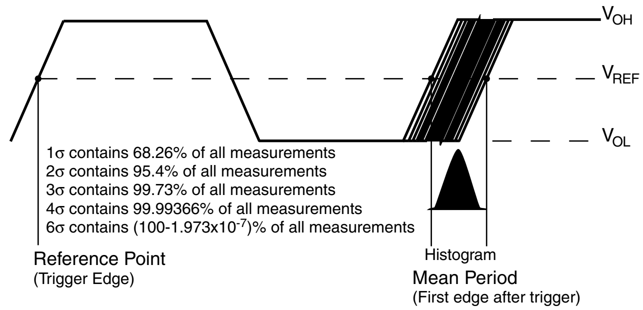
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency					700	MHz
tjit(per)	Period Jitter, RMS; NOTE 1, 2					5	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 2					40	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		600	ps
t_{nP_LOAD}	Input Rise Time	Parallel Data Load Time	20% to 80%			50	ns
t_S	Setup Time	S_DATA to S_CLOCK		20			ns
		S_CLOCK to S_LOAD		20			ns
		M, N to nP_LOAD		20			ns
t_H	Hold Time	S_DATA to S_CLOCK		20			ns
		M, N to nP_LOAD		20			ns
t_L	PLL Lock Time					10	ms
odc	Output Duty Cycle		N ≠ 1	45		55	%
			N = 1, fOUT ≤ 250MHz	45		55	%
			N = 1, 250MHz < fOUT ≤ 500MHz	40		60	%

See Parameter Measurement Information section.
Characterized using a XTAL input.
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65
NOTE 2: See Applications section.

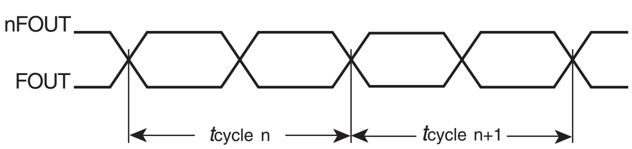
Parameter Measurement Information



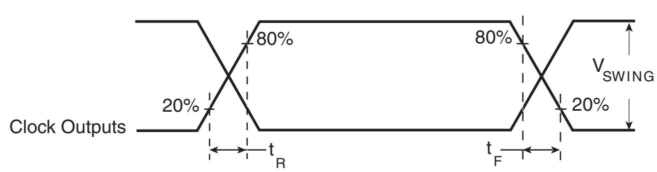
3.3V Output Load AC Test Circuit



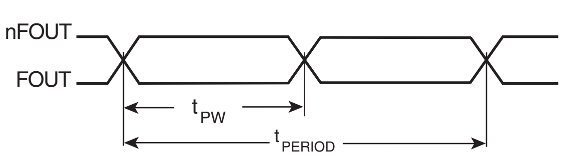
Period Jitter



Cycle-to-Cycle Jitter



Output Rise/Fall Time



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS84330-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

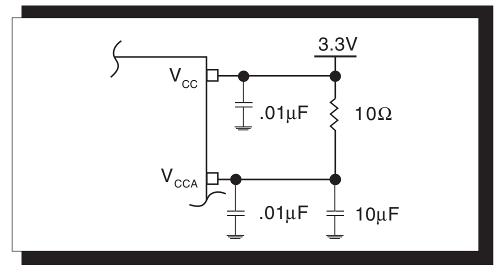


Figure 2. Power Supply Filtering

Termination for LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

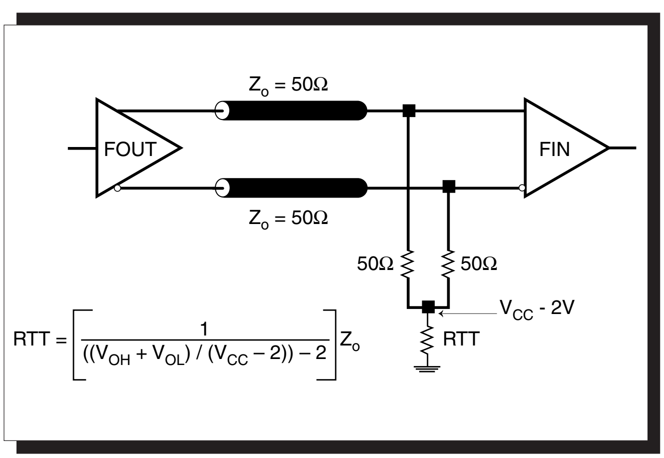


Figure 3A. LVPECL Output Termination

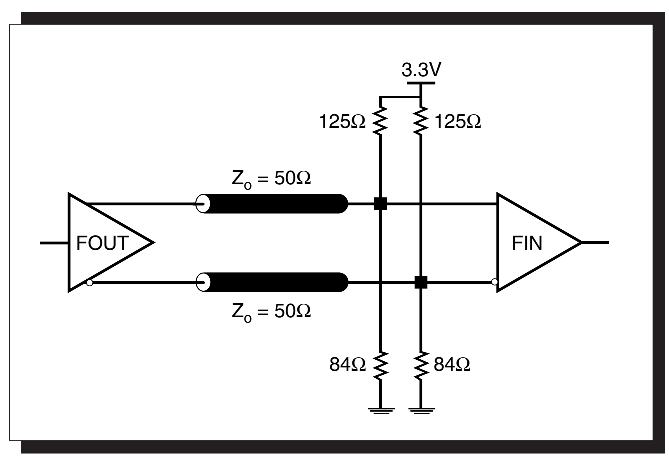


Figure 3B. LVPECL Output Termination

LVCMOS to XTAL Interface

The XTAL_IN input can accept single ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 4*. The XTAL_OUT input can be left floating. The edge rate can be as slow as 10ns. If the incoming signal has sharp edge rate and the signal path is a long trace, proper termination for the driver and controlled characteristic impedance trace may be required. The input can function with half swing amplitude. Reducing amplitude from full swing of 3.3V to half swing of about 1.65V can prevent signal interfere with power rail and may reduce noise. Please refer to the LVCMOS driver data sheet and application note for amplitude reduction and termination approach.

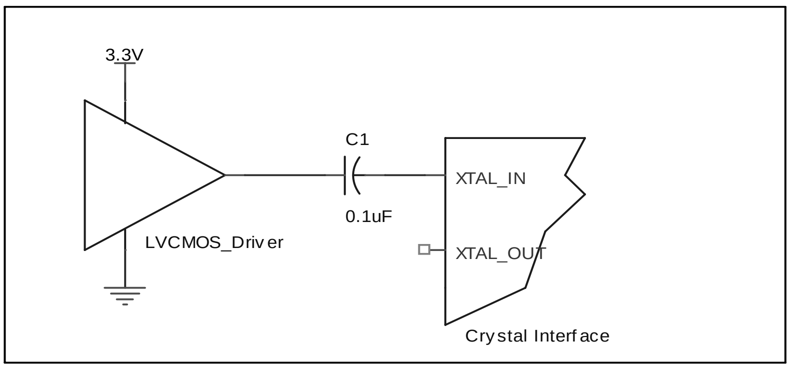


Figure 4. General Diagram for LVCMOS Driver to XTAL Input Interface

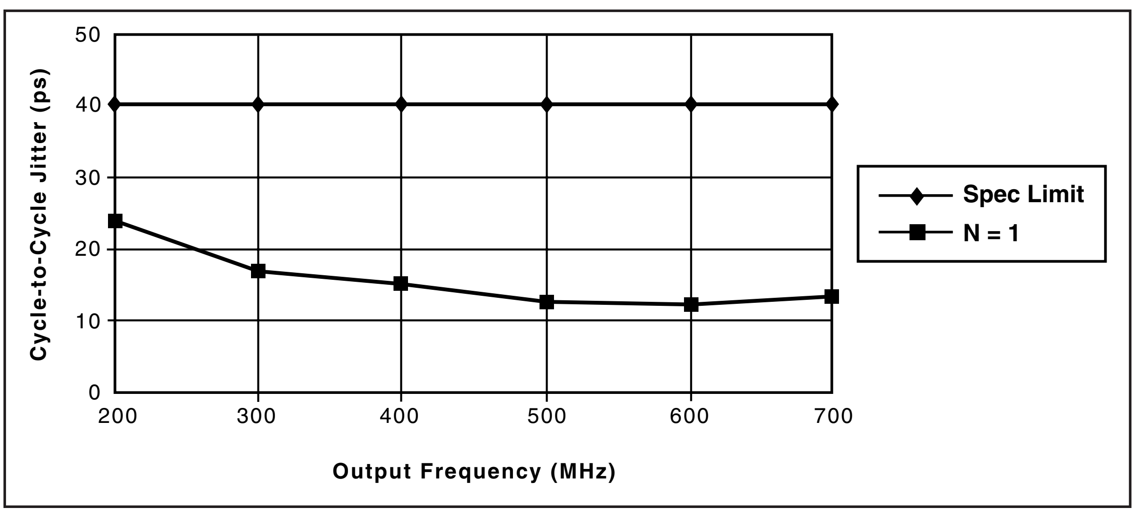


Figure 5. Cycle-to-Cycle Jitter vs. fOUT (using a 16MHz XTAL)

Layout Guideline

The schematic of the ICS84330-02 layout example used in this layout guideline is shown in *Figure 6A.* The ICS84330-02 recommended PCB board layout for this example is shown in *Figure 6B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

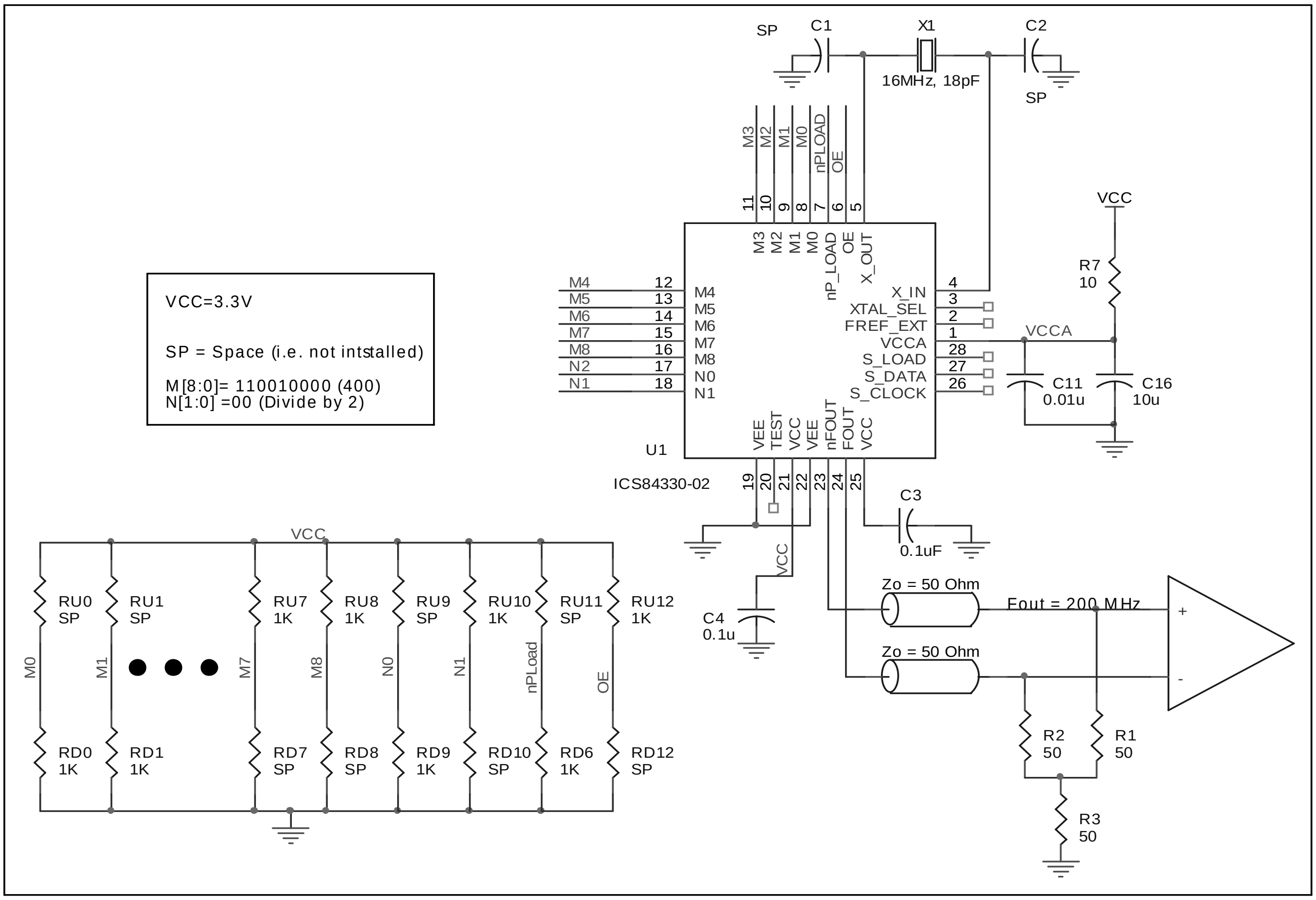


Figure 6A. Schematic of Recommended Layout

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors C3 and C4, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{CCA} pin as possible.

Clock Traces and Termination

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have the same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

Crystal

The crystal X1 should be located as close as possible to the pins 4 (XTAL_IN) and 5 (XTAL_OUT). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

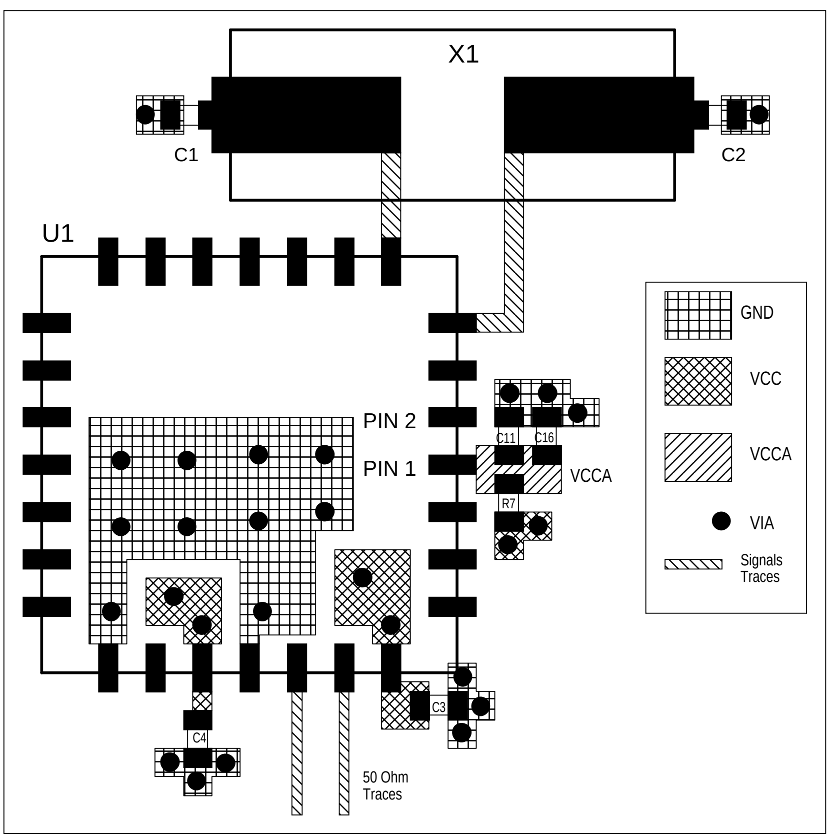


Figure 6B. PCB Board Layout for ICS84330-02

Jitter Reduction for FREF_EXT Single End Input

If the FREF_EXT input is driven by a 3.3V LVCMOS driver, the jitter performance can be improved by reducing the amplitude swing and slowing down the edge rate. *Figure 7A* shows an amplitude reduction approach for a long trace. The swing will be approximately 0.85V for logic low and 2.5V for logic high (instead of 0V to 3.3V). *Figure 7B* shows amplitude reduction approach for a short trace. The circuit shown in *Figure 7C* reduces amplitude swing and also slows down the edge rate by increasing the resistor value.

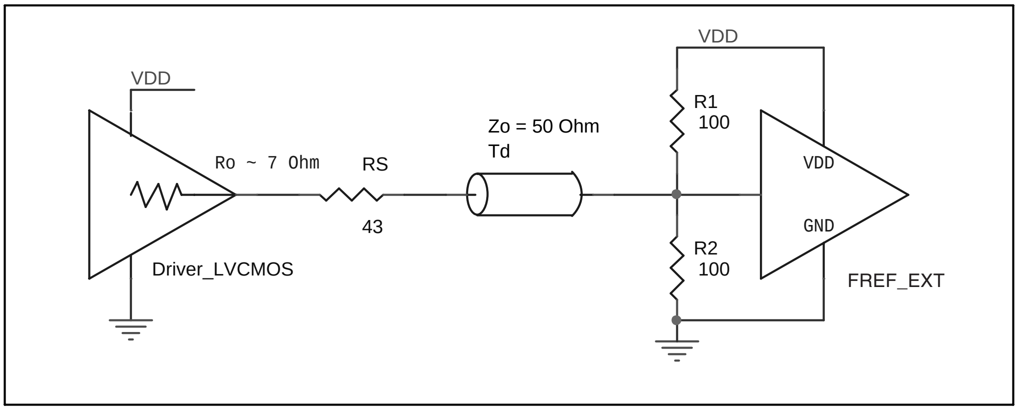


Figure 7A. Amplitude Reduction for a Long Trace

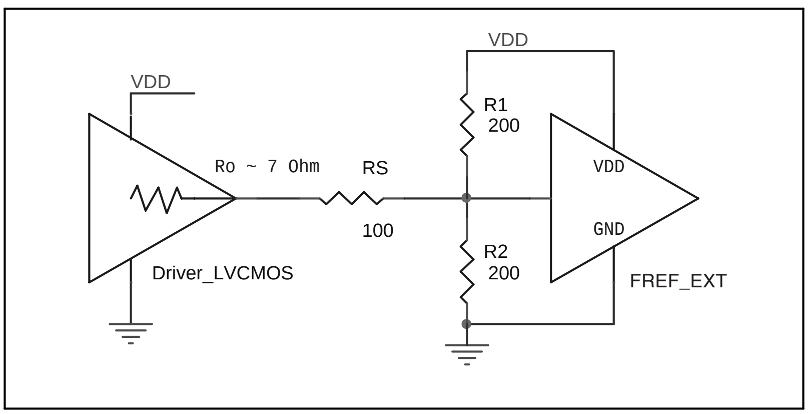


Figure 7B. Amplitude Reduction for a Short Trace

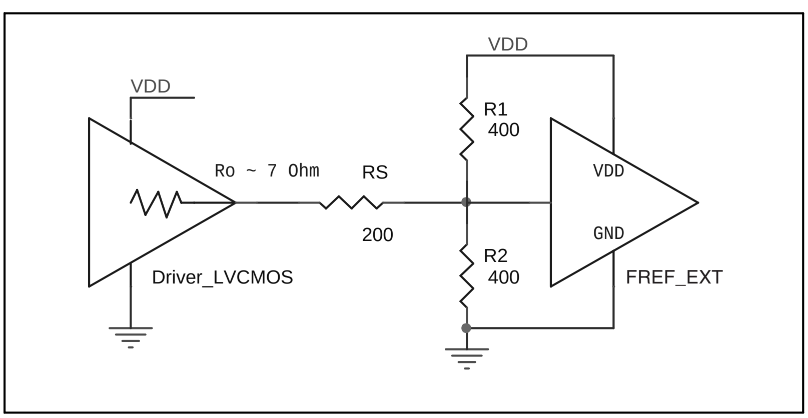


Figure 7C. Edge Rate Reduction by Increasing the Resistor Value

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS84330-02.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS84330-02 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 145mA = **502.4mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 502.4mW + 30mW = **532.4mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A
Tj = Junction Temperature
θ_{JA} = Junction-to-Ambient Thermal Resistance
Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 31.1°C/W per Table 9 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.532W * 31.1°C/W = 86.6°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 9. Thermal Resistance θ_{JA} for 28-pin PLCC, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	37.8°C/W	31.1°C/W	28.3°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in the *Figure 8.*

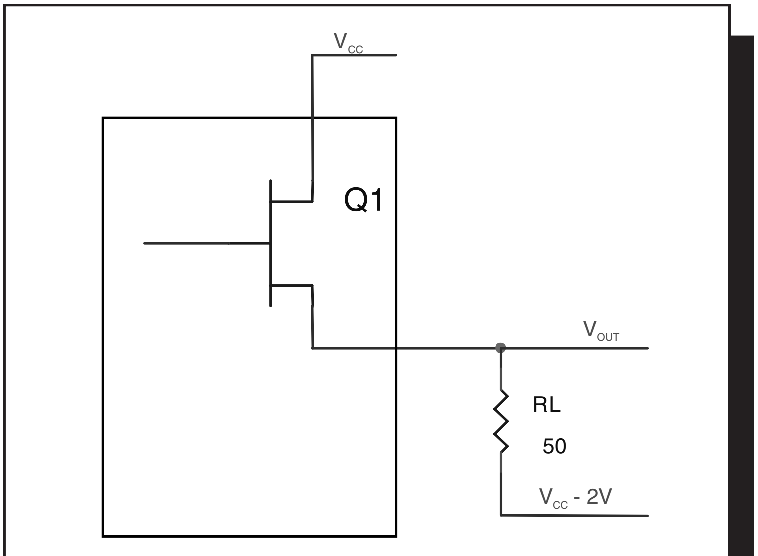


FIGURE 8. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.9V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 10. θ_{JA} vs. Air Flow PLCC Table for 28 Lead PLCC

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	37.8°C/W	31.1°C/W	28.3°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS84330-02 is: 4442

Pin compatible with the MC12430

Package Outline - V Suffix for 28 Lead PLCC

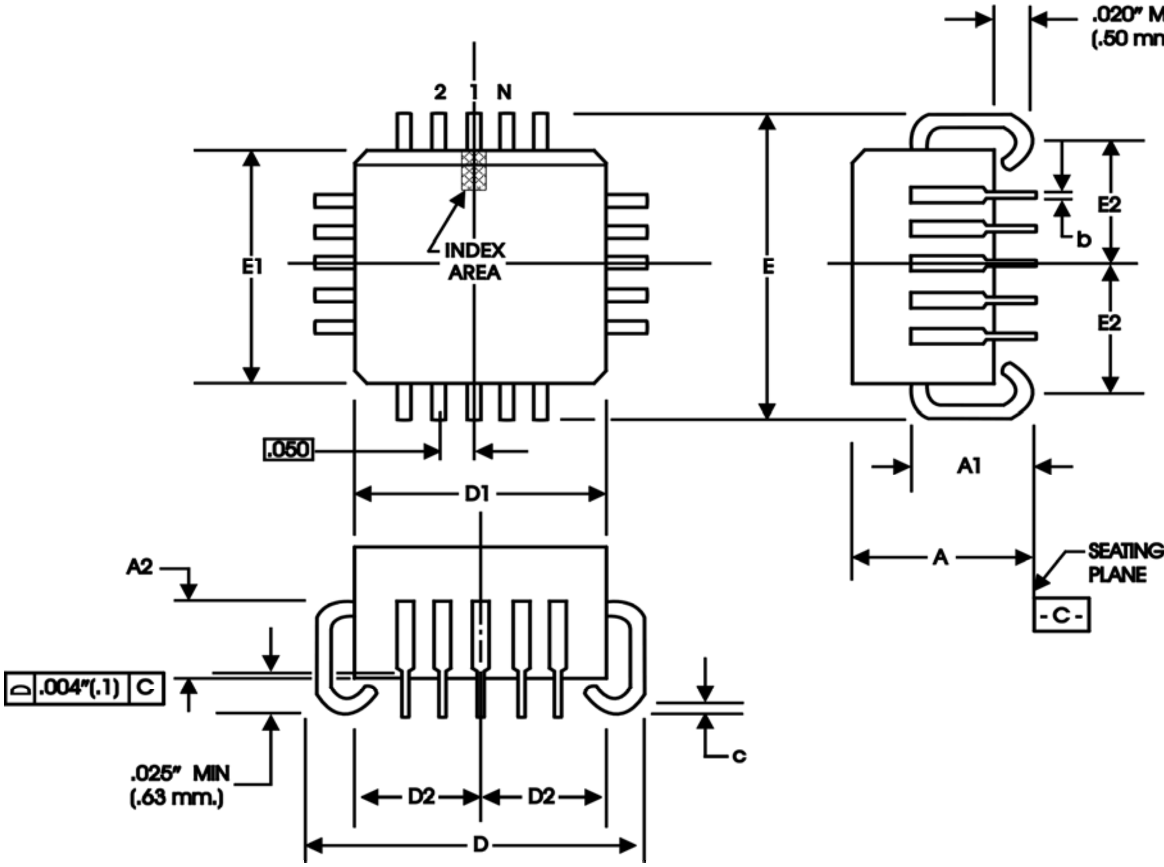


Table 11. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	28	
A	4.19	4.57
A1	2.29	3.05
A2	1.57	2.11
b	0.33	0.53
c	0.19	0.32
D	12.32	12.57
D1	11.43	11.58
D2	4.85	5.56
E	12.32	12.57
E1	11.43	11.58
E2	4.85	5.56

Reference Document: JEDEC Publication 95, MS-018

Table 12. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS84330AV-02	ICS84330AV-02	28 Lead PLCC	tube	0°C to 70°C
ICS84330AV-02T	ICS84330AV-02	28 Lead PLCC	500 tape & reel	0°C to 70°C
ICS84330AV-02LF	ICS84330AV02L	28 Lead "Lead-Free" PLCC	tube	0°C to 70°C
ICS84330AV-02LFT	ICS84330AV02L	28 Lead "Lead-Free" PLCC	500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.