



Integrated
Circuit
Systems, Inc.

PRELIMINARY

ICS843011-01 FEMTOCLOCKS™ CRYSTAL-TO- 3.3V LVPECL CLOCK GENERATOR

GENERAL DESCRIPTION



The ICS843011-01 is a Fibre Channel Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS843011-01 uses a 26.5625MHz crystal to synthesize 106.25MHz or a 25MHz crystal to synthesize 100MHz. The ICS843011-01 has excellent <1ps phase jitter performance, over the 637kHz – 10MHz integration range. The ICS843011-01 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

FEATURES

- 1 differential 3.3V LVPECL output
- Crystal oscillator interface designed for 26.5625MHz, 18pF parallel resonant crystal
- Output frequency: 106.25MHz or 100MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 106.25MHz, using a 26.5625MHz crystal (637kHz - 10MHz): 0.56ps (typical)
- RMS phase noise at 106.25MHz

Phase noise:

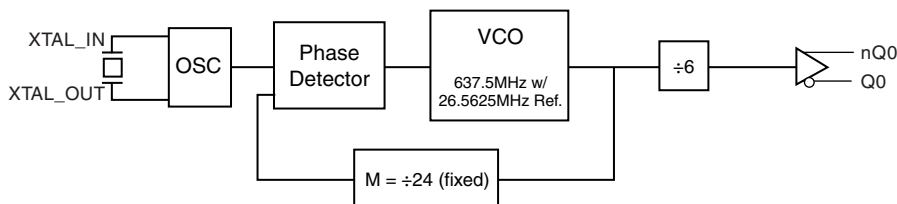
Offset	Noise Power
100Hz	-98 dBc/Hz
1KHz	-122.3 dBc/Hz
10KHz	-135.4 dBc/Hz
100KHz	-135.2 dBc/Hz

- 3.3V operating supply
- 0°C to 70°C ambient operating temperature

FREQUENCY TABLE

Crystal (MHz)	Output Frequency (MHz)
26.5625	106.25
25	100

BLOCK DIAGRAM



PIN ASSIGNMENT

VCCA	1	8	Q0
XTAL_OUT	2	7	nQ0
XTAL_IN	3	6	Vcc
VEE	4	5	nc

ICS843011-01

8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



Integrated
Circuit
Systems, Inc.

PRELIMINARY

ICS843011-01
FEMTOCLOCKS™ CRYSTAL-TO-
3.3V LVPECL CLOCK GENERATOR

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type	Description
1	V _{CCA}	Power	Analog supply pin.
2, 3	XTAL_OUT, XTAL_IN	Input	Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
4	V _{EE}	Power	Negative supply pin.
5	nc	Unused	No connect.
6	V _{CC}	Power	Core supply pin.
7, 8	nQ0, Q0	Output	Differential clock outputs. LVPECL interface levels.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_i	-0.5V to $V_{CC} + 0.5V$
Outputs, I_o	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			55		mA

TABLE 3B. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		23.33		28.33	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

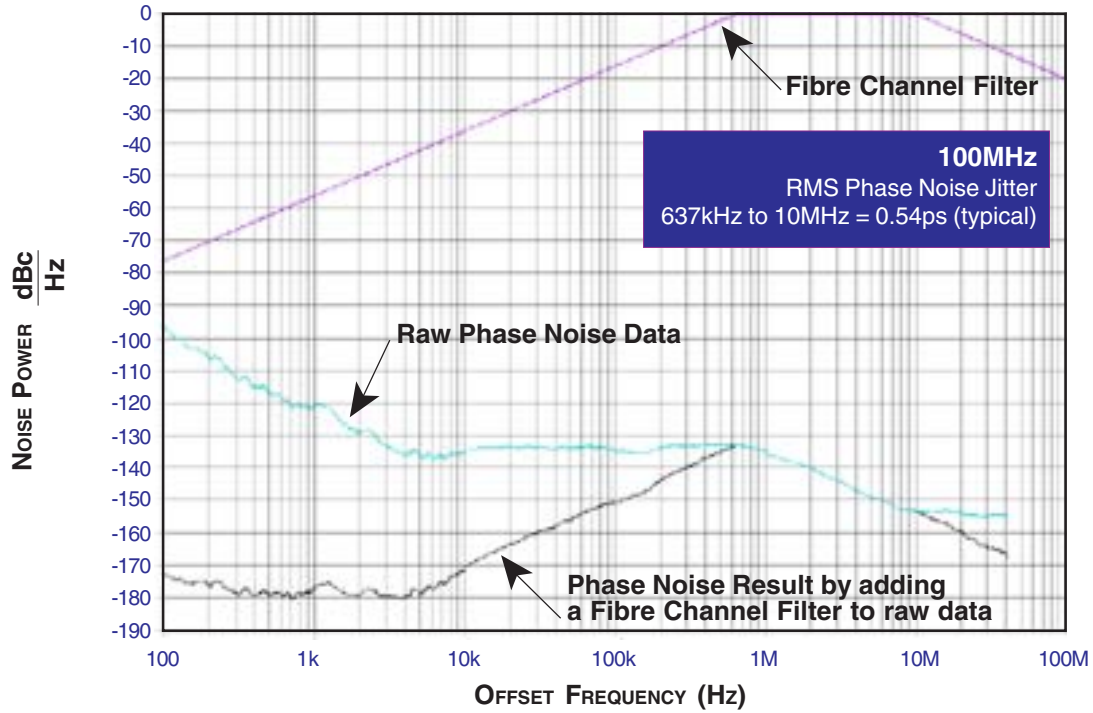
TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		93.33		113.33	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	106.25MHz; Integration Range: 637kHz - 10MHz		0.56		ps
		100MHz; Integration Range: 637kHz - 10MHz		0.54		ps
t_r / t_f	Output Rise/Fall Time	20% to 80%		350		ps
odc	Output Duty Cycle			50		%

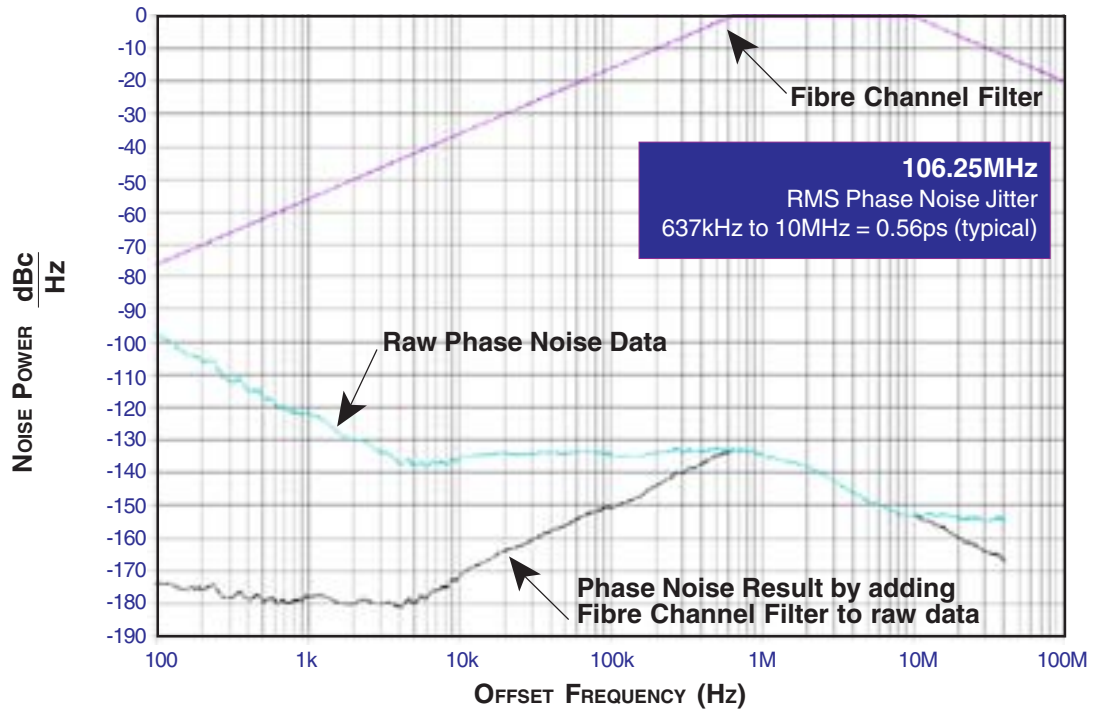
NOTE 1: Please refer to the Phase Noise Plot.



TYPICAL PHASE NOISE AT 100MHz

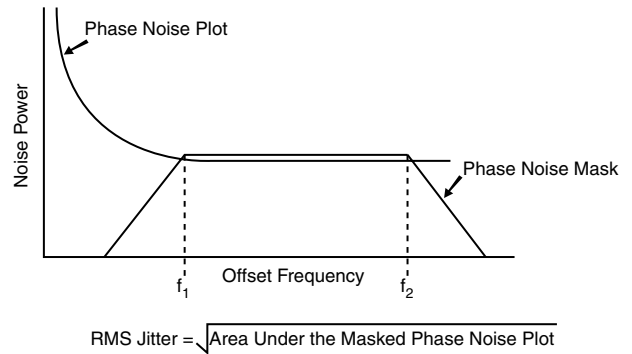
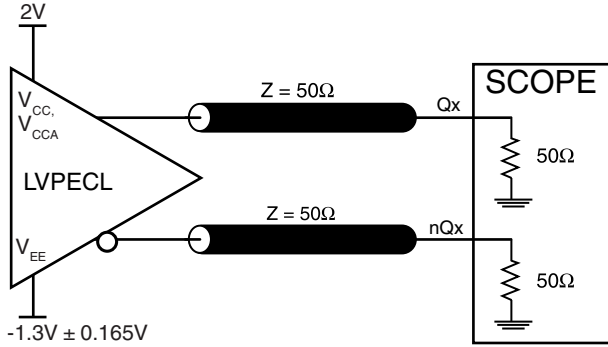


TYPICAL PHASE NOISE AT 106.25MHz



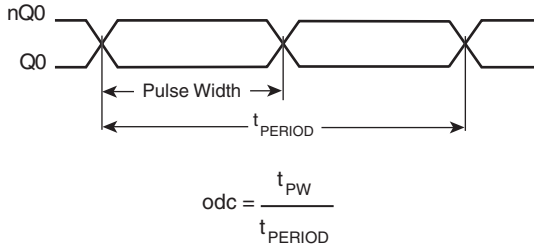


PARAMETER MEASUREMENT INFORMATION



3.3V OUTPUT LOAD AC TEST CIRCUIT

RMS PHASE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

OUTPUT RISE/FALL TIME



APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843011-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} and V_{CCA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu\text{F}$ and a $.01\mu\text{F}$ bypass capacitor should be connected to each V_{CCA} pin.

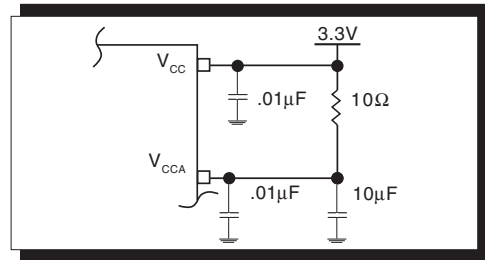


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843011-01 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel

resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

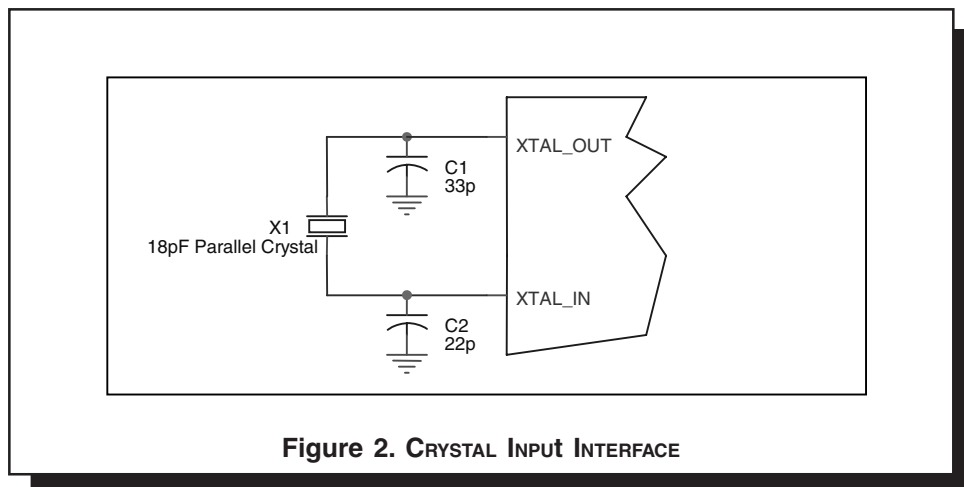


Figure 2. CRYSTAL INPUT INTERFACE



TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to

drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

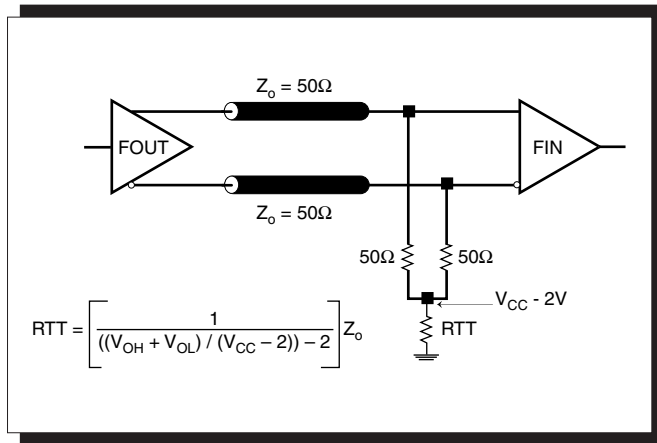


FIGURE 3A. LVPECL OUTPUT TERMINATION

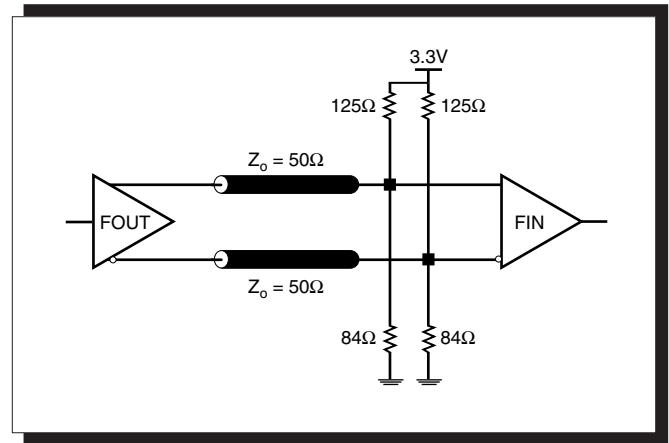


FIGURE 3B. LVPECL OUTPUT TERMINATION



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843011-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843011-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 55mA = 190.57mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 190.6mW + 30mW = \mathbf{220.6mW}$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.221W * 90.5^\circ C/W = 90^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 8-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W



3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 4.

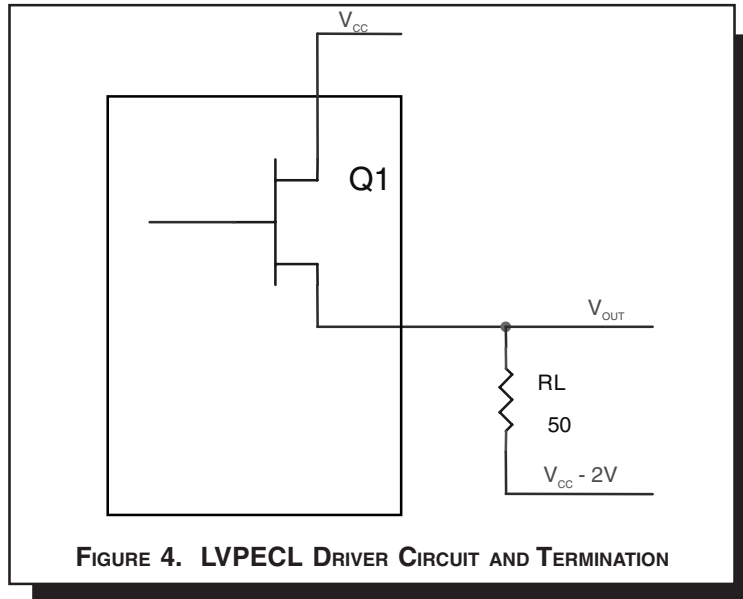


FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.9V$

$$(V_{CC_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$

$$(V_{CC_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = Pd_H + Pd_L = 30mW



Integrated
Circuit
Systems, Inc.

PRELIMINARY

ICS843011-01
FEMTOCLOCKS™ CRYSTAL-TO-
3.3V LVPECL CLOCK GENERATOR

RELIABILITY INFORMATION

TABLE 6. θ_{JA} vs. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for ICS843011-01 is: 1662



PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD TSSOP

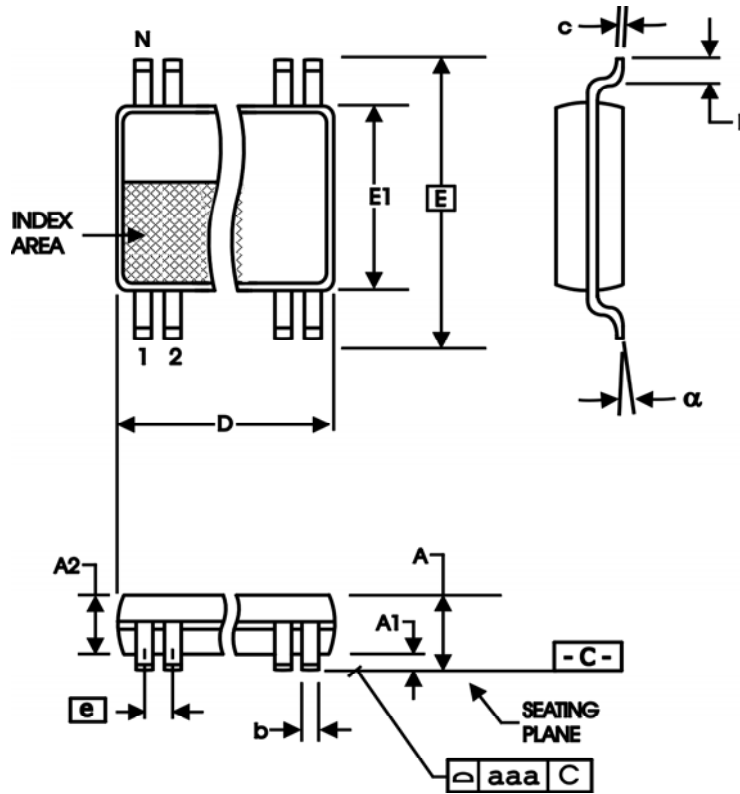


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153



Integrated
Circuit
Systems, Inc.

PRELIMINARY

ICS843011-01
FEMTOCLOCKS™ CRYSTAL-TO-
3.3V LVPECL CLOCK GENERATOR

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843011AM-01	11A01	8 Lead TSSOP	tube	0°C to 70°C
ICS843011AM-01T	11A01	8 Lead TSSOP	2500 tape & reel	0°C to 70°C

The aforementioned trademarks, HiPerClockS™ and FemtoClocks™ are a trademark of Integrated Circuit Systems, Inc. or its subsidiaries in the United States and/or other countries. While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems, Incorporated (ICS) assumes no responsibility for either its use or for infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.