

SCAN182374A

D-Type Flip-Flop with 25Ω Series Resistor Outputs

General Description

The SCAN182374A is a high performance BiCMOS D-type flip-flop featuring separate D-type inputs organized into dual 9-bit bytes with byte-oriented clock and output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

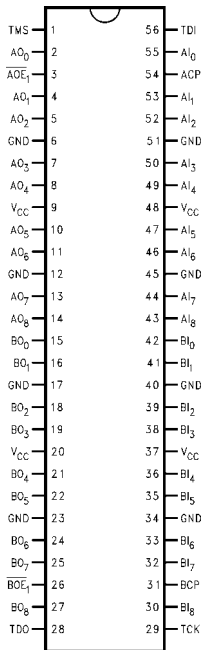
- IEEE 1149.1 (JTAG) Compliant
- High performance BiCMOS technology
- 25Ω series resistor outputs eliminate need for external terminating resistors
- Buffered positive edge-triggered clock
- 3-STATE outputs for bus-oriented applications
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP, IDCODE and HIGHZ instructions
- Additional instructions SAMPLE-IN, SAMPLE-OUT and EXTTEST-OUT
- Power up 3-STATE for hot insert
- Member of Fairchild's SCAN Products

Ordering Code:

Order Number	Package Number	Package Description
SCAN182374ASSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide

Device also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
AI ₍₀₋₈₎ , BI ₍₀₋₈₎	Data Inputs
ACP, BCP	Clock Pulse Inputs
AOE ₁ , BOE ₁	3-STATE Output Enable Inputs
AO ₍₀₋₈₎ , BO ₍₀₋₈₎	3-STATE Outputs

Truth Tables

Inputs			AO ₍₀₋₈₎
ACP	AOE ₁ (Note 1)	AI ₍₀₋₈₎	
X	H	X	Z
↘	L	L	L
↘	L	H	H

Inputs			BO ₍₀₋₈₎
BCP	BOE ₁ (Note 1)	BI ₍₀₋₈₎	
X	H	X	Z
↘	L	L	L
↘	L	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↘ = L-to-H Transition

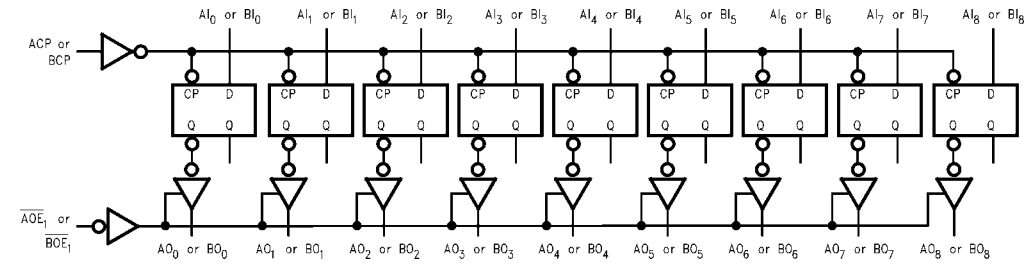
Note 1: Inactive-to-active transition must occur to enable outputs upon power-up.

Functional Description

The SCAN182374A consists of two sets of nine edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable pins are common to all flip-flops. Each set of the nine flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the

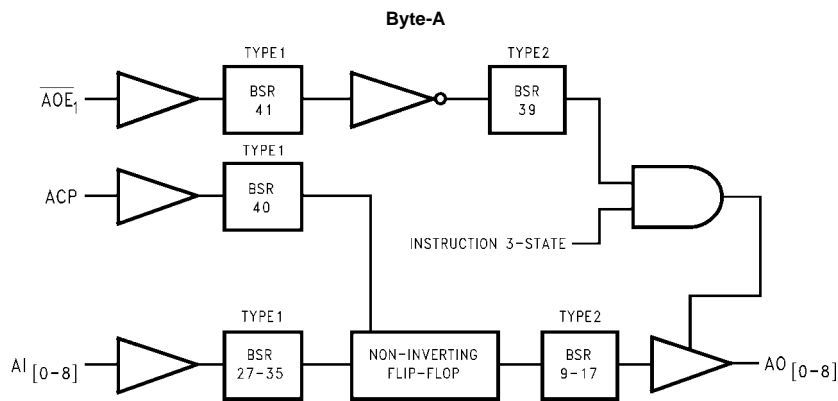
LOW-to-HIGH Clock (ACP or BCP) transition. With the Output Enable ($\overline{AOE_1}$ or $\overline{BOE_1}$) LOW, the contents of the nine flip-flops are available at the outputs. When the Output Enable is HIGH, the outputs go to the high impedance state. Operation of the Output Enable input does not affect the state of the flip-flops.

Logic Diagram

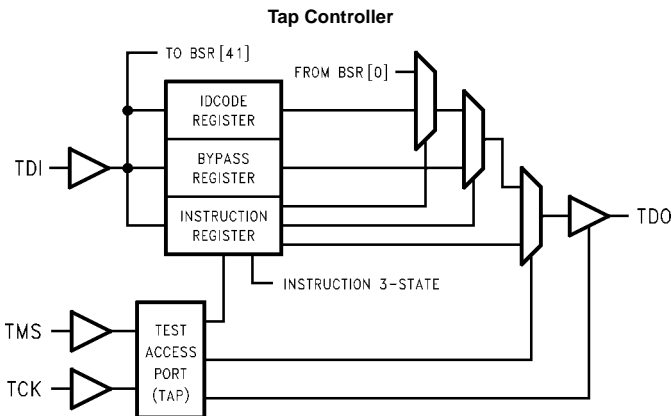


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

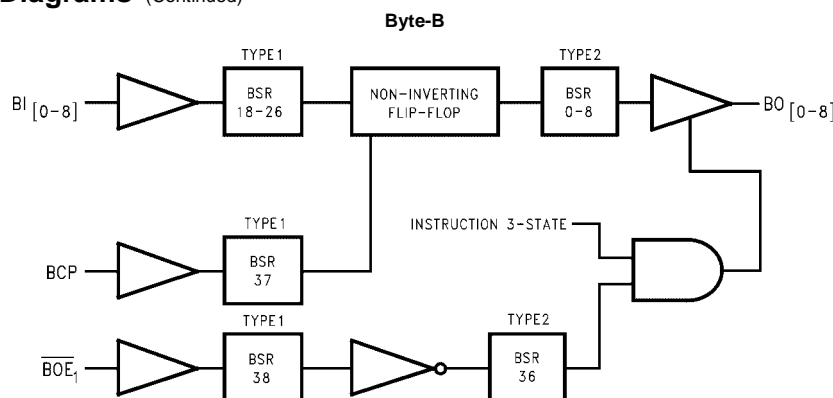
Block Diagrams



Note: BSR stands for Boundary Scan Register



Block Diagrams (Continued)



Note: BSR stands for BOUNDARY-SCAN Register

Description of BOUNDARY-SCAN Circuitry

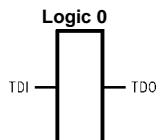
The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data.

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

The INSTRUCTION register is an 8-bit register which captures the default value of 10000001 (SAMPLE/PRELOAD) during the CAPTURE-IR instruction command. The benefit of capturing SAMPLE/PRELOAD as the default instruction during CAPTURE-IR is that the user is no longer required to shift in the 8-bit instruction for SAMPLE/PRELOAD. The sequence of: CAPTURE-IR → EXIT1-IR → UPDATE-IR will update the SAMPLE/PRELOAD instruction. For more information refer to the section on instruction definitions.

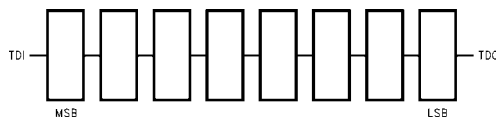
Bypass Register Scan Chain Definition



SCAN182374A Product IDCODE
(32-Bit Code per IEEE 1149.1)

Version	Entity	Per Number	Manufacturer ID	Required by 1149.1
0000	111111	00000001111	000000011111	1
MSB				LSB

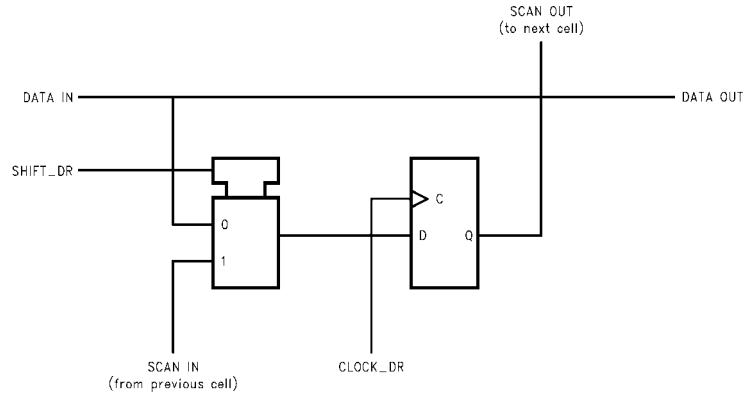
Instruction Register Scan Chain Definition



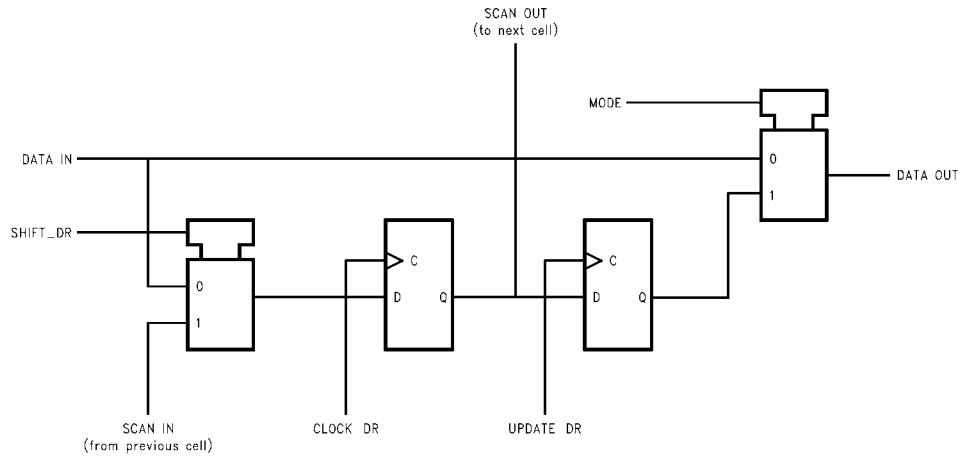
MSB → LSB

Instruction Code	Instruction
00000000	EXTTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
01000001	SAMPLE-IN
01000010	SAMPLE-OUT
00100010	EXTTEST-OUT
10101010	IDCODE
11111111	BYPASS
All Other	BYPASS

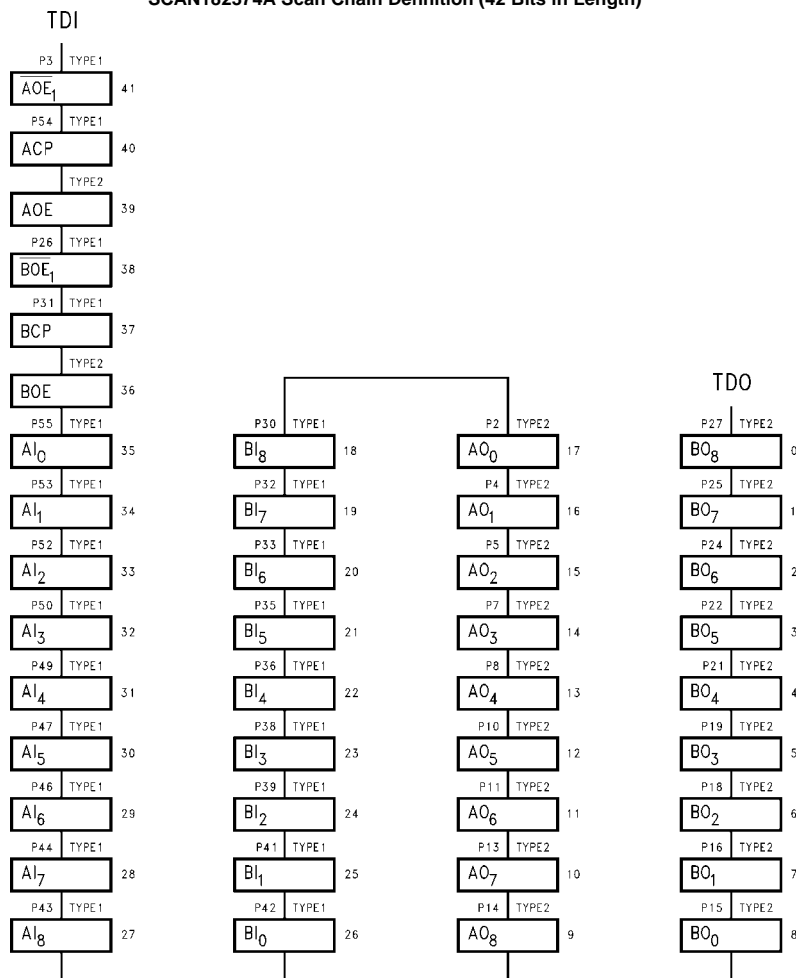
Description of BOUNDARY-SCAN Circuitry (Continued)
Scan Cell TYPE1



Scan Cell TYPE2

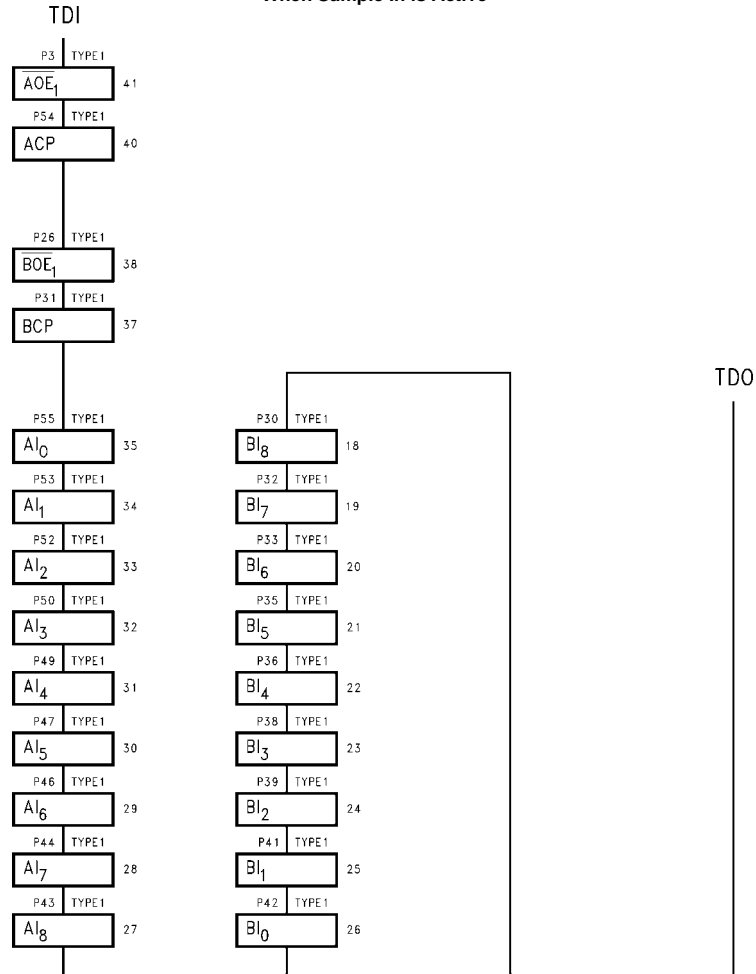


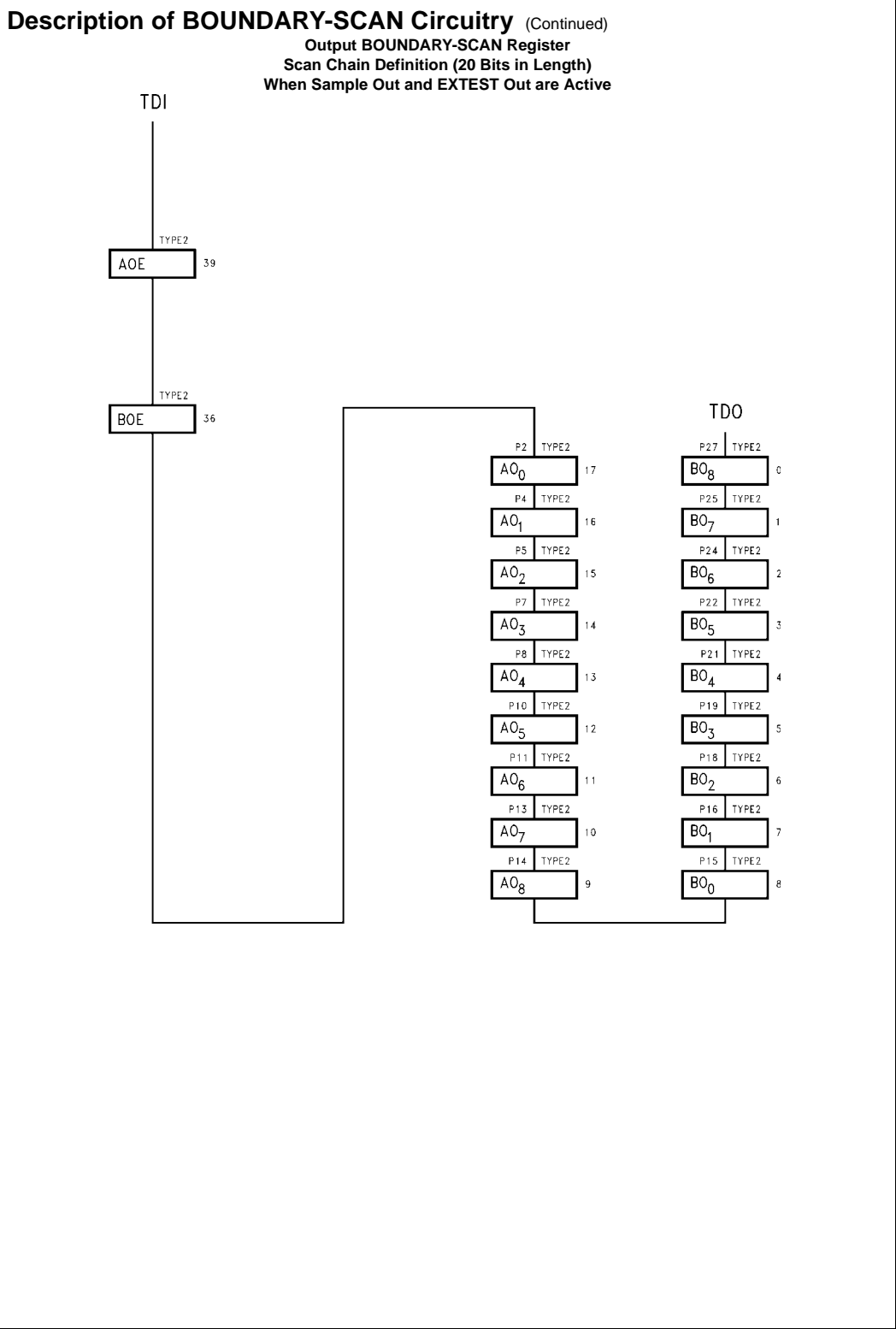
Description of BOUNDARY-SCAN Circuitry (Continued)
BOUNDARY-SCAN Register
SCAN182374A Scan Chain Definition (42 Bits in Length)



Description of BOUNDARY-SCAN Circuitry (Continued)

Input BOUNDARY-SCAN Register
Scan Chain Definition (22 Bits in Length)
When Sample In is Active





Description of BOUNDARY-SCAN Circuitry (Continued)
BOUNDARY-SCAN Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	\overline{AOE}_1	3	Input	TYPE1	Control Signals
40	ACP	54	Input	TYPE1	
39	AOE		Internal	TYPE2	
38	\overline{BOE}_1	26	Input	TYPE1	
37	BCP	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	AI ₀	55	Input	TYPE1	A-in
34	AI ₁	53	Input	TYPE1	
33	AI ₂	52	Input	TYPE1	
32	AI ₃	50	Input	TYPE1	
31	AI ₄	49	Input	TYPE1	
30	AI ₅	47	Input	TYPE1	
29	AI ₆	46	Input	TYPE1	
28	AI ₇	44	Input	TYPE1	
27	AI ₈	43	Input	TYPE1	
26	BI ₀	42	Input	TYPE1	B-in
25	BI ₁	41	Input	TYPE1	
24	BI ₂	39	Input	TYPE1	
23	BI ₃	38	Input	TYPE1	
22	BI ₄	36	Input	TYPE1	
21	BI ₅	35	Input	TYPE1	
20	BI ₆	33	Input	TYPE1	
19	BI ₇	32	Input	TYPE1	
18	BI ₈	30	Input	TYPE1	
17	AO ₀	2	Output	TYPE2	A-out
16	AO ₁	4	Output	TYPE2	
15	AO ₂	5	Output	TYPE2	
14	AO ₃	7	Output	TYPE2	
13	AO ₄	8	Output	TYPE2	
12	AO ₅	10	Output	TYPE2	
11	AO ₆	11	Output	TYPE2	
10	AO ₇	13	Output	TYPE2	
9	AO ₈	14	Output	TYPE2	
8	BO ₀	15	Output	TYPE2	B-out
7	BO ₁	16	Output	TYPE2	
6	BO ₂	18	Output	TYPE2	
5	BO ₃	19	Output	TYPE2	
4	BO ₄	21	Output	TYPE2	
3	BO ₅	22	Output	TYPE2	
2	BO ₆	24	Output	TYPE2	
1	BO ₇	25	Output	TYPE2	
0	BO ₈	27	Output	TYPE2	

Absolute Maximum Ratings ^(Note 2)		Recommended Operating Conditions	
Storage Temperature	-65°C to +150°C	Free Air Ambient Temperature	-40°C to +85°C
Ambient Temperature under Bias	-55°C to +125°C	Supply Voltage	+4.5V to +5.5V
Junction Temperature under Bias	-55°C to +150°C	Minimum Input Edge Rate	($\Delta V/\Delta t$)
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V	Data Input	50 mV/ns
Input Voltage (Note 3)	-0.5V to +7.0V	Enable Input	20 mV/ns
Input Current (Note 3)	-30 mA to +5.0 mA		
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to +5.5V		
Voltage Applied to Any Output in the HIGH State	-0.5V to V _{CC}		
Current Applied to Output in LOW State (Max)	Twice the Rated I _{OL} (mA)		
DC Latchup Source Current	-500 mA		
Over Voltage Latchup (I/O)	10V		
ESD (HBM) Min.	2000V		

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

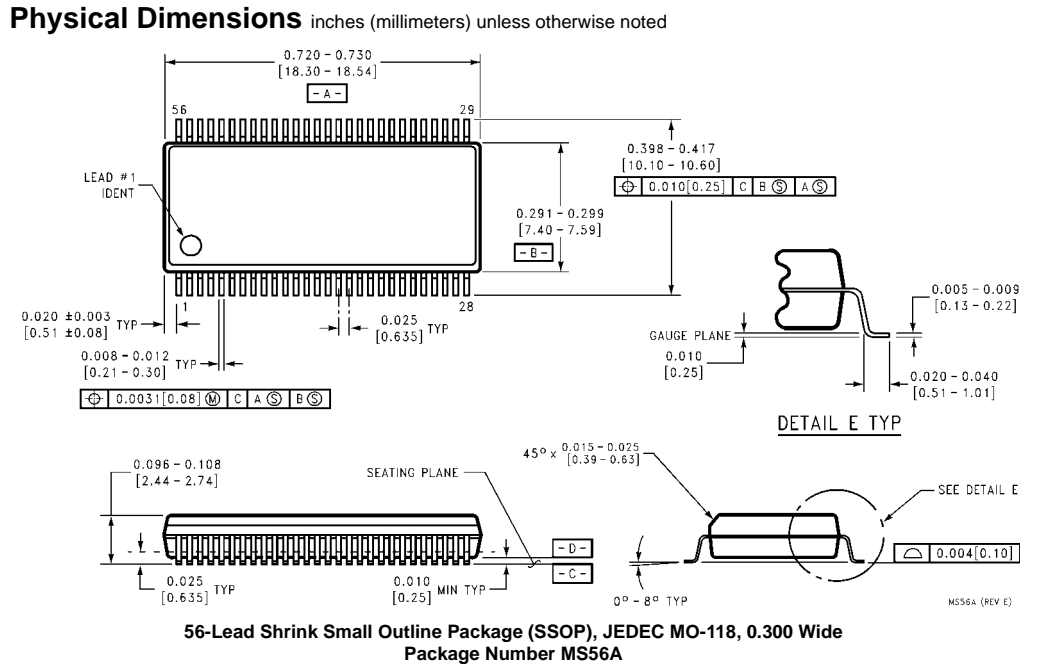
DC Electrical Characteristics

Symbol	Parameter	V _{CC}	Min	Typ	Max	Units	Conditions
V _{IH}	Input HIGH Voltage		2.0			V	Recognized HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V	Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage	Min			-1.2	V	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	Min	2.5			V	I _{OH} = -3 mA
		Min	2.0			V	I _{OH} = -32 mA
V _{OL}	Output LOW Voltage	Min			0.8	V	I _{OL} = 15 mA
I _{IH}	Input HIGH Current	All Others	Max		5	μA	V _{IN} = 2.7V (Note 4)
			Max		5	μA	V _{IN} = V _{CC}
		TMS, TDI Inputs	Max		5	μA	V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test	Max			7	μA	V _{IN} = 7.0V
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)	Max			100	μA	V _{IN} = 5.5V
I _{IL}	Input LOW Current	All Others	Max		-5	μA	V _{IN} = 0.5V (Note 4)
			Max		-5	μA	V _{IN} = 0.0V
		TMS, TDI	Max		-385	μA	V _{IN} = 0.0V
V _{ID}	Input Leakage Test	0.0	4.75			V	I _{ID} = 1.9 μA All Other Pins Grounded
I _{IH} + I _{OZH}	Output Leakage Current	Max			50	μA	V _{OUT} = 2.7V
I _{IL} + I _{OZL}	Output Leakage Current	Max			-50	μA	V _{OUT} = 0.5V
I _{OZH}	Output Leakage Current	Max			50	μA	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current	Max			-50	μA	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current	Max	-100		-275	mA	V _{OUT} = 0.0V
I _{CEx}	Output HIGH Leakage Current	Max			50	μA	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test	0.0			100	μA	V _{OUT} = 5.5V All Others Grounded
I _{CCH}	Power Supply Current	Max			250	μA	V _{OUT} = V _{CC} ; TDI, TMS = V _{CC}
		Max			1.0	mA	V _{OUT} = V _{CC} ; TDI, TMS = GND
I _{CCL}	Power Supply Current	Max			65	mA	V _{OUT} = LOW; TDI, TMS = V _{CC}
		Max			65.8	mA	V _{OUT} = LOW; TDI, TMS = GND
I _{CCZ}	Power Supply Current	Max			250	μA	TDI, TMS = V _{CC}
		Max			1.0	mA	TDI, TMS = GND
I _{CCt}	Additional I _{CC} /Input	All Other Inputs	Max		2.9	mA	V _{IN} = V _{CC} - 2.1V
		TDI, TMS Inputs	Max		3	mA	V _{IN} = V _{CC} - 2.1V
I _{CCD}	Dynamic I _{CC}	No Load	Max		0.2	mA/ MHz	Outputs Open One Bit Toggling, 50% Duty Cycle

Note 4: Guaranteed not tested.

AC Electrical Characteristics						
Normal Operation						
Symbol	Parameter	V _{CC} (V) (Note 5)	T _A = -40°C to +85°C C _L = 50 pF			Units
			Min	Typ	Max	
t _{PLH}	Propagation Delay	5.0	1.4	4.6	6.1	ns
t _{PHL}	CP to Q		2.1	4.9	6.8	
t _{PLZ}	Disable Time	5.0	1.9	4.6	8.0	ns
t _{PHZ}			1.8	4.8	8.7	
t _{PZL}	Enable Time	5.0	2.0	6.7	9.4	ns
t _{PZH}			1.4	6.0	8.2	
Note 5: Voltage Range 5.0V ± 0.5V						
AC Operating Requirements						
Normal Operation						
Symbol	Parameter	V _{CC} (V) (Note 6)	T _A = -40°C to +85°C C _L = 50 pF		Units	
			Guaranteed Minimum			
t _S	Setup Time, H or L Data to CP	5.0	2.8		ns	
t _H	Hold Time, H or L CP to Data	5.0	2.4		ns	
t _W	CP Pulse Width	5.0	0.0		ns	
f _{MAX}	Maximum ACP/BCP Clock Frequency	5.0	50		MHz	
Note 6: Voltage Range is 5.0V ± 0.5V.						
AC Electrical Characteristics						
Scan Test Operation						
Symbol	Parameter	V _{CC} (V) (Note 7)	T _A = -40°C to +85°C C _L = 50 pF			Units
			Min	Typ	Max	
t _{PLH}	Propagation Delay	5.0	2.9	5.8	9.5	ns
t _{PHL}	TCK to TDO		4.0	7.3	11.5	
t _{PLZ}	Disable Time	5.0	1.9	5.6	10.0	ns
t _{PHZ}			TCK to TDO	3.0	7.1	
t _{PZL}	Enable Time	5.0	4.4	8.4	13.2	ns
t _{PZH}			TCK to TDO	2.7	6.4	
t _{PLH}	Propagation Delay	5.0	3.4	6.5	10.5	ns
t _{PHL}			TCK to Data Out during Update-DR State	4.3	8.1	
t _{PLH}	Propagation Delay	5.0	3.9	7.8	12.8	ns
t _{PHL}			TCK to Data Out during Update-IR State	4.7	9.1	
t _{PLH}	Propagation Delay	5.0	4.7	9.5	15.6	ns
t _{PHL}			TCK to Data Out during Test Logic Reset State	5.6	10.9	
t _{PLZ}	Disable Time	5.0	3.2	7.8	13.6	ns
t _{PHZ}			TCK to Data Out during Update-DR State	3.9	8.5	
t _{PLZ}	Disable Time	5.0	3.2	8.6	15.0	ns
t _{PHZ}			TCK to Data Out during Update-IR State	3.8	9.3	
t _{PLZ}	Disable Time	5.0	4.2	10.2	18.0	ns
t _{PHZ}			TCK to Data Out during Test Logic Reset State	5.0	11.0	
t _{PZL}	Enable Time	5.0	5.0	9.6	15.3	ns
t _{PZH}			TCK to Data Out during Update-DR State	3.7	7.7	
t _{PZL}	Enable Time	5.0	5.3	10.8	17.4	ns
t _{PZH}			TCK to Data Out during Update-IR State	4.0	9.0	
t _{PZL}	Enable Time	5.0	6.2	12.6	20.4	ns
t _{PZH}			TCK to Data Out during Test Logic Reset State	4.7	10.7	
Note 7: Voltage Range 5.0V ± 0.5V						

AC Operating Requirements				
Scan Test Operation				
Symbol	Parameter	V _{CC} (V) (Note 8)	T _A = -40°C to +85°C	Units
			C _L = 50 pF Guaranteed Minimum	
t _S	Setup Time Data to TCK (Note 9)	5.0	2.7	ns
t _H	Hold Time Data to TCK (Note 9)	5.0	3.1	ns
t _S	Setup Time, H or L AOE ₁ , BOE ₁ to TCK (Note 10)	5.0	5.0	ns
t _H	Hold Time, H or L TCK to AOE ₁ , BOE ₁ (Note 10)	5.0	1.8	ns
t _S	Setup Time, H or L Internal AOE, BOE to TCK (Note 11)	5.0	3.6	ns
t _H	Hold Time, H or L TCK to Internal AOE, BOE (Note 11)	5.0	2.1	ns
t _S	Setup Time ACP, BCP (Note 12) to TCK	5.0	3.4	ns
t _H	Hold Time TCK to ACP, BCP (Note 12)	5.0	1.8	ns
t _S	Setup Time, H or L TMS to TCK	5.0	8.7	ns
t _H	Hold Time, H or L TCK to TMS	5.0	1.8	ns
t _S	Setup Time, H or L TDI to TCK	5.0	6.4	ns
t _H	Hold Time, H or L TCK to TDI	5.0	3.2	ns
t _W	Pulse Width TCK	H L	8.2 11.2	ns
f _{MAX}	Maximum TCK Clock Frequency	5.0	50	MHz
t _{PU}	Wait Time, Power Up to TCK	5.0	100	ns
t _{DN}	Power Down Delay	0.0	100	ms
<p>Note 8: Voltage Range 5.0V ± 0.5V</p> <p>Note 9: This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0–8, 9–17, 18–26 and 27–35.</p> <p>Note 10: Timing pertains to BSR 38 and 41 only.</p> <p>Note 11: This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.</p> <p>Note 12: Timing pertains to BSR 37 and 40 only.</p> <p>Note: All Input Timing Delays involving TCK are measured from the rising edge of TCK.</p>				
Capacitance				
T _A = 25°C				
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	5.8	pF	V _{CC} = 0.0V
C _{OUT} (Note 13)	Output Capacitance	13.8	pF	V _{CC} = 5.0V
<p>Note 13: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.</p>				



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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