LTC1411

Single Supply 14-Bit 2.5Msps ADC

FEATURES

- **Sample Rate: 2.5Msps**
- **80dB S/(N + D) and 90dB THD at 100kHz f_{IN}**
- **Single 5V Operation**
- **No Pipeline Delay**
- **Programmable Input Ranges**
- Low Power Dissipation: 195mW (Typ)
- True Differential Inputs Reject Common Mode Noise
- Out-of-Range Indicator
- Internal or External Reference
- Sleep (1µA) and Nap (2mA) Shutdown Modes
- 36-Pin SSOP Package

APPLICATIONS

- Telecommunications
- High Speed Data Acquisition
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Spectrum Analysis
- Imaging Systems

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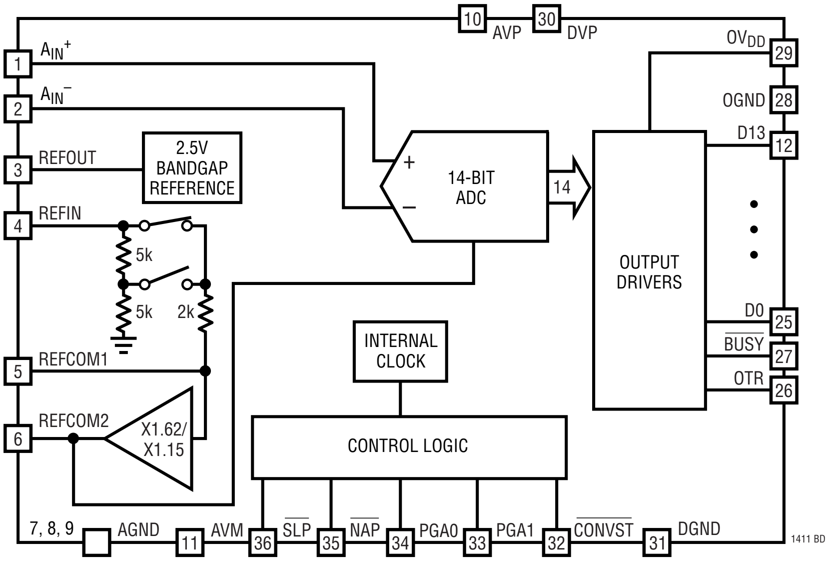
DESCRIPTION

The LTC®1411 is a 2.5Msps sampling 14-bit A/D converter in a 36-pin SSOP package, which typically dissipates only 195mW from a single 5V supply. This device comes complete with a high bandwidth sample-and-hold, a precision reference, programmable input ranges and an internally trimmed clock. The ADC can be powered down with either the Nap or Sleep mode for low power applications.

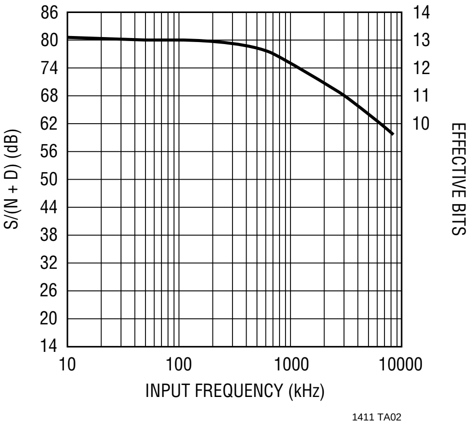
The LTC1411 converts either differential or single-ended inputs and presents data in 2's complement format. Maximum DC specs include ±2LSB INL and 14-bit no missing code over temperature. Outstanding dynamic performance includes 80dB S/(N + D) and 90dB THD at 100kHz input frequency.

The LTC1411 has four programmable input ranges selected by two digital input pins, PGA0 and PGA1. This provides input spans of ±1.8V, ±1.27V, ±0.9V and ±0.64V. An out-of-the-range signal together with the D13 (MSB) will indicate whether a signal is over or under the ADC's input range. A simple conversion start input and a data ready signal ease connections to FIFOs, DSPs and microprocessors.

BLOCK DIAGRAM



S/(N + D) and Effective Bits vs Input Frequency

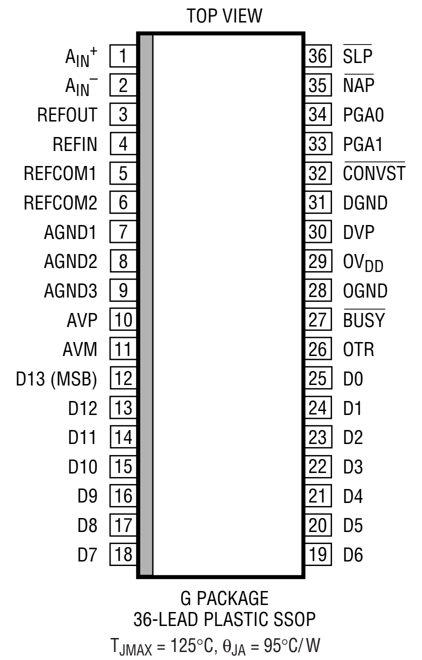


ABSOLUTE MAXIMUM RATINGS

AVP = DVP = OV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Analog Input Voltage (Note 3) ... – 0.3V to (V_{DD} + 0.3V)
Digital Input Voltage (Note 4) .... – 0.3V to 10V
Digital Output Voltage .... – 0.3V to (V_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
LTC1411C .... 0°C to 70°C
LTC1411I .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
36-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1411CG
LTC1411IG

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Notes 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	14			Bits
Integral Linearity Error	(Note 7)	●			±2	LSB
Offset Error	(Note 8)	 ●			±16 ±24	LSB LSB
Full-Scale Error	External Reference = 2.5V				±60	LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0			±15		ppm/°C

DYNAMIC ACCURACY T_A = 25°C (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal 500kHz Input Signal		80.0 77.5		dB dB
THD	Total Harmonic Distortion	100kHz Input Signal, Up to 5th Harmonic 500kHz Input Signal, Up to 5th Harmonic		–90 –82		dB dB
	Peak Harmonic or Spurious Noise	100kHz Input Signal 500kHz Input Signal		90 82		dB dB
	Full Linear Bandwidth	S/(N + D) ≥ 74dB		1.0		MHz
	Transition Noise			0.66		LSB_{RMS}

ANALOG INPUT $T_A = 25°C$ (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	$(A_{IN}^+) - (A_{IN}^-)$, PGA0 = PGA1 = 5V		±1.8		V
		$(A_{IN}^+) - (A_{IN}^-)$, PGA0 = 5V, PGA1 = 0V		±1.27		V
		$(A_{IN}^+) - (A_{IN}^-)$, PGA0 = 0V, PGA1 = 5V		±0.9		V
		$(A_{IN}^+) - (A_{IN}^-)$, PGA0 = PGA1 = 0V		±0.64		V
	Common Mode Input Range	A_{IN}^+ or A_{IN}^-	0		V_{DD}	V
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode)		10		pF
		During Conversions (Hold Mode)		4		pF
t_{ACQ}	Sample-and-Hold Acquisition Time			100		ns
t_{AP}	Sample-and-Hold Aperture Delay Time			7		ns
t_{jitter}	Sample-and-Hold Aperture Delay Time Jitter			1		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	$0V < (A_{IN}^- = A_{IN}^+) < V_{DD}$		62		dB
	Input Leakage Current (Pins 1, 2)			0.1		µA

INTERNAL REFERENCE CHARACTERISTICS $T_A = 25°C$ (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	$I_{OUT} = 0$	2.480	2.500	2.520	V
V_{REF} Output Tempco	$I_{OUT} = 0$		±15		ppm/°C
V_{REF} Line Regulation	$4.75V \le V_{DD} \le 5.25V$		0.01		LSB/V
V_{REF} Load Regulation	$0 \le \lvert I_{OUT} \rvert \le 1mA$		2		LSB/mA
REFCOM2 Output Voltage	$I_{OUT} = 0$, PGA0 = PGA1 = 5V		4.05		V
REFIN Input Current	REFIN = External Reference 2.5V		250		µA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25°C$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	$V_{DD} = 5.25V$	●	2.4			V
V_{IL}	Low Level Input Voltage	$V_{DD} = 4.75V$	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}, Except $\overline{SLP}$, $\overline{NAP}$ (Note 11)	●			±10	µA
C_{IN}	Digital Input Capacitance				2		pF
V_{OH}	High Level Output Voltage	$V_{DD} = 4.75V$, $I_O = -10µA$			4.75		V
		$V_{DD} = 4.75V$, $I_O = -200µA$	●	4.0			V
V_{OL}	Low Level Output Voltage	$V_{DD} = 4.75V$, $I_O = 160µA$			0.05		V
		$V_{DD} = 4.75V$, $I_O = 1.6mA$	●		0.10	0.4	V
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$			–10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{DD}$			10		mA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25°C$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage	(Note 9)		4.75		5.25	V
I_{DD}	Supply Current		●		39	65	mA
	Nap Mode	$\overline{NAP}$ = 0V (Note 11)			2		mA
	Sleep Mode	$\overline{SLP}$ = 0V			1		µA
P_D	Power Dissipation		●		195	325	mW
	Nap Mode	$\overline{NAP}$ = 0V			10		mW
	Sleep Mode	$\overline{SLP}$ = 0V			5		µW

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Notes 5) (See Figures 11a, 11b)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency	(Note 9)	●	2.5			MHz
t_{CONV}	Conversion Time		●		250	350	ns
t_{ACQ}	Acquisition Time				100		ns
t_0	$\overline{\text{SLP}}$↑ to $\overline{\text{CONVST}}$↓ Wake-Up Time	10µF Bypass Capacitor at REFCOM2 Pin			210		ms
t_1	$\overline{\text{NAP}}$↑ to $\overline{\text{CONVST}}$↓ Wake-Up Time				250		ns
t_2	$\overline{\text{CONVST}}$ Low Time	(Note 10)	●	20			ns
t_3	$\overline{\text{CONVST}}$ to $\overline{\text{BUSY}}$ Delay	C_L = 25pF			12		ns
t_4	Data Ready After $\overline{\text{BUSY}}$↑				7		ns
t_5	$\overline{\text{CONVST}}$ High Time	(Note 10)	●	20			ns
t_6	Aperture Delay of Sample-and-Hold				7		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, OGND, AVM and AGND wired together unless otherwise noted.

Note 3: When these pin voltages are taken below AGND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA without latchup.

Note 4: When these pin voltages are taken below AGND, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below AGND without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, PGA1 = PGA0 = 5V, f_{SAMPLE} = 2.5MHz at 25°C and $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended A_{IN}^+ input with A_{IN}^- tied to an external 2.5V reference voltage.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

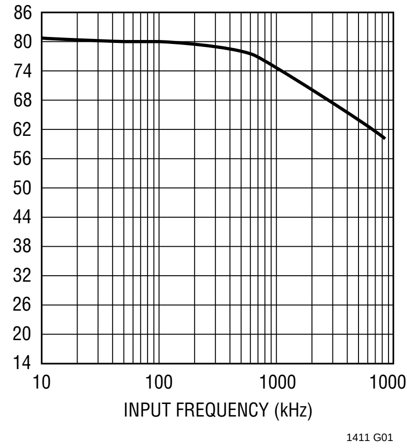
Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11.

Note 9: Recommended operating conditions.

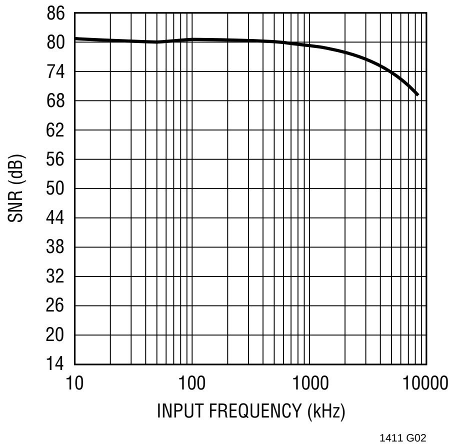
Note 10: The falling $\overline{\text{CONVST}}$ edge starts a conversion. If $\overline{\text{CONVST}}$ returns high at a critical point during the conversion it can create small errors. For best performance ensure that $\overline{\text{CONVST}}$ returns high within 20ns after conversion start of after $\overline{\text{BUSY}}$ rises.

Note 11: $\overline{\text{SLP}}$ and $\overline{\text{NAP}}$ have an internal pull-down so the pins will draw approximately 7µA when tied high and less than 1µA when tied low.

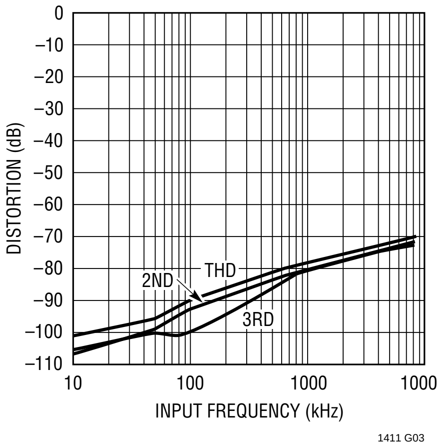
TYPICAL PERFORMANCE CHARACTERISTICS



S/(N + D) vs Input Frequency

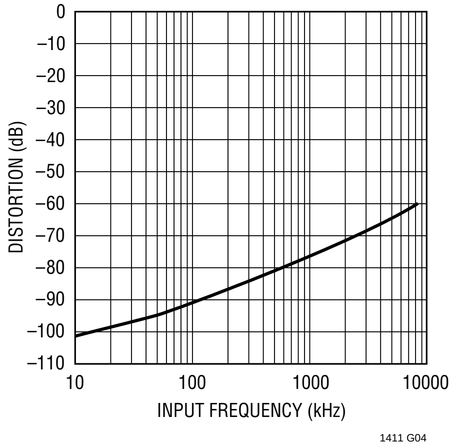


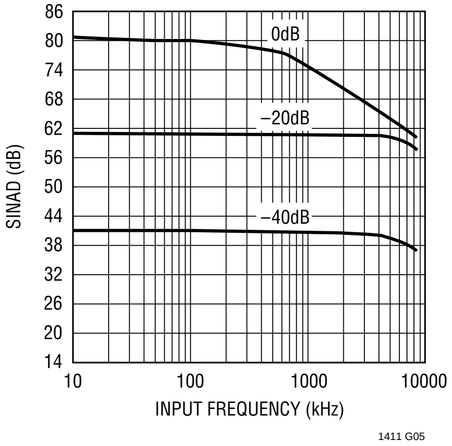
Signal-to-Noise Ratio vs Input Frequency

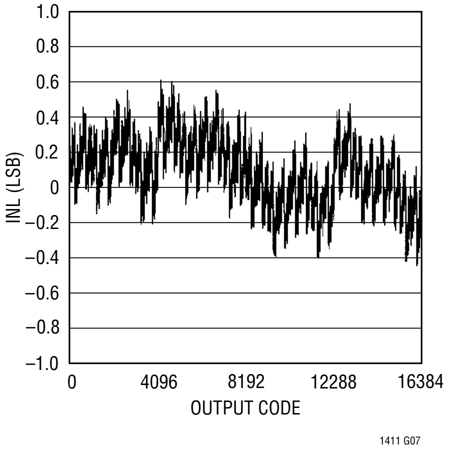


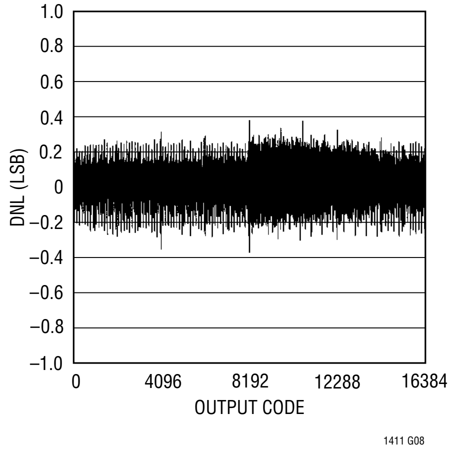
Distortion vs Input Frequency

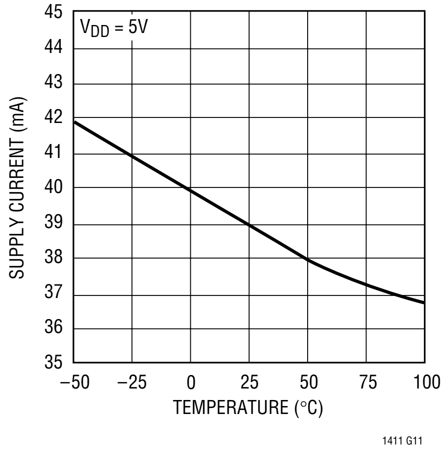
TYPICAL PERFORMANCE CHARACTERISTICS

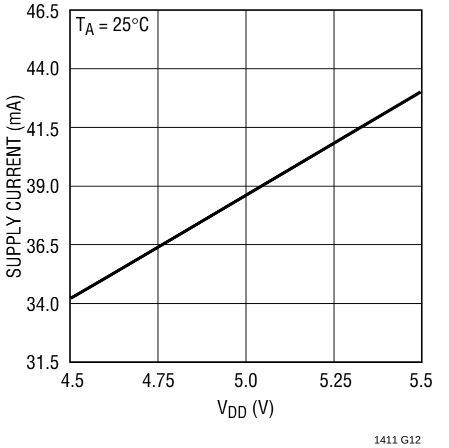

Spurious Free Dynamic Range vs Input Frequency

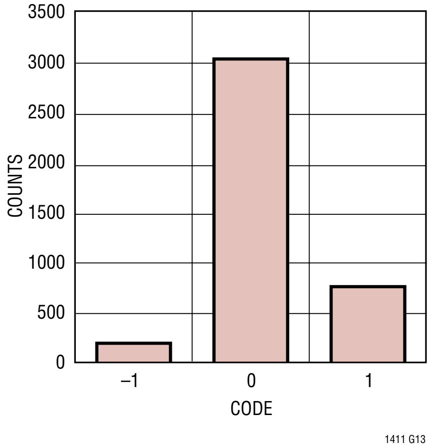

S/(N + D) vs Input Frequency and Amplitude

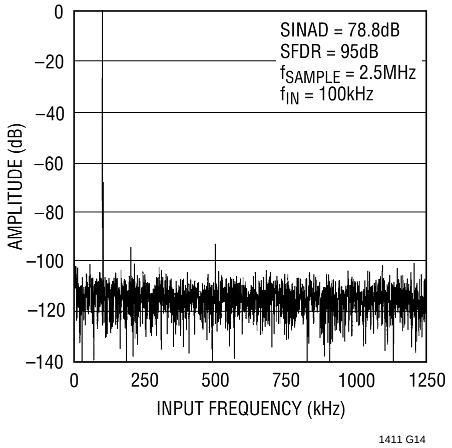

Integral Nonlinearity vs Output Code


Differential Nonlinearity vs Output Code

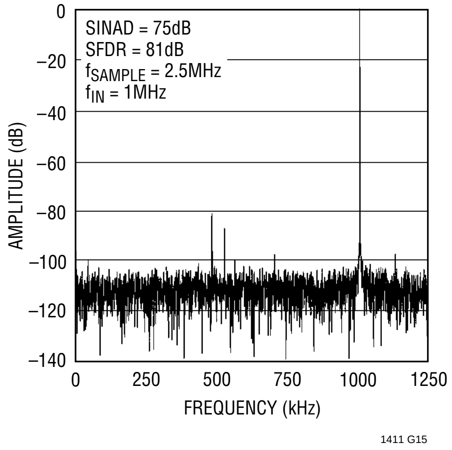

Supply Current vs Temperature


Supply Current vs Supply Voltage

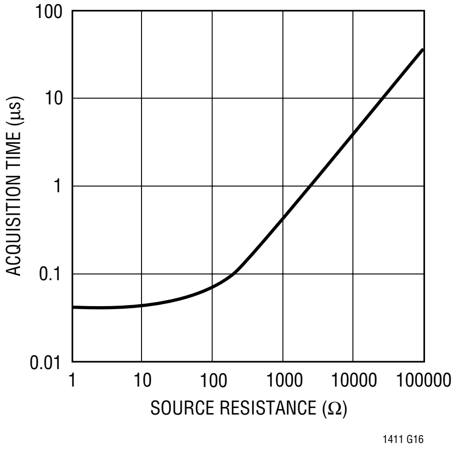

Histogram for 4096 Conversions


4096 Points FFT Plot (100kHz)

TYPICAL PERFORMANCE CHARACTERISTICS



4096 Points FFT Plot (1MHz)



Acquisition Time vs Source Resistance

PIN FUNCTIONS

A_{IN}^+ (Pin 1): Positive Analog Input. The ADC converts the difference voltage between A_{IN}^+ and A_{IN}^- with programmable input ranges of ±1.8V, ±1.27V, ±0.9V and ±0.64V depending on PGA selection. A_{IN}^+ has common mode range between 0V and V_{DD}.

A_{IN}^- (Pin 2): Negative Analog Input. This pin can be tied to the REFOUT pin of the ADC or tied to an external DC voltage. This voltage is also the bipolar zero for the ADC. A_{IN}^- has common mode range between 0V and V_{DD}.

REFOUT (Pin 3): 2.5V Reference Output. Bypass to AGND1 with a 22μF tantalum capacitor if REFOUT is tied to A_{IN}^-. No capacitor is needed if the external reference is used to drive A_{IN}^-.

REFIN (Pin 4): Reference Buffer Input. This pin can be tied to REFOUT or to an external reference if more precision is required.

REFCOM1 (Pin 5): Noise Reduction Pin. Put a 10μF bypass capacitor at this pin to reduce the noise going into the reference buffer.

REFCOM2 (Pin 6): 4.05V Reference Compensation Pin. Bypass to AGND1 with a 10μF tantalum capacitor in parallel with a 0.1μF ceramic.

AGND (Pins 7 to 9): Analog Ground. AGND1 is the ground for the reference. AGND2 is the ground for the comparator and AGND3 is the ground for the remaining analog circuitry.

AVP (Pin 10): 5V Analog Power Supply. Bypass to AGND with a 10μF tantalum capacitor.

AVM (Pin 11): Analog and Digital Substrate Pin. Tie this pin to AGND.

D13 to D0 (Pins 12 to 25): Digital Data Outputs. D13 is the MSB (Most Significant Bit).

OTR (Pin 26): Out-of-the-Range Pin. This pin can be used in conjunction with D13 to determine if a signal is less than or greater than the analog input range. If D13 is low and OTR is high, the analog input to the ADC exceeds the maximum voltage of the input range.

$\overline{\text{BUSY}}$ (Pin 27): Busy Output. Converter status pin. It is low during conversion.

OGND (Pin 28): Digital Ground for Output Drivers (Data Bits, OTR and $\overline{\text{BUSY}}$).

OV_{DD} (Pin 29): 3V or 5V Digital Power Supply for Output Drivers (Data Bits, OTR and $\overline{\text{BUSY}}$). Bypass to OGND with a 10μF tantalum capacitor.

PIN FUNCTIONS

DVP (Pin 30): 5V Digital Power Supply Pin. Bypass to OGND with a 10µF tantalum capacitor.

DGND (Pin 31): Digital Ground.

$\overline{\text{CONVST}}$ (Pin 32): Conversion Start Signal. This active low signal starts a conversion on its falling edge.

PGA1, PGA0 (Pins 33, 34): Logic Inputs for Programmable Input Range. This ADC has four input ranges (or four REFCOM2 voltages) controlled by these two pins. For the logic inputs applied to PGA0 and PGA1, the following summarizes the gain levels and the analog input range with A_{IN}^- tied to 2.5V.

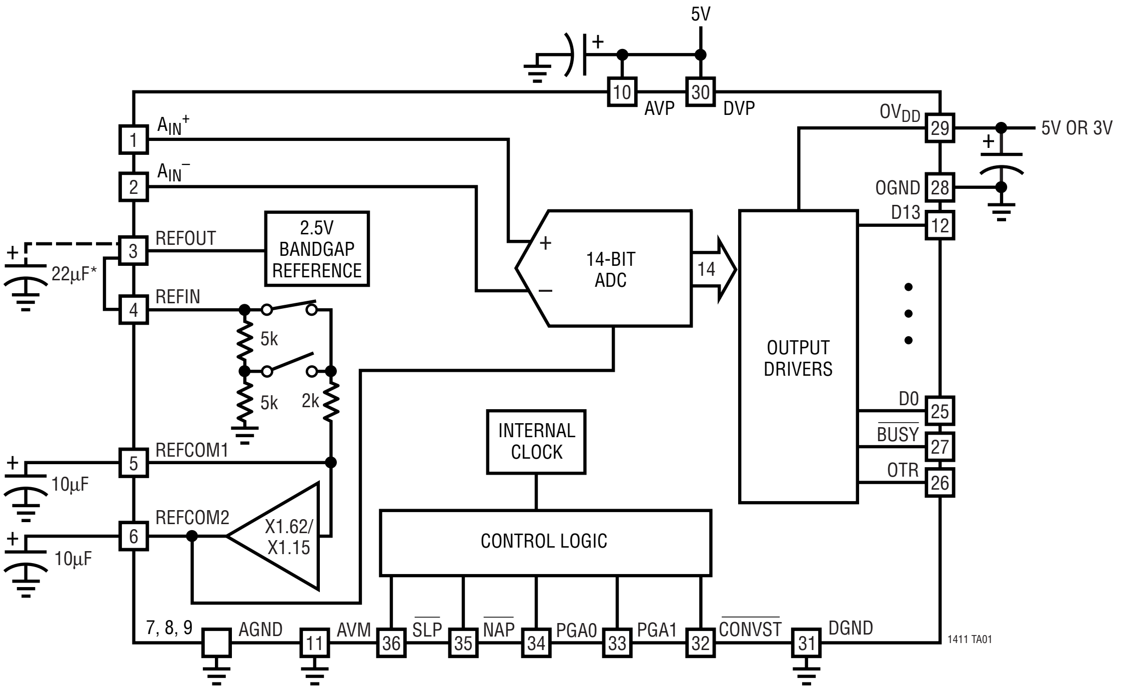
Table 1. Input Spans for LTC1411

PGA0	PGA1	LEVEL	INPUT SPAN	REFCOM2 VOLTAGE
5V	5V	0dB	±1.8V	4V
5V	0V	–3dB	±1.28V	2.9V
0V	5V	–6dB	±0.9V	2V
0V	0V	–9dB	±0.64V	1.45V

$\overline{\text{NAP}}$ (Pin 35): Nap Input. Driving this pin low will put the ADC in the Nap mode and will reduce the supply current to 2mA and the internal reference will remain active.

$\overline{\text{SLP}}$ (Pin 36): Sleep Input. Driving this pin low will put the ADC in the Sleep mode and the ADC draws less than 1µA of supply current.

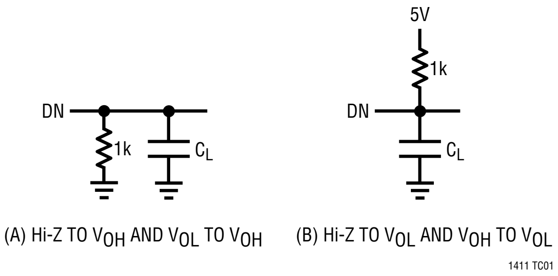
TYPICAL CONNECTION DIAGRAM



*A 22µF CAPACITOR IS NEEDED IF REFOUT IS USED TO DRIVE A_{IN}^-

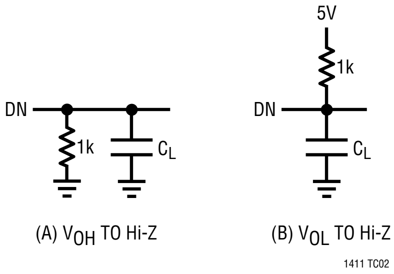
TEST CIRCUITS

Load Circuits for Access Timing



(A) Hi-Z TO V_{OH} AND V_{OL} TO V_{OH} (B) Hi-Z TO V_{OL} AND V_{OH} TO V_{OL}

Load Circuits for Output Float Delay



(A) V_{OH} TO Hi-Z (B) V_{OL} TO Hi-Z

APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1411 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 14-bit parallel output. The ADC is complete with a precision reference, internal clock and a programmable input range. The device is easy to interface with microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversions are started by a falling edge on the $\overline{\text{CONVST}}$ input. Once a conversion cycle has begun, it cannot be restarted. Between conversions, the ADC acquires the analog input in preparation for the next conversion. In the acquire phase, a minimum time of 100ns will provide enough time for the sample-and-hold capacitors to acquire the analog signal.

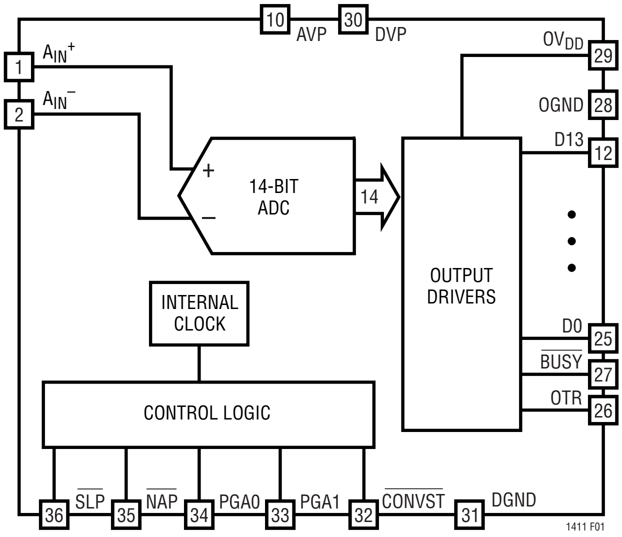


Figure 1. Simplified Block Diagram

During the conversion, the internal differential 14-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). The input is successively compared with the binary weighted charges supplied by the differential capacitive DAC. Bit decisions are made by a high speed comparator. At the end of a conversion, the DAC output balances the analog input ($A_{IN}^+ - A_{IN}^-$). The SAR contents (a 14-bit data word) which represents the difference of A_{IN}^+ and A_{IN}^- are loaded into the 14-bit output latches.

DYNAMIC PERFORMANCE

The LTC1411 has excellent high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2a shows a typical LTC1411 FFT plot.

Signal-to-Noise

The signal-to-(noise + distortion) ratio [S/N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from the above DC and below half the sampling frequency. Figure 2a shows a typical spectral content with a 2.5MHz sampling rate and a 100kHz input. The dynamic performance holds well to higher input frequencies (see Figure 2b).

APPLICATIONS INFORMATION

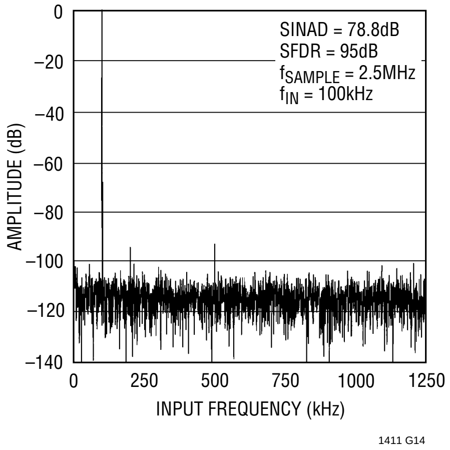


Figure 2a. LTC1411 Nonaveraged, 4096 Point FFT, Input Frequency = 100kHz

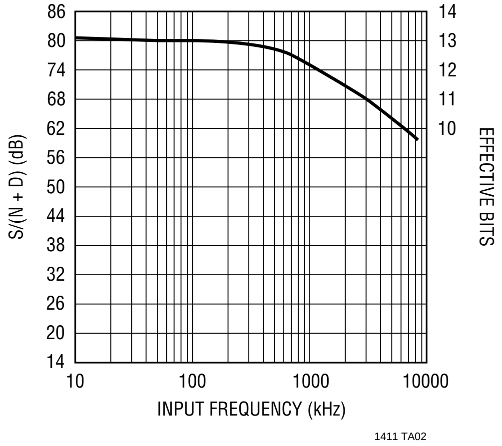


Figure 3. Effective Bits and Signal/(Noise + Distortion) vs Input Frequency

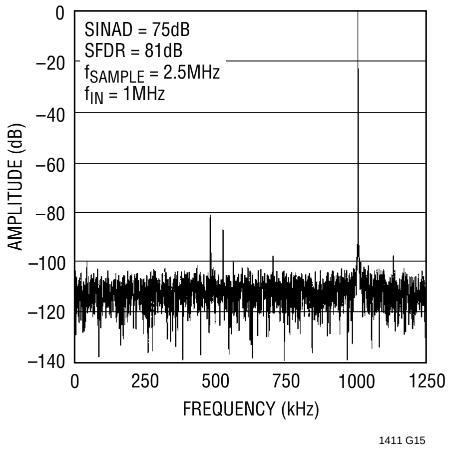


Figure 2b. LTC1411 4096 Point FFT, Input Frequency = 1MHz

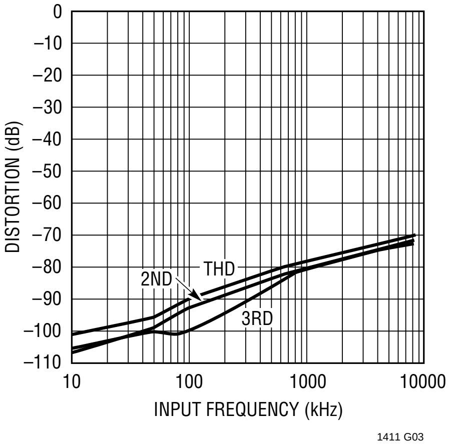


Figure 4. Distortion vs Input Frequency

Effective Number of Bits

The effective number of bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$ENOB_S = [S/(N + D) – 1.76]/6.02$$

where S/(N + D) is expressed in dB. At the maximum sampling rate of 2.5MHz the LTC1411 maintains good ENOBs up to the Nyquist input frequency of 1.25MHz. Refer to Figure 3.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics. THD vs input frequency is shown in Figure 4. The LTC1411 has good distortion performance up to the Nyquist frequency and beyond.

APPLICATIONS INFORMATION

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in dB relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3db for a full-scale input signal.

The full-linear bandwidth is the input frequency at which the S/(N + D) has dropped to 74dB (12 effective bits). The LTC1411 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Driving the Analog Input

The differential analog inputs of the LTC1411 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the A_{IN}^- input is tied to a fixed DC voltage such as the REFOUT pin of the LTC1411 or an external source). Figure 1 shows a simplified block diagram for the analog inputs of the LTC1411. The A_{IN}^+ and A_{IN}^- are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion, the analog inputs draw only a small leakage current. If the source impedance of the driving circuits is low, then the LTC1411 inputs can be driven directly. More acquisition time should be allowed for a higher impedance source. Figure 5 shows the acquisition time versus source resistance.

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 40MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions.

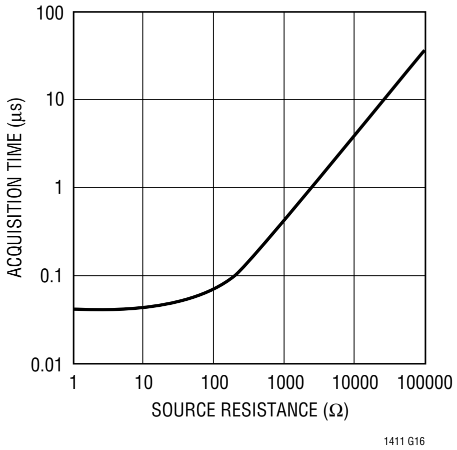


Figure 5. Acquisition Time vs Source Resistance

The best choice for an op amp to drive the LTC1411 will depend on the application. Generally applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC1411. More detailed information is available in the Linear Technology Databooks and on the LinearView™ CD-ROM.

LT®1227: 140MHz Video Current Feedback Amplifier. 10mA supply current. ±5V to ±15V supplies. Low noise. Good for AC applications.

LT1395: 400MHz Current Feedback Amplifier. Single 5V or ±5V supplies. Good for AC applications.

LT1800: 80MHz, 25V/µs Low Power Rail-to-Rail Input and Output Precision Op Amp. Specified at 3V, 5V and ±5V supplies. Excellent DC performance.

APPLICATIONS INFORMATION

LT6203: Dual 100MHz, Low Noise, Low Power Op Amp. Specified at 3V, 5V and ±5V supplies. 1.9nV/$\sqrt{Hz}$ noise voltage.

Programmable Input Range

The LTC1411 has two logic input pins (PGA0 and PGA1) that are used to select one of four analog input ranges. These input ranges are set by changing the reference voltage that is applied to the internal DAC of the ADC (REFCOM2). For the "0dB" setting the internal DAC sees the full reference voltage of 4V. The analog input range is 0.7V to 4.3V with A_{IN}^- = 2.5V. This corresponds to an input span of ±1.8V with respect to the voltage applied to A_{IN}^-. For the "–3dB" setting the internal reference is reduced to 0.707 • 4V = 2.9V. Likewise the input span is reduced to ±1.28V. The following table lists the input span with respect to A_{IN}^- for the different PGA0 and PGA1 settings.

Table 1. Input Spans for LTC1411

PGA0	PGA1	LEVEL	INPUT SPAN	REFCOM2 VOLTAGE
5V	5V	0dB	±1.8V	4V
5V	0V	–3dB	±1.28V	2.9V
0V	5V	–6dB	±0.9V	2V
0V	0V	–9dB	±0.64V	1.45V

When changing from one input span to another, more time is needed for the REFCOM2 pin to reach the correct level because the bypass capacitor on the pin needs to be charged or discharged. Figure 6 shows the recommended capacitors at the REFCOM1 and REFCOM2 pins (10µF each).

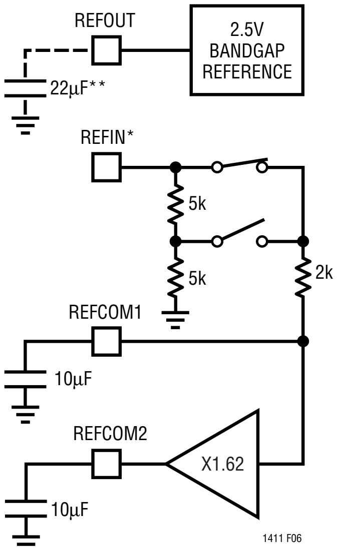
When –6dB or –9dB is selected, the voltage at REFCOM1 (see Figure 2) must first settle before REFCOM2 reaches the correct level. The typical delay is about 700ms.

When the REFCOM2 level is changed from 2.9V to 4V (changing PGA setting from –3dB to 0dB), the typical delay is 0.6ms. However, if the voltage at REFCOM2 is changed from 4V to 2.9V (changing PGA setting from 0dB to –3dB) only a 60µA sink current is present to discharge the 10µF bypass capacitor. In this case, the delay will be 11ms.

Internal Reference

The LTC1411 has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.500V. If this REFOUT pin is used to drive the A_{IN}^- pin, a 22µF tantalum bypass capacitor is required and this REFOUT voltage sets the bipolar zero for the ADC.

The REFIN pin is connected to the reference buffer through a 2k resistor and two PGA switches. The REFIN pin can be connected to REFOUT directly or to an external reference. Figure 6 shows the reference and buffer structure for the LTC1411. The input to the reference buffer is either REFIN or 1/2 of REFIN depending on the PGA selection. The REFCOM1 pin bypassed with a 10µF tantalum capacitor helps reduce the noise going into the buffer. The reference buffer has a gain of 1.62 or 1.15 (depends on PGA selection). It is compensated at the REFCOM2 pin with a 10µF tantalum capacitor. The input span of the ADC is set by the output voltage of this REFCOM2 voltage. For a 2.5V input at the REFIN pin, the REFCOM2 will have 4V output for PGA1 = PGA0 = 5V and the ADC will have a span of 3.6V.



*THIS PIN CAN BE TIED TO REFOUT OR AN EXTERNAL SOURCE
**A 22µF CAPACITOR IS NEEDED IF REFOUT IS USED TO DRIVE A_{IN}^-

Figure 6. Reference Structure for the LTC1411 for PGA1 = PGA0 = 5V

APPLICATIONS INFORMATION

Figure 7 shows a typical reference, the LT1019A-2.5 connected to the LTC1411. This will provide an improved drift (equal to the maximum 5ppm/°C of the LT1019A-2.5).

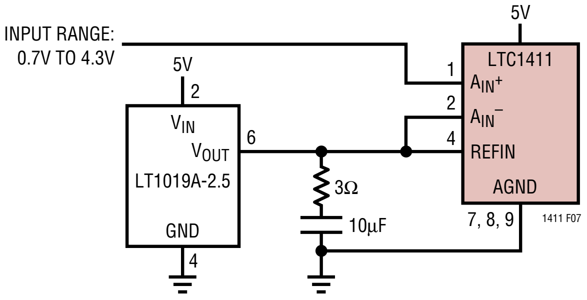


Figure 7. Supplying a 2.5V Reference Voltage to the LTC1411 with the LT1019A-2.5

Digital Interface

The ADC has a very simple digital interface with only one control input, $\overline{\text{CONVST}}$. A logic low applied to the $\overline{\text{CONVST}}$ input will initiate a conversion. The ADC presents digital data in 2's complement format with bipolar zero set by the voltage applied to the A_{IN}^- pin.

Internal Clock

The internal clock is factory trimmed to achieve a typical conversion time of 260ns. With the typical acquisition time of 100ns, a throughput sampling rate of 2.5Msps is guaranteed.

Out-of-the-Range Signal (OTR)

The LTC1411 has a digital output, OTR, that indicates if an analog input signal is out of range. The OTR remains low when the analog input is within the specified range. Once the analog signal goes to the most negative input (1000 0000 0000 00) or 64LSB above the specified most positive input, OTR will go high. By NORing D13 (MSB) and its complement with OTR, overrange and underrange can be detected as shown in Figure 8. Table 2 is the truth table of the out-of-the-range circuit in Figure 8.

Power Shutdown (Sleep and Nap Modes)

The LTC1411 provides two shutdown features that will save power when the ADC is inactive.

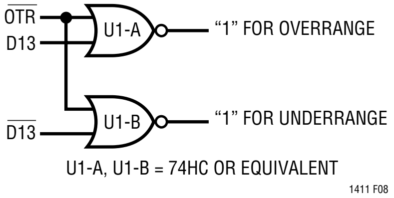


Figure 8. Overrange and Underrange Logic

Table 2. Out-of-the-Range Truth Table

OTR	D13 (MSB)	ANALOG INPUT
0	0	In Range
0	1	In Range
1	0	Overrange
1	1	Underrange

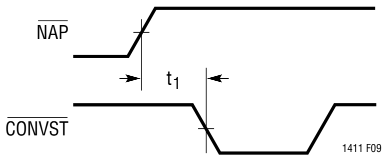


Figure 9. $\overline{\text{NAP}}$ to $\overline{\text{CONVST}}$ Wake-Up Timing

By driving the $\overline{\text{SLP}}$ pin low for Sleep mode, the ADC shuts down to less than 1µA. After release from the Sleep mode, the ADC needs 210ms (10µF bypass capacitor on the REFCOM2 pin) to wake up.

In Nap mode, all the power is off except the internal reference which is still active for the other external circuitry. In this mode the ADC draws about 2mA instead of 39mA (for minimum power, the logic inputs must be within 600mV from the supply rails). The wake-up time from Nap mode to active state is 250ns as shown in Figure 9.

Board Layout and Bypassing

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1411, a printed circuit board with a ground plane is required. Layout for the printed circuit board should ensure that the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track.

APPLICATIONS INFORMATION

An analog ground plane separate from the logic system ground should be established under and around the ADC. AGND1, 2, 3 (Pins 7 to 9), AVM (Pin 11), DGND (Pin 31) and OGND (Pin 28) and all other analog grounds should be connected to a single analog ground point. The REFOUT, REFCOM1, REFCOM2 and AVP should bypass to this analog ground plane (see Figure 10). No other digital grounds should be connected to this analog ground plane. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible.

Timing and Control

Conversion start is controlled by the $\overline{\text{CONVST}}$ digital input. The falling edge transition of the $\overline{\text{CONVST}}$ will start a conversion. Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{\text{BUSY}}$ output. $\overline{\text{BUSY}}$ is low during a conversion.

The digital output code is updated at the end of conversion about 7ns after $\overline{\text{BUSY}}$ rises, i.e., output data is not valid on the rising edge of $\overline{\text{BUSY}}$. Valid data can be latched with the falling edge of $\overline{\text{BUSY}}$ or with the rising edge of $\overline{\text{CONVST}}$. In either case, the data latched will be for the previous conversion results. Figures 11a and 11b are the timing diagrams for the LTC1411.

3V Input/Output Compatible

The LTC1411 operates on a 5V supply, which makes the device easy to interface to 5V digital systems. This device can also talk to 3V digital systems: the digital input pins ($\overline{\text{CONVST}}$, $\overline{\text{NAP}}$ and $\overline{\text{SLP}}$) of the LTC1411 recognize 3V or 5V inputs. The LTC1411 has a dedicated output supply pin (OV_{DD}) that controls the output swings of the digital output pins (D0 to D13, $\overline{\text{BUSY}}$ and OTR) and allows the part to talk to either 3V or 5V digital systems. The output is two's complement binary.

Figure 12 is the input/output characteristics of the ADC when $A_{IN}^- = 2.5V$. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB... FS – 1.5LSB). The output code is scaled such that 1LSB = FS/16384 = 3.6V/16384 = 219.7µV.

Offset and Full-Scale Adjustment

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 13 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset applied to the A_{IN}^- input. For zero offset error, apply 2.49989V (i.e., –0.5LSB) at A_{IN}^+ and adjust R2 at the A_{IN}^- input until the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11. For full-scale adjustment, an input voltage of 4.29967V (FS – 1.5LSBs) is applied to A_{IN}^+ and R5 is adjusted until the output code flickers between 0111 1111 1111 10 and 0111 1111 1111 11.

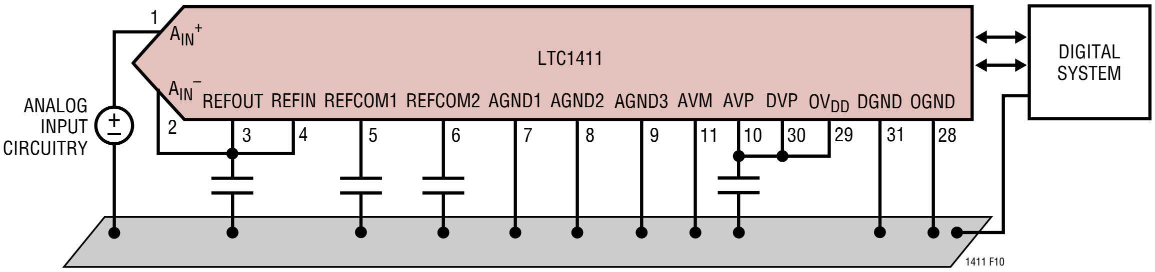


Figure 10. Power Supply Grounding Practice

APPLICATIONS INFORMATION

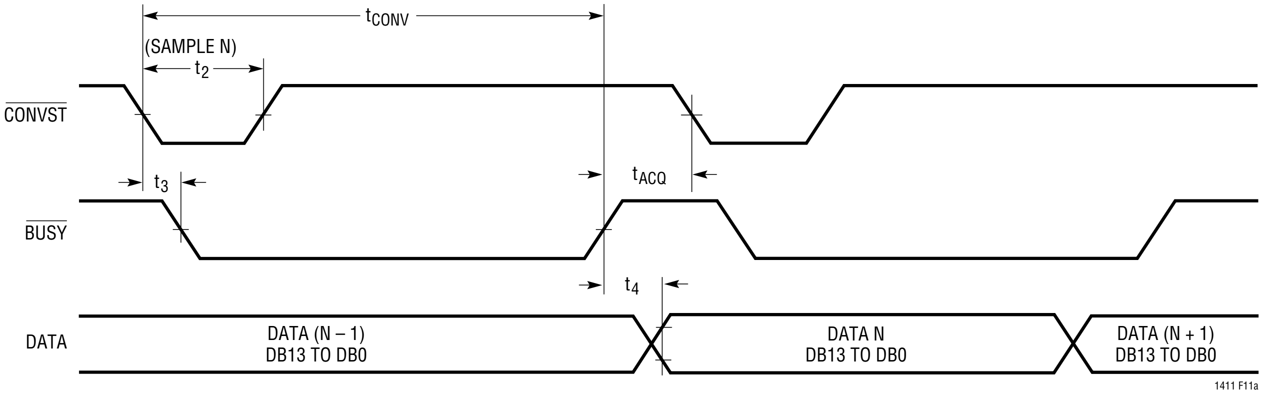


Figure 11a. $\overline{\text{CONVST}}$ Starts a Conversion with a Short Active Low Pulse

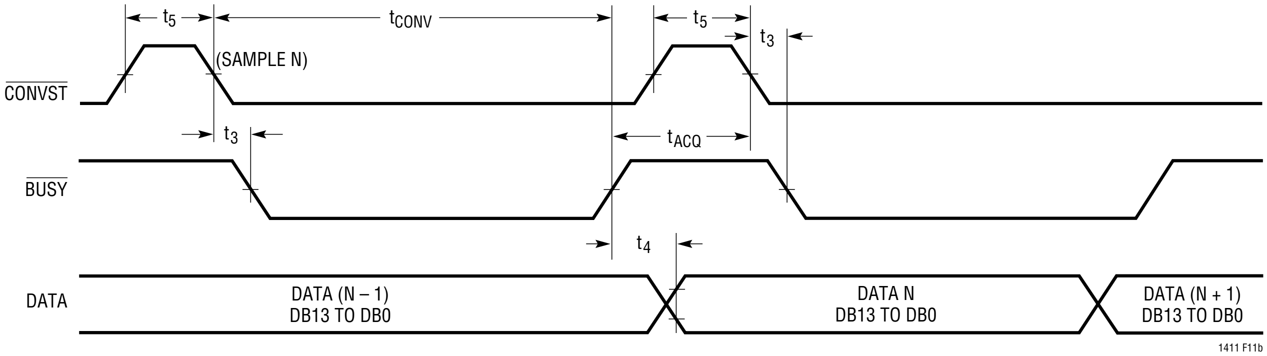


Figure 11b. $\overline{\text{CONVST}}$ Starts a Conversion with a Short Active High Pulse

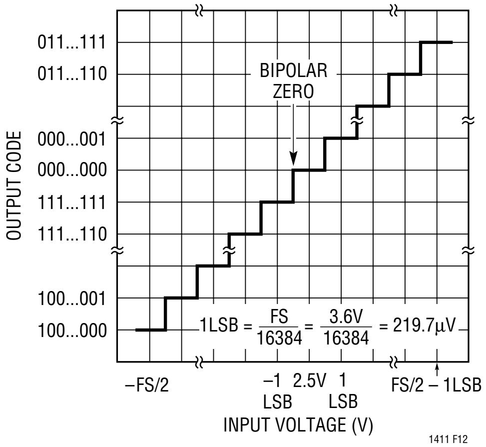


Figure 12. LTC1411 Bipolar Transfer Characteristics (2's Complement)

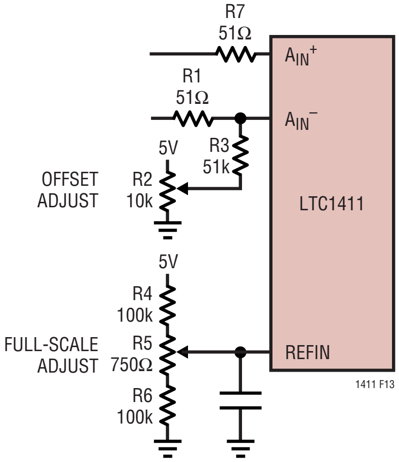
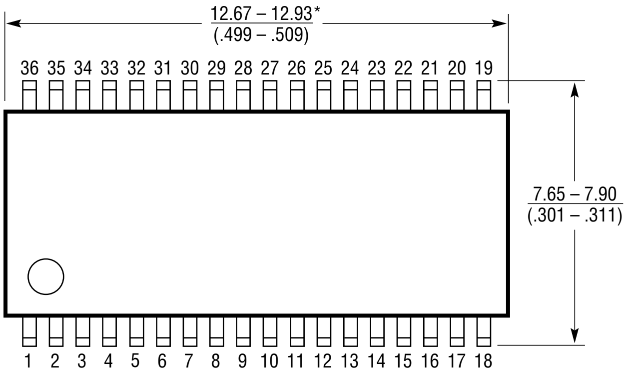
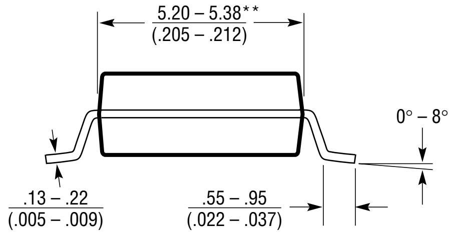


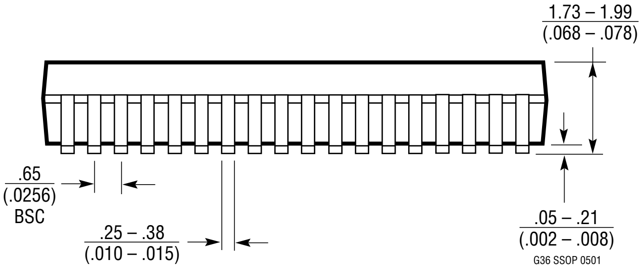
Figure 13. Offset and Full-Scale Adjustment

PACKAGE DESCRIPTION

G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)







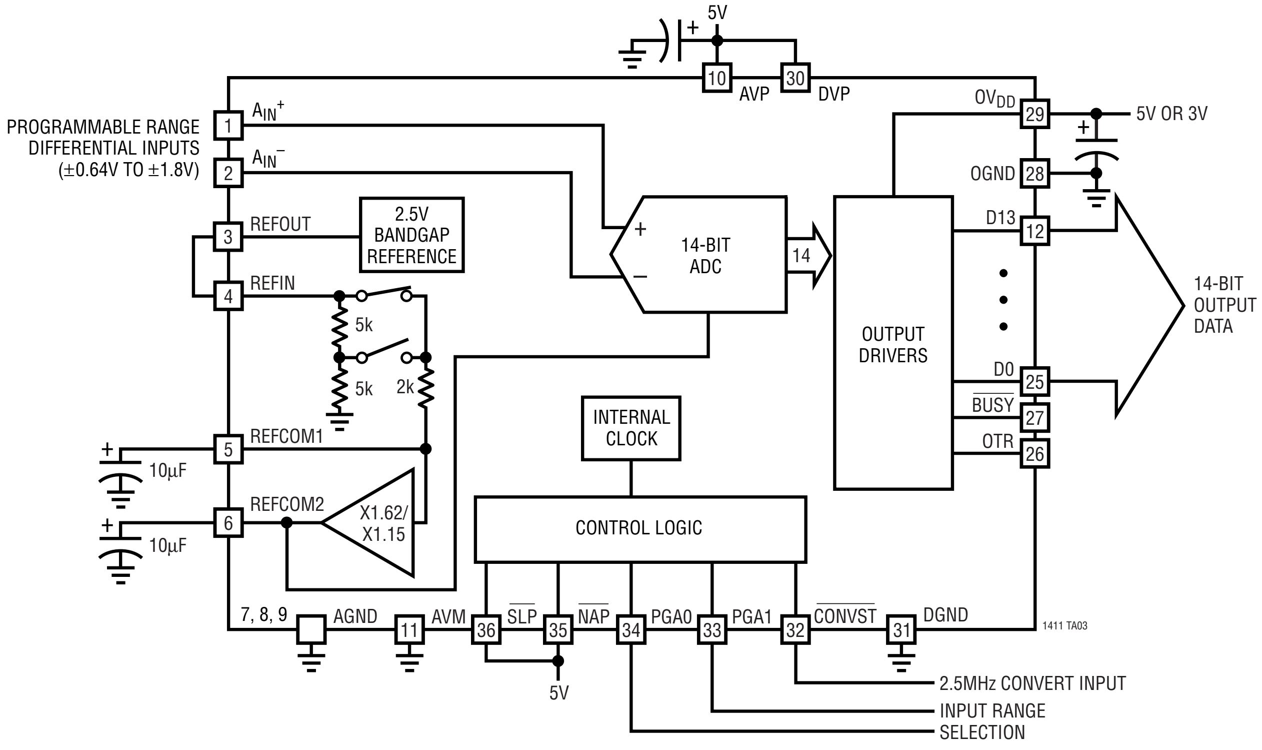
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

TYPICAL APPLICATION

2.5Msps 14-Bit ADC with Programmable Input Range



RELATED PARTS

PART NUMBER	RESOLUTION	SPEED	COMMENTS
16-Bit			
LTC1608	16	500ksps	±2.5V Input Range, Pin Compatible with LTC1604
14-Bit			
LTC1414	14	2.2Msps	150mW, 81dB SINAD and 95dB SFDR
LTC1419	14	800ksps	150mW, 81.5dB SINAD and 95dB SFDR
LTC1744	14	50Msps	1.5W, Two Modes: 77dB SNR or 90dB SFDR
12-Bit			
LTC1420	12	10Msps	5V or ±5V Supply, 71dB SINAD and Input PGA
LTC1412	12	3Msps	150mW, 71dB SINAD and 84dB THD
LTC1402	12	2.2Msps	90mW, Serial Interface, 16-Lead SSOP Package
LTC1405	12	5Msps	115mW, 71.3dB S/N+D, 85dB SFDR
LTC1410	12	1.25Msps	150mW, 71.5dB SINAD and 84dB THD
LTC1415	12	1.25Msps	55mW, Single 5V Supply

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