

Four-Bit Single-Chip Microcontrollers with 4, 6, and 8 KB of On-Chip ROM

Overview

The LC662104A, LC662106A, and LC662108A are 4-bit CMOS microcontrollers that integrate on a single chip all the functions required in a special-purpose telephone controller, including ROM, RAM, I/O ports, a serial interface, a DTMF generator, timers, and interrupt functions. These microcontrollers are available in a 30-pin package.

Features and Functions

- On-chip ROM capacities of 4, 6, and 8 kilobytes, and an on-chip RAM capacity of 384 × 4 bits.
- Fully supports the LC66000 Series common instruction set (128 instructions). (The special-purpose instructions for TM1 and SI/01 are disabled.)
- I/O ports: 24 pins
- · DTMF generator

This microcontroller incorporates a circuit that can generate two sine wave outputs, DTMF output.

• 8-bit serial interface: one circuit

- Instruction cycle time: 0.95 to 10 µs (at 3.0 to 5.5 V)
- Powerful timer functions and prescalers
 - Time limit timer, event counter, pulse width measurement, and square wave output using a 12-bit timer.
 - Time base function using a 12-bit prescaler.
- Powerful interrupt system with 6 interrupt factors and 6 interrupt vector locations.
 - External interrupts: 3 factors/3 vector locations
 - Internal interrupts: 3 factors/3 vector locations
- Flexible I/O functions

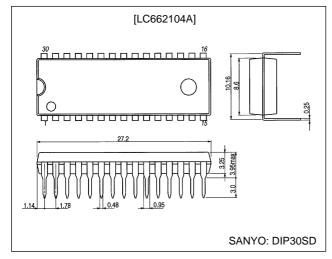
 Selectable options include 20-mA drive outputs, pull-up and open drain circuits.
- Optional runaway detection function (watchdog timer)
- 8-bit I/O functions
- Power saving functions using halt and hold modes.
- Packages: DIP30SD, MFP30S
- Evaluation ICs: LC665099 (evaluation chip) + EVA86K
 ECB662500
 - LC66E2108(on-chip EPROM microcontroller)

- Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.
- SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

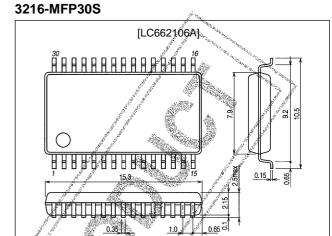
Package Dimensions

unit: mm

3196-DIP30SD

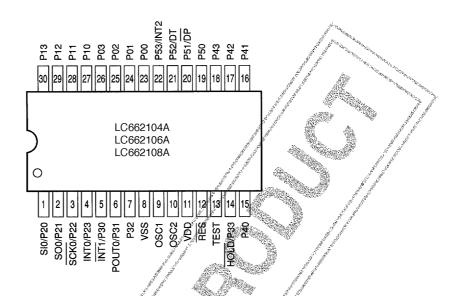






SANYO: MFP30S

				1500 Kills		
Type No.	No. of pins	ROM capacity	RAM capacity	Pacl	kage	Features
LC66304A/306A/308A	42	4 K/6 K/8 KB	512 W	DIP42S	QFP48E	
LC66404A/406A/408A	42	4 K/6 K/8 KB	512 W	DIP42S	QFP48E	Normal versions 4.0 to 6.0 V/0.92 µs
LC66506B/508B/512B/516B	64	6 K/8 K/12 K/16 KB	512 W	DIP64S	QFP64A	4.0 to 6.0 V/0.92 μs
LC66354A/356A/358A	42	4 K/6 K/8 KB	512 W	DIP42S / /	QFP48E	
LC66354S/356S/358S	42	4 K/6 K/8 KB	512 W	1 1	QFP44M	Low-voltage versions
LC66556A/558A/562A/566A	64	6 K/8 K/12 K/16 KB	512 W	DIP64S	QFP64E	2.2 to 5.5 V/3.92 μs
LC66354B/356B/358B	42	4 K/6 K/8 KB	512 W	DIP42S	QFP48E	Low-voltage high-speed versions
LC66556B/558B/562B/566B	64	6 K/8 K/12 K/16 KB	512 W	DIP64S	QFP64E	3.0 to 5.5 V/0.92 µs
LC66354C/356C/358C	42	4 K/6 K/8 KB	512 W	ĎIP42S	QFP48E	2.5 to 5.5 V/0.92 µs
LC662104A/06A/08A	30	4 K/6 K/8 KB	384 W	DIP30SD	MFP30S	0 11 5715
LC662304A/06A/08A/12A/16A	42	4 K/6 K/8 K/12 K/16 KB	512 W	DIP42S	QFP48E	On-chip DTMF generator versions 3.0 to 5.5 V/0.95 µs
LC662508A/12A/16A	64	8 K/12 K/16 KB	512 W	DIP64S	QFP64E	σ.ο το σ.ο γγο.οο μο
LC665304A/06A/08A/12A/16A	48	4 K/6 K/8 K/12 K/16 KB	512 W	DIP48S	QFP48E	Dual oscillator support 3.0 to 5.5 V/0.95 µs
LC66E308	42	EPROM 8 KB	512 W	DIC42S with window	QFC48 with window	
LC66P308	42	OTPROM 8 KB	512 W	DIP42S	QFP48E	
LC66E408	42	EPROM & KB	512 W	DIC42S with window	QFC48 with window	Window and OTP evaluation versions
LC66P408	42	OTPROM 8 KB	512 W	DIP42S	QFP48E	4.5 to 5.5 V/0.92 μs
LC66E516	64	EPROM 16 KB	512 W	DIC64S with window	QFC64 with window	
LC66P516	64 🖟 👌	OTPROM 16 KB	512 W	DIP64S	QFP64E	
LC66E2108	30	EPROM 8 KB	384 W			
LC66E2316	42	EPROM 16 KB	512 W	DIC42S with window	QFC48 with window	Window evaluation versions
LC66E2516	64	EPROM 16 KB	512 W	DIC64S with window	QFC64 with window	4.5 to 5.5 V/0.95 µs
LC66E5316	52/48	EPROM 16 KB	512 W	DIC52S with window	QFC48 with window	
LC66P2108	30	OTPROM 8 KB	384 W	DIP30SD	MFP30S	
LC66P2316	42	OTPROM 16 KB	512 W	DIP42S	QFP48E	OTP
LC66P2516	64	OTPROM 16 KB	512 W	DIP64S	QFP64E	4.0 to 5.5 V/0.95 μs
LC66P5316	48	OTPROM 16 KB	512 W	DIP48S	QFP48E	

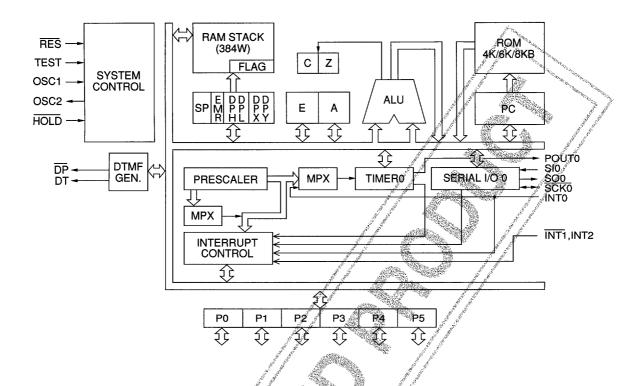


We recommend the use of reflow-soldering techniques to solder-mount MFP packages.

Please consult with your Sanyo representative for details on process conditions if the package itself is to be directly immersed in a dip-soldering bath (dip-soldering techniques).



System Block Diagram



Differences between the LC663XX Series and the LC6621XX Series

	/ / *WWW	<i>M J J J</i>	
Item	LC6630X Series (Including the LC66599 evaluation chip)	LC6635XB Series	LC6621XX Series
System differences • Hardware wait time (number of cycles) when hold mode is cleared	65536 cycles About 64 ms at 4 MHz (Teys = 1 µs)	16384 cycles About 16 ms at 4 MHz (Tcyc = 1 µs)	16384 cycles About 16 ms at 4 MHz (Tcyc = 1 µs)
Value of timer 0 after a reset (Including the value after hold mode is cleared)	Set to FF0.	Set to FFC.	Set to FFC.
DTMF generator	None (Tools are handled with external devices.)	None	Yes
• Inverter array	None (Tools are handled with external devices.)	None	None
• SIO1	Yes	Yes	None
Three-value inputs/comparator inputs	Yes	Yes	None
Three-state output from P31 and P32	None	None	Yes
Using P0 to clear halt mode	In 4-bit groups	In 4-bit groups	Can be specified for each bit.
External extended interrupts	None for INT3, INT4, and INT5. (Tools are handled with external devices.)	None for INT3, INT4, and INT5.	INT3, INT4, and INT5 can be used with the internal functions.
Ofher P53 functions	Shared with INT2 (Fools are handled with external devices.)	Shared with INT2	Shared with INT2
Differences in main characteristics Operating power supply voltage and operating speed (cycle time)	LC66304A/306A/308A 4.0 to 6.0 V/0.92 to 10 μs LC66E308/P308 4.5 to 5.5 V/0.92 to 10 μs	• 3.0 to 5.5 V/0.92 to 10 µs • LC6635XA 2.2 to 5.5 V/3.92 to 10 µs 3.0 to 5.5 V/1.96 to 10 µs	3.0 to 5.5 V/0.95 to 10 μs
Pull-up resistors	P0, P1, P4, and P5: about 3 to 10 kΩ	P0, P1, P4, and P5: about 3 to 10 $k\Omega$	P0, P1, P4, and P5: about 100 kΩ
Port voltage handling	P2 to P6 and PC: 15V handling P0, P1, PD, PE: Normal voltage handling	P2 to P6 and PC: 15V handling P0, P1, PD, PE: Normal voltage handling	P2 to P4, P51, and P53: 15V voltage handling Others: normal voltage handling

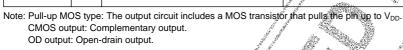
Pin Function Overview

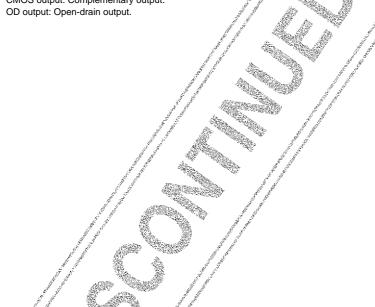
Pin	I/O	Overview	Output driver type	Options	State after a reset
P00 P01 P02 P03	I/O	I/O ports P00 to P03 Input or output in 4-bit or 1-bit units P00 to P03 support the halt mode control function (This function can be specified in bit units.)	Pch: Pull-up MOS type Nch: Intermediate sink current type	Pull-up MOS or Nch OD output Output level on reset	High or low (option)
P10 P11 P12 P13	I/O	I/O ports P10 to P13 Input or output in 4-bit or 1-bit units	Pch: Pull-up MOS type Nch: Intermediate sink current, type **The company of the current of the	Pull-up MOS or Nch OD output • Output level on reset	High or low (option)
P20/SI0 P21/SO0 P22/SCK0 P23/INT0	I/O	I/O ports P20 to P23 Input or output in 4-bit or 1-bit units P20 is also used as the serial input SI0 pin. P21 is also used as the serial output SO0 pin. P22 is also used as the serial clock SCK0 pin. P23 is also used as the INTO interrupt request pin, and also as the timer 0 event counting and pulse width measurement input.	Pch: CMOS type Nch: Intermediate sink current type Nch: +15V handling when QD option selected Pch: CMOS type The current ty	CMOS or Nori OD output	Н
P30/INT1 P31/POUT0 P32	I/O	I/O ports P30 to P32 Input or output in 3-bit or 1-bit units P30 is also used as the INT1 interrupt request. P31 is also used for the square wave output from timer 0. P31 and P32 also support 3-state outputs.	Peh: CMOS type Non-intermediate sink current type Neh: +15V handling when OD option selected • Peh: CMOS type • Neh: +15V handling when OD option selected	CMOS or Nch OD output	Н
P33/HOLD	I STATE OF THE STA	Hold mode control input Hold mode is set up by the HOLD instew. In hold mode, the CPU is restarted by setting HOLD to the high level. This pin can be used as input port P33' along with P30 to P32. When the P33/HOLD pin is at the low level the CPU will not be reset by a low level on the RES pin. Therefore, applications must not set P33/HOLD tow when power is first applied.	September 1985 and 19		
P40 P41 P42 P43	ì/O	I/O ports P40 to P43 • Input or output in 4-bit or 1-bit units • Input or output in 8-bit units when used in conjunction with P50 to P53. • Can be used for output of 8-bit ROM data when used in conjunction with P50 to P53.	Pch: Pull-up MOS type Nch: Intermediate sink current type Nch: +15V handkling when OD option selected	Pull-up MOS or Nch OD output Output level on reset	High or low (option)

Continued on next page.

Continued from preceding page.

Pin	I/O	Overview	Output driver type	Options	State after a reset
P50 P51/DP P52/DT P53/INT2	I/O	I/O ports P50 to P53 Input or output in 4-bit or 1-bit units P51 is also used for dial pulse output P52 is also used for DTMF output P53 is also used as the INT2 interrupt request.	Pch: Pull-up MOS type Nch: Intermediate sink current type Nch: +15-V handling when OD option selected (P51 and P53 only)	Pull-up MOS or Neh OD output Output level on reset Output level after a reset (An external pull-up resistor must be supplied when used for DT output)	High or low (option)
OSC1 OSC2	0	System clock oscillator connections When an external clock is used, leave OSC2 open and connect the clock signal to OSC1.	And the state of t	Ceramic oscillator or external clock selection	Option selection
RES	ı	System reset input When the P33/HOLD pin is at the high level, a low level input to the RES pin will initialize the CPU.			
TEST	ı	CPU test pin This pin must be connected to V _{SS} during normal operation.			
V _{DD} V _{SS}		Power supply pins			





User Options

1. Port 0, 1, 4, and 5 output level options a reset

The output levels at reset for I/O ports 0, 1, 4, and 5 in independent 4-bit groups, can be selected from the following two options.

Option	Conditions and notes
Output high at reset	The four bits of ports 0, 1, 4, or 5 are set in a group
Output low at reset	The four bits of ports 0, 1, 4, or 5 are set in a group

2. Oscillator circuit options

• Main clock

Option	Circuit	and the same of th	Conditions and notes
External clock	OSC1 DOMESTIC		The input has Schmitt characteristics
Ceramic oscillator	C1 OSC1 Ceramic oscillator C2 OSC2		

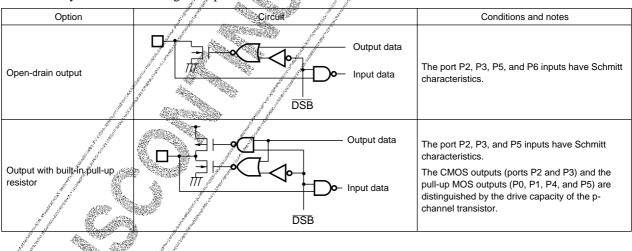
Note: There is no RC oscillator option.

3. Watchdog timer option

A runaway detection function (watchdog timer) can be selected as an option.

4. Port output type options

• The output type of each bit (pin) in ports P0, P1, P2, P3 (except for the P33/HOLD pin), P4, and P5 can be selected individually from the following two options.



LC662108 Series Option Data Area and Definitions

ROM area	Bit		Option specified	Option/data relationship	
	7	P5	Output level at reset	0 = high level, 1 = low level	
	6	P4			
	5	Unused		This bit must be set to 0.	
2000H	4	Oscillator	option	0 = (RC oscillator) external clock, 1 = ceramic oscillator	
	3	Unused	T	This bit must be set to 0.	
	2	P1	Output level at reset	0 = low level, 1 ≠ high level	
	1	P0	Aire a realise		
	7	P13	timer option	0 = none, 1 ≠ yes	
	6	P12			
	5	P11	Output type	0 = QD, 1 = PU	
	4	P10			
2001H	3	P03			
	2	P02			
	1	P01	Output type	0 = Q0 1 = PU	
	0	P00	11		
	7	Unused		This bit must be set to 0.	
	6	P32			
	5	P31	Output type	0 = QD _s 1 = PU	
000011	4	P30			
2002H	3	P23	11	Do. 11	
	2	P22	Output type	0 = OD 1 ± PU	
	1	P21	Output type	0 = 00, 1 = P0	
	0	P20			
	7	P53			
	6	P52	Output type	0 = OD, 1 = PU	
	5	P51	Output type	0 - 02, 1 - 1 0	
2003H	4	P50	<u> </u>		
	3	P43			
	2	P42	Output type	0 = OD, 1 = PU	
	1	P41			
	0	P40			
	7				
	6	11			
2004H	5	garate water		T1: 1:	
to	4	Unused		This bit must be set to 0.	
200CH	2	r ş		*: Location 2008H must be set to 7F.	
	4/1				
	0				
	7 7				
g Parket	6				
A Part	5				
	-4	46,50		This data is generated by the assmbler (21).	
200DH	3	Reserved	Must be set to predefined values.	If the assembler is not used, set this data to 00.	
A Comment	- 2				
A STANDARD OF THE STANDARD OF	1				
and the same	0	and the state of t			
	Z	J. J.			
	6	1			
	5	1			
200511	4	Des -: .	Must be est to madefine division	This data is generated by the assmbler (0x).	
200EH	3	reserved	. Must be set to predefined values.	If the assembler is not used, set this data to 00.	
	2]			
	1				
	0			Continued on next pa	

Continued on next page.

Continued from preceding page.

ROM area	Bit	Option specified	Option/data relationship
	7		
	6		
	5		
200FH	4	Reserved. Must be set to predefined values.	This data is generated by the assmbler (00).
200111	3	reserved. Must be set to predefined values.	If the assembler is not used, set this data to (00):
	2		
	1		
	0		

Specifications

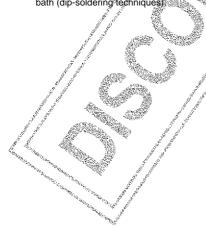
Absolute Maximum Ratings at $Ta = 25^{\circ}C$, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings	Unit	Note
Maximum supply voltage	V _{DD} max	V _{DD}	≠0,3 to +7.0	V	
Input voltage	V _{IN} 1	P2, P3 (except for the P33/HOLD pin), P4, P51, and P53	0.3 to +15.0	V	1
	V _{IN} 2	All other inputs	-0.3 to V _{DD} + 0.3	V	2
Output voltage	V _{OUT} 1	P2 and P3 (except for the P33/HQLD pin)	−0.3 to +15.0	V	1
Output voltage	V _{OUT} 2	All other inputs	-0.3 to $V_{DD} + 0.3$	V	2
	I _{ON} 1	P0, P1, P2, P3 (except for the P33/HOLD pin), P4, P5	20	mA	3
Output current per pin	−l _{OP} 1	P0, P1, P4, P5	2	mA	4
	-I _{OP} 2	P2, P3 (except for the P33/HOLD pin)	4	mA	4
	Σ I _{ON} 1	P1, P2, P3 (except for the P33/HQLD pin)	75	mA	3
Total pin augrent	Σ I _{ON} 2	P0, P4, P5	75	mA	3
Total pin current	Σl _{OP} 1	P1, P2, P3 (except for the P33/HOLD pin)	25	mA	4
	Σ _{lop} 2	P0, P4, P5	25	mA	4
Allowable power dissipation	.Pd max	Ta = -30 to +70°C: DIP30S (MFP30S)	340 (200)	mW	5
Operating temperature	Topr		-30 to +70	°C	
Storage temperature	Tstg		-55 to +125	°C	

Note: 1. Applies to pins with open-drain output specifications. For pins with other than open-drain output specifications, the ratings in the pin column for that pin apply.

2. For the oscillator input and output pins, levels up to the free-running oscillation level are allowed.

- 3. Sink current
- Source current
 We recommend the use of reflow soldering techniques to solder mount MFP packages.
 Please consult with your Sanyo representative for details on process conditions if the package itself is to be directly immersed in a dip-soldering bath (dip-soldering techniques).



Allowable Operating Ranges at Ta = -30 to $+70^{\circ}C$, $V_{SS} = 0$ V, $V_{DD} = 3.0$ to 5.5 V, unless otherwise specified.

D	Oh al	O an aliticana		Ratings		1.1-24	NI-4-
Parameter	Symbol	Conditions	min	typ	max	Unit	Note
Operating supply voltage	V_{DD}	V _{DD}	3.0		5.5	V	
Memory retention supply voltage	$V_{DD}H$	V _{DD} : During hold mode	1.8		5.5	V	
	V _{IH} 1	P2, P3 (except for the P33/HOLD pin), P4, P51, and P53: N-channel output transistor off	0.8 V _{DD}	11	13.5	V	1
Input high-level voltage	V _{IH} 2	P33/HOLD, RES, OSC1: N-channel output transistor off	0.8 V _{DD}	1 1	V _{DD}	V,	s.
	V _{IH} 3	P0, P1, P50, P52: N-channel output transistor off	0.8 V _{pD}		V _{DD}	/ x	
	V _{IL} 1	P2, P3 (except for the P33/HOLD pin), RES, and OSC1: N-channel output transistor off	V _{ss}	47 41 (0)	0.2 V _{DD}	¹ V	2
Input low-level voltage	V _{IL} 2	P33/HOLD: V _{DD} = 1.8 to 5.5 V	√ V _{SS} 🤄	b. 1	0.2 V _{DD}	V	
	V _{IL} 3	P0, P1, P4, P5, TEST: N-channel output transistor off	V _{SS}		0.2 V _{DD}	>	
Operating frequency (instruction cycle time)	fop (Tcyc)		0.4 (10)		4.20 (0.95)	MHz (µs)	
[External clock input conditions]							
Frequency	f_{ext}		0.4		4.20	MHz	
Pulse width	$t_{\rm extH}$, $t_{\rm extL}$	OSC1: Defined by Figure 1. Input the clock signal to OSC1 and leave OSC2 open. (External clock input must be selected as the oscillator circuit option.)	1,00			ns	
Rise and fall times	$t_{\text{extR}}, t_{\text{extF}}$				30	ns	

Note: 1. Applies to pins with open-drain specifications. However, V_{II}2 is applied to the P33/HOLD pin. When ports P2 and P3 have CMOS output specifications they cannot be used as input pins.

2. Applies to pins with open-drain specifications.



Electrical Characteristics at Ta = -30 to +70 $^{\circ}$ C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V unless otherwise specified.

D		Symbol Conditions			Ratings			Note	
Parameter		Symbol	Conditi	ions	min	typ	max	Unit	Note
Input high-level current		I _{IH} 1	P2, P3 (except for the P3: P51, and P53: V _{IN} = 13.5 Nch transistor off			and the second	5.0	μА	1
		I _{IH} 2	P0, P1, P50, P52, OSC1, $V_{IN} = V_{DD}$, with the output				1.0	μΑ	1
Input low-level current		I _{IL} 1	P0, P1, P2, P3, P4, and F $V_{IN} = V_{SS}$, with the output		-1.0	1		μA	2
Output high-level voltage		V _{OH} 1	P2, P3 (except for the P33/HOLD pin)	$I_{OH} = -1 \text{ mA}$ $I_{OH} = -0.1 \text{ mA}$	$V_{DD} = 1.0$ $V_{DD} = 0.5$		A. SA	//v	3
Value of the output pull-up	resistor	R _{PO}	P0, P1, P4, P5		30	100	150	kΩ	
		V _{OL} 1	P0, P1, P2, P3, P4, and F (except for the P33/HOLD		/ 4		0.4	V	5
Output low-level voltage		V _{OL} 2	P0, P1, P2, P3, P4, and F (except for the P33/HOLD	C" 47			1.5	V	
		I _{OFF} 1	P2, P3, P4, P51, and P53	3: V _{IN} = 13.5 V	2000 x 2000		5.0	μA	6
Output off leakage curren	t	I _{OFF} 2	Does not apply to P2, P3, $V_{IN} = V_{DD}$	P4, P51, and P53:		A Part of the last	1.0	μA	6
[Schmitt characteristics]					AND WAR	See Market			
Hysteresis voltage		V _{HYS}			Na.	0.1 V _{DD}			
High-level threshold volta	ge	Vt _H	P2, P3, P4, P5, and RES	// 455m. Va.	0.5 V _{DB}	1	0.8 V _{DD}	V	
Low-level threshold voltage	je	VtL			0.2 V _{DD}	f"	0.5 V _{DD}	V	
[Ceramic oscillator]	-				11				
Oscillator frequency		f _{CF}	OSC1, OSC2: See Figure	2. 4 MHz		4.0		MHz	
Oscillator stabilization tim	e	f _{CFS}	See Figure 3. 4 MHz		//		10.0	ms	
[Serial clock]		0.0	John John State Committee	*************************************	7				
	Input			*************************************	0.9			μs	
Cycle time	Output	t _{CKCY}	// 4		2.0			Tcyc	
Low-level and high-level	Input	t _{CKL}	SCK0. With the timing of	Figure 4 and the test	0.4			μs	
pulse widths	Output	t _{CKH}	load of Figure 5.	1/	1.0			Tcyc	
Rise an fall times	Output	t _{CKR} , t _{CKF}		7/			0.1	μs	
[Serial input]		-CRIC -CRI	<u> </u>					P-5	
Data setup time			SIO: With the timing of Fig		0.3			μs	
		t _{ick}	Stipulated with respect to		0.3			-	
Data hold time		‡ckı		*	0.3			μs	
[Serial output]	- F	A Albert	1000 1000 11 - 15 - 4 - 15	: 4 4 4 4					_
Output delay time	A CONTRACTOR OF THE PARTY OF TH	t _{CKO} *	SO0 With the timing of Fi load of Figure 5. Stipulate falling edge (1) of SCK0.	ed with respect to the			0.3	μs	
[Pulse conditions]	100	' 			1	1	1	1	
INT0 high and low-level		t _{IOH} , t _{IOL}	INTO: Figure 6, conditions interrupt can be accepted which the timer 0 event comeasurement input can b	, conditions under ounter or pulse width	2			Тсус	
High and low-level pulses for interrupt inputs other th		t _{IIH} , t _{IIL}	NT1, INT2: Figure 6, con the corresponding interru	ditions under which	2			Тсус	
RES high and low-level pulse widths		t _{RSH} , t _{RŠL}	RES: Figure 6, conditions can be applied.	•	3			Тсус	
7 4 40 . *	A.	1	1		1	1	1	ı	-
		V7.	V _{DD} : 4-MHz ceramic oscil	lator		4.5	8.0	mA	
Operating current drain	de de la companya de	/ I _{DD OP}	V _{DD} : 4-MHz external clock			4.5	8.0	mA	- 8
The state of the s	al parties of the same	8	V _{DD} : 4-MHz ceramic oscil			2.5	5.5	mA	
Halt mode current drain	A STREET PROPERTY.	I _{DDHALT}	V _{DD} : 4-MHz external clock			2.5	5.5	mA	1
Hold mode current drain	No.	I _{DDHOLD}	V _{DD} : V _{DD} = 1.8 to 5.5 V			0.01	10	μA	
	loh trono		red I/O ports with the open	drain output enocification	ne Thoso pi	ns cannot bo	Lucad on innu		

Note: 1. With the output Nch transistor off in shared I/O ports with the open-drain output specifications. These pins cannot be used as input pins if the CMOS output specifications are selected.

^{2.} With the output Nch transistor off in shared I/O ports with the open-drain output specifications. The rating for the pull-up output specification pins is stipulated in terms of the output pull-up current IPO. These pins cannot be used as input pins if the CMOS output specifications are selected.

^{3.} With the output Nch transistor off for CMOS output specification pins.

^{4.} With the output Nch transistor off for pull-up output specification pins.

^{6.} With the output Pch transistor off for open-drain output specification pins.

^{7.} Reset state

Tone (DTMF) Output Characteristics

DC Characteristics at $Ta = -30~to~+70^{\circ}C,\,V_{SS} = 0~V$

Parameter	Symbol	Symbol Conditions		Ratings				
Farameter	Symbol	Conditions	min	, typ 🔍	max	Unit		
Tone output voltage	V _{T1}	DT: Single tone, V _{DD} = 3.5 to 5.5 V*	0.9	1:3	2.0	Vp-p		
Row/column tone output voltage ratio	D _{BCR1}	DT: Dual tones, V _{DD} = 3.5 to 5.5 V*	4.0	2.0	3.0	dB		
			111		A. S.	7		

Note*: See Figure 7.

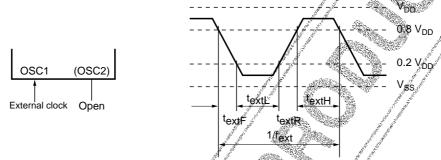


Figure 1 External Clock Input Waveform

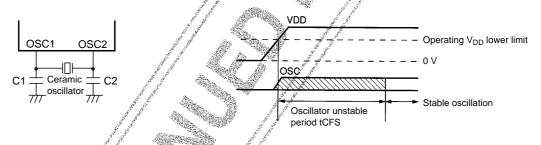


Figure 2 Ceramic Oscillator Circuit

Figure 3 Oscillator Stabilization Period

External capacitor type		Built-in ca	apacitor type	
4 MHz (Murata Mfg. Co., Ltd.) CSA4.00MG	C1 = 33 pF C2 = 33 pF	A MHz (Murata Mfg. Co., Ltd.) CST4.00MG		
4 MHz (Kyocera Corporation) KBR4.0MSB	C1 = 33 pF C2 #33 pF	4 MHz (Kyocera Corporation) KBR4.0MKC		
SCK0 0/2 VDD (input) 0.4 VDD (output) SI0	0.8 VD 0.2 VD	tCKF 0.8 VDD (input) VDD = 1 (output) D	TEST point O	₹ R=1kΩ
SO0	V _{DD} - 1 0.4 V _{DD}			C=50p

Timing Load

Figure 4 Serial I/O Timing Figure 5

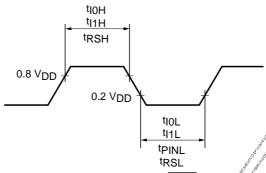


Figure 6 Input Timing for the INT0, INT1, INT2, and RES pins

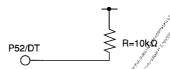


Figure 7 Tone Output Pin Load

- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of October, 1998. Specifications and information herein are subject to change without notice.