Ordering number : EN5996

CMOS IC

LC662104A, 662106A, 662108A

Four-Bit Single-Chip Microcontrollers with 4, 6, and 8 KB of On-Chip ROM

Overview

The LC662104A, LC662106A, and LC662108A are 4-bit CMOS microcontrollers that integrate on a single chip all the functions required in a special-purpose telephone controller, including ROM, RAM, I/O ports, a serial interface, a DTMF generator, timers, and interrupt functions. These microcontrollers are available in a 30-pin package.

Features and Functions

- On-chip ROM capacities of 4, 6, and 8 kilobytes, and an on-chip RAM capacity of 384 × 4 bits.
- Fully supports the LC66000 Series common instruction set (128 instructions). (The special-purpose instructions for TM1 and SI/01 are disabled.)
- I/O ports: 24 pins
- DTMF generator
  This microcontroller incorporates a circuit that can generate two sine wave outputs, DTMF output.
- 8-bit serial interface: one circuit
- Instruction cycle time: 0.95 to 10 µs (at 3.0 to 5.5 V)
- Powerful timer functions and prescalers
  — Time limit timer, event counter, pulse width measurement, and square wave output using a 12-bit timer.
  — Time base function using a 12-bit prescaler.
- Powerful interrupt system with 6 interrupt factors and 6 interrupt vector locations.
  — External interrupts: 3 factors/3 vector locations
  — Internal interrupts: 3 factors/3 vector locations
- Flexible I/O functions
  Selectable options include 20-mA drive outputs, pull-up and open drain circuits.
- Optional runaway detection function (watchdog timer)
- 8-bit I/O functions
- Power saving functions using halt and hold modes.
- Packages: DIP30SD, MFP30S
- Evaluation ICs: LC665099 (evaluation chip) + EVA86K - ECB662500
  LC66E2108(on-chip EPROM microcontroller)

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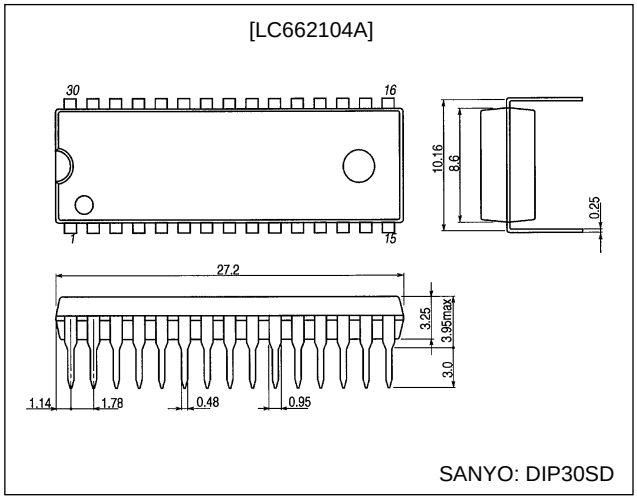
Package Dimensions

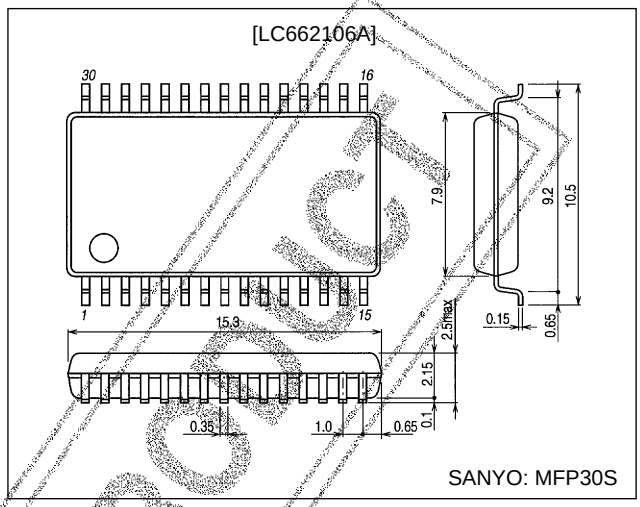
unit: mm

3196-DIP30SD

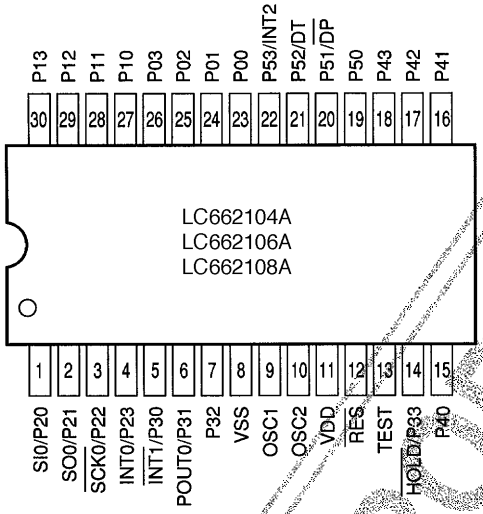


unit: mm

3216-MFP30S

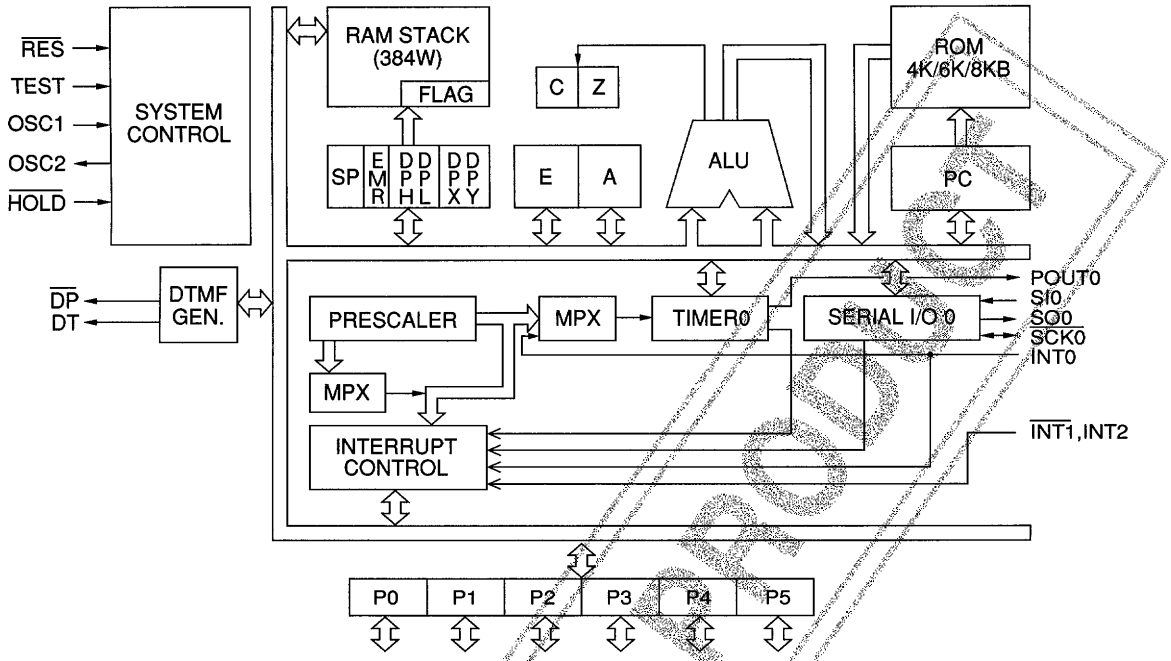


Type No.	No. of pins	ROM capacity	RAM capacity	Package		Features
LC66304A/306A/308A	42	4 K/6 K/8 KB	512 W	DIP42S	QFP48E	Normal versions 4.0 to 6.0 V/0.92 µs
LC66404A/406A/408A	42	4 K/6 K/8 KB	512 W	DIP42S	QFP48E	
LC66506B/508B/512B/516B	64	6 K/8 K/12 K/16 KB	512 W	DIP64S	QFP64A	
LC66354A/356A/358A	42	4 K/6 K/8 KB	512 W	DIP42S	QFP48E	Low-voltage versions 2.2 to 5.5 V/3.92 µs
LC66354S/356S/358S	42	4 K/6 K/8 KB	512 W		QFP44M	
LC66556A/558A/562A/566A	64	6 K/8 K/12 K/16 KB	512 W	DIP64S	QFP64E	
LC66354B/356B/358B	42	4 K/6 K/8 KB	512 W	DIP42S	QFP48E	Low-voltage high-speed versions 3.0 to 5.5 V/0.92 µs
LC66556B/558B/562B/566B	64	6 K/8 K/12 K/16 KB	512 W	DIP64S	QFP64E	
LC66354C/356C/358C	42	4 K/6 K/8 KB	512 W	DIP42S	QFP48E	2.5 to 5.5 V/0.92 µs
LC662104A/06A/08A	30	4 K/6 K/8 KB	384 W	DIP30SD	MFP30S	On-chip DTMF generator versions 3.0 to 5.5 V/0.95 µs
LC662304A/06A/08A/12A/16A	42	4 K/6 K/8 K/12 K/16 KB	512 W	DIP42S	QFP48E	
LC662508A/12A/16A	64	8 K/12 K/16 KB	512 W	DIP64S	QFP64E	
LC665304A/06A/08A/12A/16A	48	4 K/6 K/8 K/12 K/16 KB	512 W	DIP48S	QFP48E	Dual oscillator support 3.0 to 5.5 V/0.95 µs
LC66E308	42	EPROM 8 KB	512 W	DIC42S with window	QFC48 with window	Window and OTP evaluation versions 4.5 to 5.5 V/0.92 µs
LC66P308	42	OTPROM 8 KB	512 W	DIP42S	QFP48E	
LC66E408	42	EPROM 8 KB	512 W	DIC42S with window	QFC48 with window	
LC66P408	42	OTPROM 8 KB	512 W	DIP42S	QFP48E	
LC66E516	64	EPROM 16 KB	512 W	DIC64S with window	QFC64 with window	
LC66P516	64	OTPROM 16 KB	512 W	DIP64S	QFP64E	
LC66E2108	30	EPROM 8 KB	384 W			Window evaluation versions 4.5 to 5.5 V/0.95 µs
LC66E2316	42	EPROM 16 KB	512 W	DIC42S with window	QFC48 with window	
LC66E2516	64	EPROM 16 KB	512 W	DIC64S with window	QFC64 with window	
LC66E5316	52/48	EPROM 16 KB	512 W	DIC52S with window	QFC48 with window	
LC66P2108	30	OTPROM 8 KB	384 W	DIP30SD	MFP30S	OTP 4.0 to 5.5 V/0.95 µs
LC66P2316	42	OTPROM 16 KB	512 W	DIP42S	QFP48E	
LC66P2516	64	OTPROM 16 KB	512 W	DIP64S	QFP64E	
LC66P5316	48	OTPROM 16 KB	512 W	DIP48S	QFP48E	



We recommend the use of reflow-soldering techniques to solder-mount MFP packages.
Please consult with your Sanyo representative for details on process conditions if the package itself is to be directly immersed in a dip-soldering bath (dip-soldering techniques).

System Block Diagram



Differences between the LC663XX Series and the LC6621XX Series

Item	LC6630X Series (Including the LC66599 evaluation chip)	LC6635XB Series	LC6621XX Series
System differences • Hardware wait time (number of cycles) when hold mode is cleared	65536 cycles About 64 ms at 4 MHz (Tcyc = 1 µs)	16384 cycles About 16 ms at 4 MHz (Tcyc = 1 µs)	16384 cycles About 16 ms at 4 MHz (Tcyc = 1 µs)
• Value of timer 0 after a reset (Including the value after hold mode is cleared)	Set to FF0.	Set to FFC.	Set to FFC.
• DTMF generator	None (Tools are handled with external devices.)	None	Yes
• Inverter array	None (Tools are handled with external devices.)	None	None
• SIO1	Yes	Yes	None
• Three-value inputs/comparator inputs	Yes	Yes	None
• Three-state output from P31 and P32	None	None	Yes
• Using P0 to clear halt mode	In 4-bit groups	In 4-bit groups	Can be specified for each bit.
• External extended interrupts	None for INT3, INT4, and INT5. (Tools are handled with external devices.)	None for INT3, INT4, and INT5.	INT3, INT4, and INT5 can be used with the internal functions.
• Other P53 functions	Shared with $\overline{INT2}$ (Tools are handled with external devices.)	Shared with $\overline{INT2}$	Shared with INT2
Differences in main characteristics • Operating power-supply voltage and operating speed (cycle time)	• LC66304A/306A/308A 4.0 to 6.0 V/0.92 to 10 µs • LC66E308/P308 4.5 to 5.5 V/0.92 to 10 µs	• 3.0 to 5.5 V/0.92 to 10 µs • LC6635XA 2.2 to 5.5 V/3.92 to 10 µs 3.0 to 5.5 V/1.96 to 10 µs	3.0 to 5.5 V/0.95 to 10 µs
• Pull-up resistors	P0, P1, P4, and P5: about 3 to 10 kΩ	P0, P1, P4, and P5: about 3 to 10 kΩ	P0, P1, P4, and P5: about 100 kΩ
• Port voltage handling	• P2 to P6 and PC: 15V handling • P0, P1, PD, PE: Normal voltage handling	• P2 to P6 and PC: 15V handling • P0, P1, PD, PE: Normal voltage handling	P2 to P4, P51, and P53: 15V voltage handling Others: normal voltage handling

Pin Function Overview

Pin	I/O	Overview	Output driver type	Options	State after a reset
P00 P01 P02 P03	I/O	I/O ports P00 to P03 • Input or output in 4-bit or 1-bit units • P00 to P03 support the halt mode control function (This function can be specified in bit units.)	• Pch: Pull-up MOS type • Nch: Intermediate sink current type	• Pull-up MOS or Nch OD output • Output level on reset	High or low (option)
P10 P11 P12 P13	I/O	I/O ports P10 to P13 Input or output in 4-bit or 1-bit units	• Pch: Pull-up MOS type • Nch: Intermediate sink current type	• Pull-up MOS or Nch OD output • Output level on reset	High or low (option)
P20/SI0 P21/$\overline{SO0}$ P22/$\overline{SCK0}$ P23/INT0	I/O	I/O ports P20 to P23 • Input or output in 4-bit or 1-bit units • P20 is also used as the serial input SI0 pin. • P21 is also used as the serial output $\overline{SO0}$ pin. • P22 is also used as the serial clock $\overline{SCK0}$ pin. • P23 is also used as the INT0 interrupt request pin, and also as the timer 0 event counting and pulse width measurement input.	• Pch: CMOS type • Nch: Intermediate sink current type • Nch: +15V handling when OD option selected	CMOS or Nch OD output	H
P30/$\overline{INT1}$ P31/POUT0 P32	I/O	I/O ports P30 to P32 • Input or output in 3-bit or 1-bit units • P30 is also used as the $\overline{INT1}$ interrupt request. • P31 is also used for the square wave output from timer 0. • P31 and P32 also support 3-state outputs.	• Pch: CMOS type • Nch: Intermediate sink current type • Nch: +15V handling when OD option selected	CMOS or Nch OD output	H
P33/$\overline{HOLD}$	I	Hold mode control input • Hold mode is set up by the HOLD instruction when $\overline{HOLD}$ is low. • In hold mode, the CPU is restarted by setting $\overline{HOLD}$ to the high level. • This pin can be used as input port P33 along with P30 to P32. • When the P33/$\overline{HOLD}$ pin is at the low level, the CPU will not be reset by a low level on the $\overline{RES}$ pin. Therefore, applications must not set P33/$\overline{HOLD}$ low when power is first applied.			
P40 P41 P42 P43	I/O	I/O ports P40 to P43 • Input or output in 4-bit or 1-bit units • Input or output in 8-bit units when used in conjunction with P50 to P53. • Can be used for output of 8-bit ROM data when used in conjunction with P50 to P53.	• Pch: Pull-up MOS type • Nch: Intermediate sink current type • Nch: +15V handkling when OD option selected	• Pull-up MOS or Nch OD output • Output level on reset	High or low (option)

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Pin	I/O	Overview	Output driver type	Options	State after a reset
P50 P51/$\overline{DP}$ P52/DT P53/INT2	I/O	I/O ports P50 to P53 • Input or output in 4-bit or 1-bit units • P51 is also used for dial pulse output • P52 is also used for DTMF output • P53 is also used as the INT2 interrupt request.	• Pch: Pull-up MOS type • Nch: Intermediate sink current type • Nch: +15-V handling when OD option selected (P51 and P53 only)	• Pull-up MOS or Nch OD output • Output level on reset • Output level after a reset (An external pull-up resistor must be supplied when used for DT output.)	High or low (option)
OSC1 OSC2	I O	System clock oscillator connections When an external clock is used, leave OSC2 open and connect the clock signal to OSC1.		Ceramic oscillator or external clock selection	Option selection
$\overline{RES}$	I	System reset input When the P33/$\overline{HOLD}$ pin is at the high level, a low level input to the $\overline{RES}$ pin will initialize the CPU.			
TEST	I	CPU test pin This pin must be connected to V_{SS} during normal operation.			
V_{DD} V_{SS}		Power supply pins			

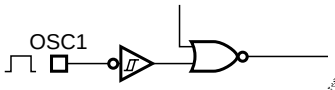
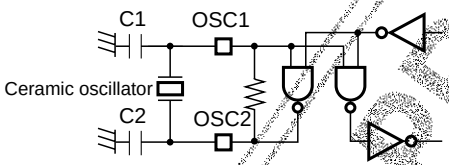
Note: Pull-up MOS type: The output circuit includes a MOS transistor that pulls the pin up to V_{DD}.
CMOS output: Complementary output.
OD output: Open-drain output.

User Options

1. Port 0, 1, 4, and 5 output level options a reset
   The output levels at reset for I/O ports 0, 1, 4, and 5 in independent 4-bit groups, can be selected from the following two options.

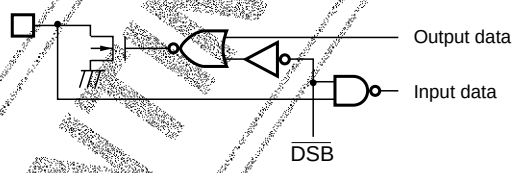
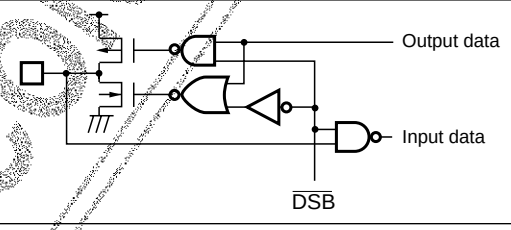
Option	Conditions and notes
Output high at reset	The four bits of ports 0, 1, 4, or 5 are set in a group
Output low at reset	The four bits of ports 0, 1, 4, or 5 are set in a group

2. Oscillator circuit options
   • Main clock

Option	Circuit	Conditions and notes
External clock		The input has Schmitt characteristics
Ceramic oscillator		

Note: There is no RC oscillator option.

3. Watchdog timer option
   A runaway detection function (watchdog timer) can be selected as an option.
4. Port output type options
   • The output type of each bit (pin) in ports P0, P1, P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P4, and P5 can be selected individually from the following two options.

Option	Circuit	Conditions and notes
Open-drain output		The port P2, P3, P5, and P6 inputs have Schmitt characteristics.
Output with built-in pull-up resistor		The port P2, P3, and P5 inputs have Schmitt characteristics. The CMOS outputs (ports P2 and P3) and the pull-up MOS outputs (P0, P1, P4, and P5) are distinguished by the drive capacity of the p-channel transistor.

LC662108 Series Option Data Area and Definitions

ROM area	Bit	Option specified		Option/data relationship
2000H	7	P5	Output level at reset	0 = high level, 1 = low level
	6	P4		
	5	Unused		This bit must be set to 0.
	4	Oscillator option		0 = (RC oscillator) external clock, 1 = ceramic oscillator
	3	Unused		This bit must be set to 0.
	2	P1	Output level at reset	0 = low level, 1 = high level
	1	P0		
	0	Watchdog timer option		0 = none, 1 = yes
2001H	7	P13	Output type	0 = OD, 1 = PU
	6	P12		
	5	P11		
	4	P10		
	3	P03	Output type	0 = OD, 1 = PU
	2	P02		
	1	P01		
	0	P00		
2002H	7	Unused		This bit must be set to 0.
	6	P32	Output type	0 = OD, 1 = PU
	5	P31		
	4	P30		
	3	P23	Output type	0 = OD, 1 = PU
	2	P22		
	1	P21		
	0	P20		
2003H	7	P53	Output type	0 = OD, 1 = PU
	6	P52		
	5	P51		
	4	P50		
	3	P43	Output type	0 = OD, 1 = PU
	2	P42		
	1	P41		
	0	P40		
2004H to 200CH	7	Unused		This bit must be set to 0. *: Location 2008H must be set to 7F.
	6			
	5			
	4			
	3			
	2			
	1			
	0			
200DH	7	Reserved. Must be set to predefined values.		This data is generated by the assmbler (21). If the assembler is not used, set this data to 00.
	6			
	5			
	4			
	3			
	2			
	1			
	0			
200EH	7	Reserved. Must be set to predefined values.		This data is generated by the assmbler (0x). If the assembler is not used, set this data to 00.
	6			
	5			
	4			
	3			
	2			
	1			
	0			

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ROM area	Bit	Option specified	Option/data relationship
200FH	7	Reserved. Must be set to predefined values.	This data is generated by the assmbler (00). If the assembler is not used, set this data to (00).
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit	Note
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V	
Input voltage	$V_{IN}1$	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P4, P51, and P53	–0.3 to +15.0	V	1
	$V_{IN}2$	All other inputs	–0.3 to V_{DD} + 0.3	V	2
Output voltage	$V_{OUT}1$	P2 and P3 (except for the P33/$\overline{HOLD}$ pin)	–0.3 to +15.0	V	1
	$V_{OUT}2$	All other inputs	–0.3 to V_{DD} + 0.3	V	2
Output current per pin	$I_{ON}1$	P0, P1, P2, P3 (except for the P33/$\overline{HOLD}$ pin), P4, P5	20	mA	3
	$-I_{OP}1$	P0, P1, P4, P5	2	mA	4
	$-I_{OP}2$	P2, P3 (except for the P33/$\overline{HOLD}$ pin)	4	mA	4
Total pin current	$\Sigma I_{ON}1$	P1, P2, P3 (except for the P33/$\overline{HOLD}$ pin)	75	mA	3
	$\Sigma I_{ON}2$	P0, P4, P5	75	mA	3
	$\Sigma I_{OP}1$	P1, P2, P3 (except for the P33/$\overline{HOLD}$ pin)	25	mA	4
	$\Sigma I_{OP}2$	P0, P4, P5	25	mA	4
Allowable power dissipation	Pd max	Ta = –30 to +70°C: DIP30S (MFP30S)	340 (200)	mW	5
Operating temperature	Topr		–30 to +70	°C	
Storage temperature	Tstg		–55 to +125	°C	

Note: 1. Applies to pins with open-drain output specifications. For pins with other than open-drain output specifications, the ratings in the pin column for that pin apply.
2. For the oscillator input and output pins, levels up to the free-running oscillation level are allowed.
3. Sink current
4. Source current
5. We recommend the use of reflow soldering techniques to solder mount MFP packages.
Please consult with your Sanyo representative for details on process conditions if the package itself is to be directly immersed in a dip-soldering bath (dip-soldering techniques).

Allowable Operating Ranges at Ta = –30 to +70°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit	Note
			min	typ	max		
Operating supply voltage	V_{DD}	V_{DD}	3.0		5.5	V	
Memory retention supply voltage	$V_{DD}H$	V_{DD}: During hold mode	1.8		5.5	V	
Input high-level voltage	$V_{IH}1$	P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P4, P51, and P53: N-channel output transistor off	0.8 V_{DD}		13.5	V	1
	$V_{IH}2$	P33/$\overline{\text{HOLD}}$, $\overline{\text{RES}}$, OSC1: N-channel output transistor off	0.8 V_{DD}		V_{DD}	V	
	$V_{IH}3$	P0, P1, P50, P52: N-channel output transistor off	0.8 V_{DD}		V_{DD}	V	
Input low-level voltage	$V_{IL}1$	P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), RES, and OSC1: N-channel output transistor off	V_{SS}		0.2 V_{DD}	V	2
	$V_{IL}2$	P33/$\overline{\text{HOLD}}$: V_{DD} = 1.8 to 5.5 V	V_{SS}		0.2 V_{DD}	V	
	$V_{IL}3$	P0, P1, P4, P5, TEST: N-channel output transistor off	V_{SS}		0.2 V_{DD}	V	
Operating frequency (instruction cycle time)	fop (Tcyc)		0.4 (10)		4.20 (0.95)	MHz (µs)	
[External clock input conditions]							
Frequency	f_{ext}	OSC1: Defined by Figure 1. Input the clock signal to OSC1 and leave OSC2 open. (External clock input must be selected as the oscillator circuit option.)	0.4		4.20	MHz	
Pulse width	t_{extH}, t_{extL}		100			ns	
Rise and fall times	t_{extR}, t_{extF}				30	ns	

Note: 1. Applies to pins with open-drain specifications. However, $V_{IH}2$ is applied to the P33/$\overline{\text{HOLD}}$ pin. When ports P2 and P3 have CMOS output specifications they cannot be used as input pins.
2. Applies to pins with open-drain specifications.

Electrical Characteristics at Ta = –30 to +70°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V unless otherwise specified.

Parameter		Symbol	Conditions		Ratings min	Ratings typ	Ratings max	Unit	Note
Input high-level current		$I_{IH}1$	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P4, P51, and P53: V_{IN} = 13.5 V, with the output Nch transistor off				5.0	µA	1
		$I_{IH}2$	P0, P1, P50, P52, OSC1, $\overline{RES}$, and P33/$\overline{HOLD}$: V_{IN} = V_{DD}, with the output Nch transistor off				1.0	µA	1
Input low-level current		$I_{IL}1$	P0, P1, P2, P3, P4, and P5: V_{IN} = V_{SS}, with the output Nch transistor off		–1.0			µA	2
Output high-level voltage		$V_{OH}1$	P2, P3 (except for the P33/$\overline{HOLD}$ pin)	I_{OH} = –1 mA	V_{DD} – 1.0			V	3
				I_{OH} = –0.1 mA	V_{DD} – 0.5				
Value of the output pull-up resistor		R_{PO}	P0, P1, P4, P5		30	100	150	kΩ	
Output low-level voltage		$V_{OL}1$	P0, P1, P2, P3, P4, and P5 (except for the P33/$\overline{HOLD}$ pin): I_{OL} = 1.6 mA				0.4	V	5
		$V_{OL}2$	P0, P1, P2, P3, P4, and P5 (except for the P33/$\overline{HOLD}$ pin): I_{OL} = 8 mA				1.5	V	
Output off leakage current		$I_{OFF}1$	P2, P3, P4, P51, and P53: V_{IN} = 13.5 V				5.0	µA	6
		$I_{OFF}2$	Does not apply to P2, P3, P4, P51, and P53: V_{IN} = V_{DD}				1.0	µA	6
[Schmitt characteristics]									
Hysteresis voltage		V_{HYS}	P2, P3, P4, P5, and $\overline{RES}$			0.1 V_{DD}			
High-level threshold voltage		Vt_H			0.5 V_{DD}		0.8 V_{DD}	V	
Low-level threshold voltage		Vt_L			0.2 V_{DD}		0.5 V_{DD}	V	
[Ceramic oscillator]									
Oscillator frequency		f_{CF}	OSC1, OSC2: See Figure 2. 4 MHz			4.0		MHz	
Oscillator stabilization time		f_{CFS}	See Figure 3. 4 MHz				10.0	ms	
[Serial clock]									
Cycle time	Input	t_{CKCY}	$\overline{SCK0}$: With the timing of Figure 4 and the test load of Figure 5.		0.9			µs	
	Output				2.0			Tcyc	
Low-level and high-level pulse widths	Input	t_{CKL}			0.4			µs	
	Output	t_{CKH}			1.0			Tcyc	
Rise an fall times	Output	t_{CKR}, t_{CKF}					0.1	µs	
[Serial input]									
Data setup time		t_{ICK}	SI0: With the timing of Figure 4. Stipulated with respect to the rising edge (↑) of $\overline{SCK0}$.		0.3			µs	
Data hold time		t_{CKI}			0.3			µs	
[Serial output]									
Output delay time		t_{CKO}	SO0: With the timing of Figure 4 and the test load of Figure 5. Stipulated with respect to the falling edge (↓) of $\overline{SCK0}$.				0.3	µs	
[Pulse conditions]									
INT0 high and low-level		t_{IOH}, t_{IOL}	INT0: Figure 6, conditions under which the INT0 interrupt can be accepted, conditions under which the timer 0 event counter or pulse width measurement input can be accepted		2			Tcyc	
High and low-level pulse widths for interrupt inputs other than INT0		t_{IIH}, t_{IIL}	$\overline{INT1}$, INT2: Figure 6, conditions under which the corresponding interrupt can be accepted		2			Tcyc	
$\overline{RES}$ high and low-level pulse widths		t_{RSH}, t_{RSL}	$\overline{RES}$: Figure 6, conditions under which reset can be applied.		3			Tcyc	
Operating current drain		$I_{DD\,OP}$	V_{DD}: 4-MHz ceramic oscillator			4.5	8.0	mA	8
			V_{DD}: 4-MHz external clock			4.5	8.0	mA	
Halt mode current drain		I_{DDHALT}	V_{DD}: 4-MHz ceramic oscillator			2.5	5.5	mA	
			V_{DD}: 4-MHz external clock			2.5	5.5	mA	
Hold mode current drain		I_{DDHOLD}	V_{DD}: V_{DD} = 1.8 to 5.5 V			0.01	10	µA	

Note: 1. With the output Nch transistor off in shared I/O ports with the open-drain output specifications. These pins cannot be used as input pins if the CMOS output specifications are selected.
2. With the output Nch transistor off in shared I/O ports with the open-drain output specifications. The rating for the pull-up output specification pins is stipulated in terms of the output pull-up current IPO. These pins cannot be used as input pins if the CMOS output specifications are selected.
3. With the output Nch transistor off for CMOS output specification pins.
4. With the output Nch transistor off for pull-up output specification pins.
6. With the output Pch transistor off for open-drain output specification pins.
7. Reset state

Tone (DTMF) Output Characteristics

DC Characteristics at Ta = –30 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Tone output voltage	V_{T1}	DT: Single tone, V_{DD} = 3.5 to 5.5 V*	0.9	1.3	2.0	Vp-p
Row/column tone output voltage ratio	D_{BCR1}	DT: Dual tones, V_{DD} = 3.5 to 5.5 V*	1.0	2.0	3.0	dB

Note*: See Figure 7.

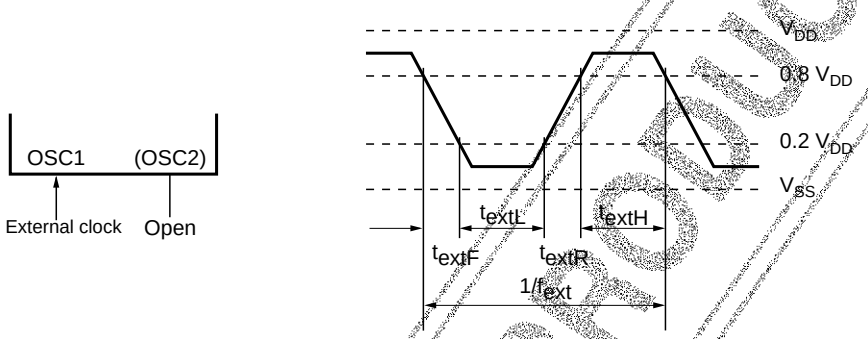

Figure 1 External Clock Input Waveform

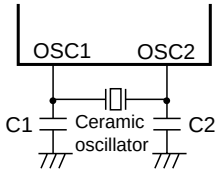

Figure 2 Ceramic Oscillator Circuit

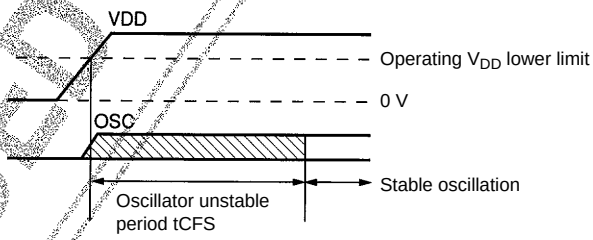

Figure 3 Oscillator Stabilization Period

Table 1 Recomended Ceramic Oscillator Constants

External capacitor type		Built-in capacitor type
4 MHz (Murata Mfg. Co., Ltd.) CSA4.00MG	C1 = 33 pF C2 = 33 pF	4 MHz (Murata Mfg. Co., Ltd.) CST4.00MG
4 MHz (Kyocera Corporation) KBR4.0MSB	C1 = 33 pF C2 = 33 pF	4 MHz (Kyocera Corporation) KBR4.0MKC

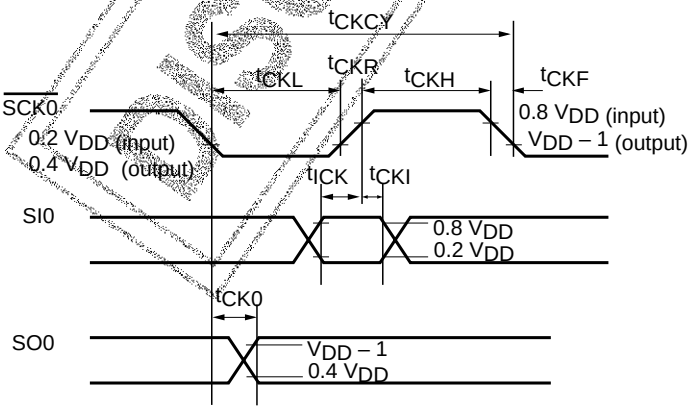

Figure 4 Serial I/O Timing

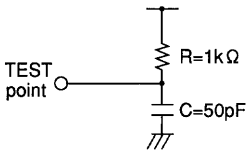

Figure 5 Timing Load

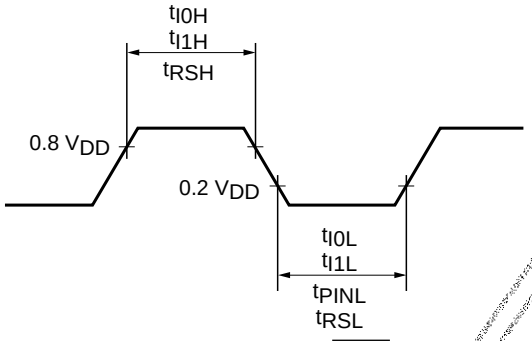

Figure 6 Input Timing for the INT0, INT1, INT2, and $\overline{RES}$ pins

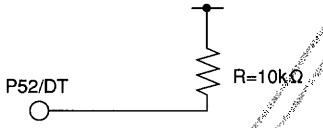

Figure 7 Tone Output Pin Load