3.3V CMOS 20-BIT BUFFER

IDT74FCT163827A/C

FEATURES:

- **0.5 MICRON CMOS Technology**
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **V_{CC} = 3.3V ± 0.3V, Normal Range, or V_{CC} = 2.7V to 3.6V, Extended Range**
- **CMOS power levels (0.4µ W typ. static)**
- **Rail-to-rail output swing for increased noise margin**
- **Low Ground Bounce (0.3V typ.)**
- **Inputs (except I/O) can be driven by 3.3V or 5V components**
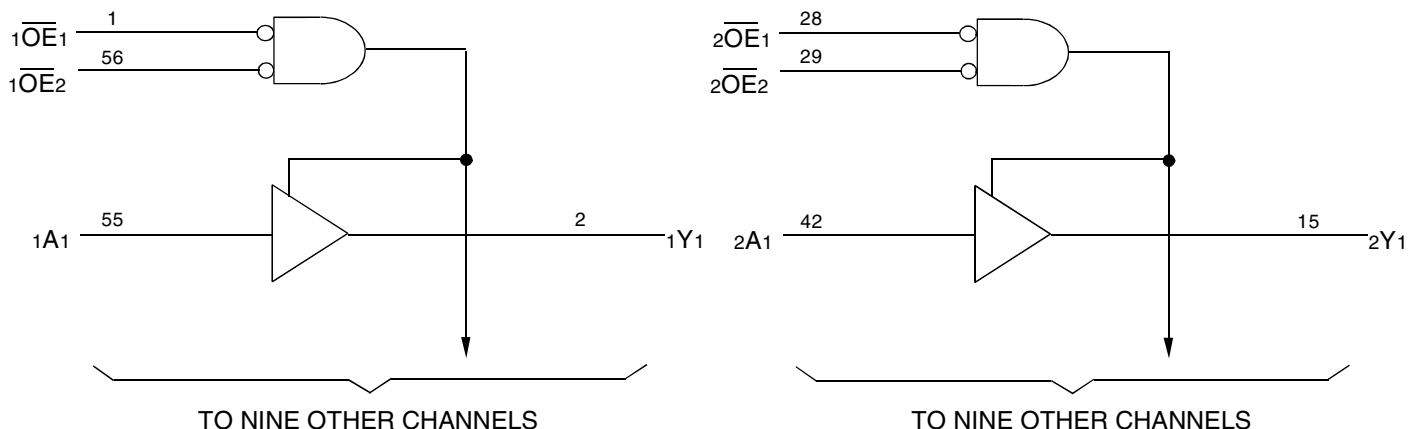- **Available in SSOP and TSSOP packages**

DESCRIPTION:

The FCT163827 20-bit buffer is built using advanced dual metal CMOS technology. These 20-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or busses carrying parity. Two pairs of NAND-ed output enable controls offer maximum control flexibility and are organized to operate the device as two 10-bit buffers or one 20-bit buffer. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.
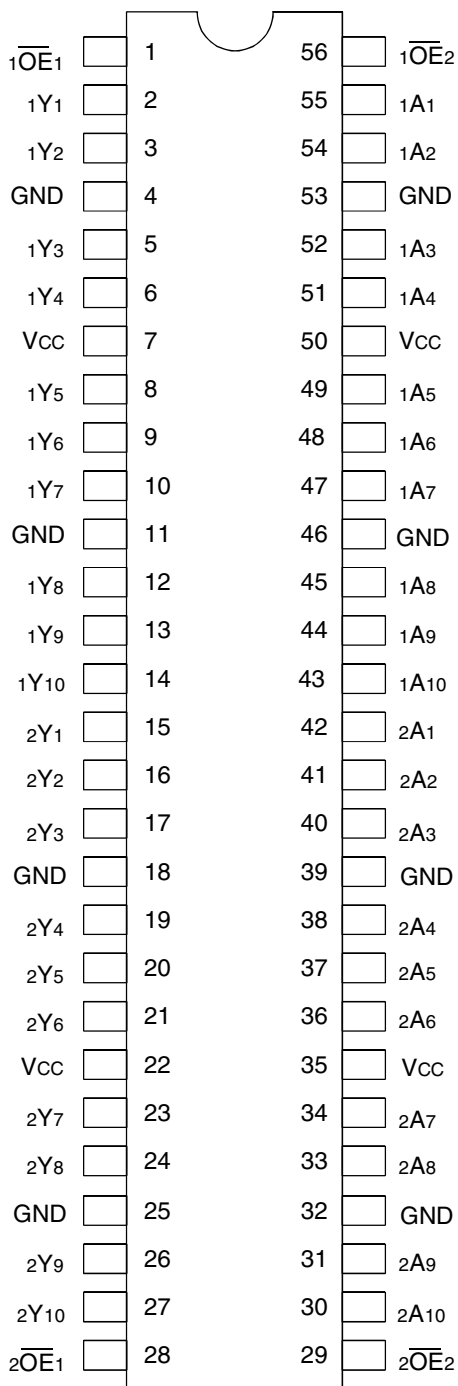
The FCT163827 has series current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times, reducing the need for external series terminating resistors.

The inputs of the FCT163827 can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

FUNCTIONAL BLOCK DIAGRAM

TO NINE OTHER CHANNELS

TO NINE OTHER CHANNELS

INDUSTRIAL TEMPERATURE RANGE

MAY 2002

DSC-3083/6

PIN CONFIGURATION

1$\overline{OE}_1$	1		56	1$\overline{OE}_2$
1Y1	2		55	1A1
1Y2	3		54	1A2
GND	4		53	GND
1Y3	5		52	1A3
1Y4	6		51	1A4
VCC	7		50	VCC
1Y5	8		49	1A5
1Y6	9		48	1A6
1Y7	10		47	1A7
GND	11		46	GND
1Y8	12		45	1A8
1Y9	13		44	1A9
1Y10	14		43	1A10
2Y1	15		42	2A1
2Y2	16		41	2A2
2Y3	17		40	2A3
GND	18		39	GND
2Y4	19		38	2A4
2Y5	20		37	2A5
2Y6	21		36	2A6
VCC	22		35	VCC
2Y7	23		34	2A7
2Y8	24		33	2A8
GND	25		32	GND
2Y9	26		31	2A9
2Y10	27		30	2A10
2$\overline{OE}_1$	28		29	2$\overline{OE}_2$

SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to 7	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	−0.5 to VCC+0.5	V
T_{STG}	Storage Temperature	−65 to +150	°C
I_{OUT}	DC Output Current	−60 to +60	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Outputs and I/O terminals.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
x$\overline{OE}$x	Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

FUNCTION TABLE[1]

Inputs			Outputs
x$\overline{OE}_1$	x$\overline{OE}_2$	xAx	xYx
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2	—	5.5	V
	Input HIGH Level (I/O pins)			2	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±1	
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±1	μA
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	μA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}-0.2	—	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3	—	V
		V_{CC} = 3V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA	2.4[5]	3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	V
		V_{CC} = 3V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.1	10	μA

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC}–0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. $V_{IN} = V_{CC}$ - 0.6V[3]		—	2	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}1 = x\overline{OE}2$ = GND One Input Togging 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max.,Outputs Open f_I = 10MHz 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	0.5	0.7	mA
		$x\overline{OE}1 = x\overline{OE}2$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	—	0.5	0.8	
		V_{CC} = Max.,Outputs Open f_I = 2.5MHz 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	2.5	3.7[5]	
		$x\overline{OE}1 = x\overline{OE}2$ = GND Twenty Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	—	2.5	4.1[5]	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input. All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}N_{CP}/2 + f_iN_i)$

   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})

   ΔI_{CC} = Power Supply Current for a TTL High Input

   D_H = Duty Cycle for TTL Inputs High

   N_T = Number of TTL Inputs at D_H

   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

   N_{CP} = Number of Clock Inputs at f_{CP}

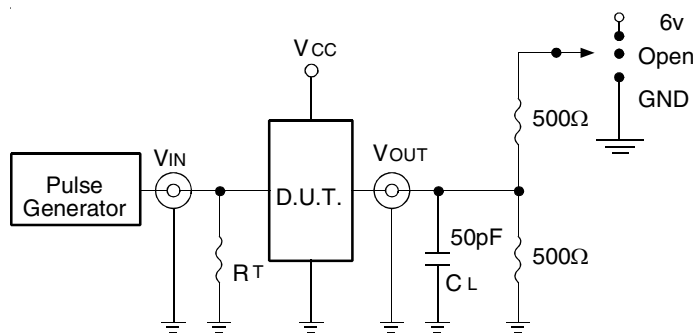 f_i = Input Frequency

   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[1]

Symbol	Parameter	Condition[2]	FCT163827A		FCT163827C		Unit
			Min.[3]	Max.	Min.[3]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	$C_L = 50pF$ $R_L = 500\Omega$	1.5	8	1.5	4.4	ns
		$C_L = 300pF^{(4)}$ $R_L = 500\Omega$	1.5	15	1.5	10	
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$x to xYx	$C_L = 50pF$ $R_L = 500\Omega$	1.5	12	1.5	7	ns
		$C_L = 300pF^{(4)}$ $R_L = 500\Omega$	1.5	23	1.5	14	
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$x to xYx	$C_L = 5pF^{(4)}$ $R_L = 500\Omega$	1.5	9	1.5	5.7	ns
		$C_L = 50pF$ $R_L = 500\Omega$	1.5	10	1.5	6	
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3V \pm 0.3V$, Normal Range. For $V_{CC} = 2.7V$ to $3.6V$, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
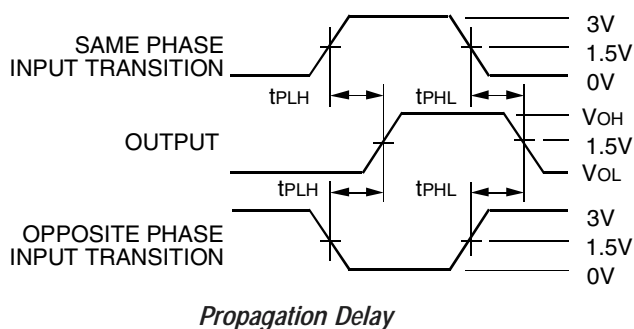
TEST CIRCUITS AND WAVEFORMS

Test Circuits for All Outputs
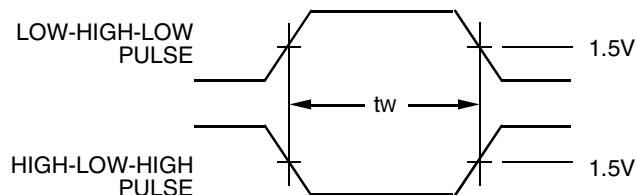

Set-up, Hold, and Release Times
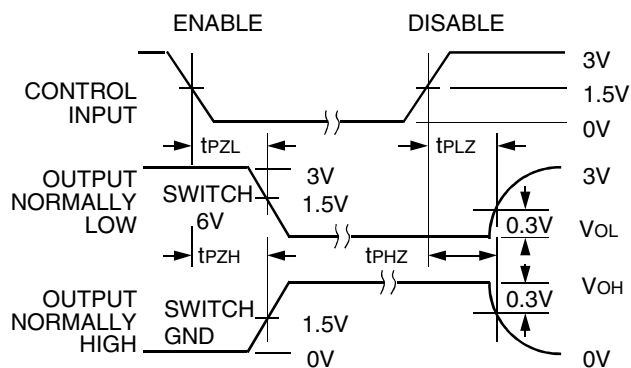

Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
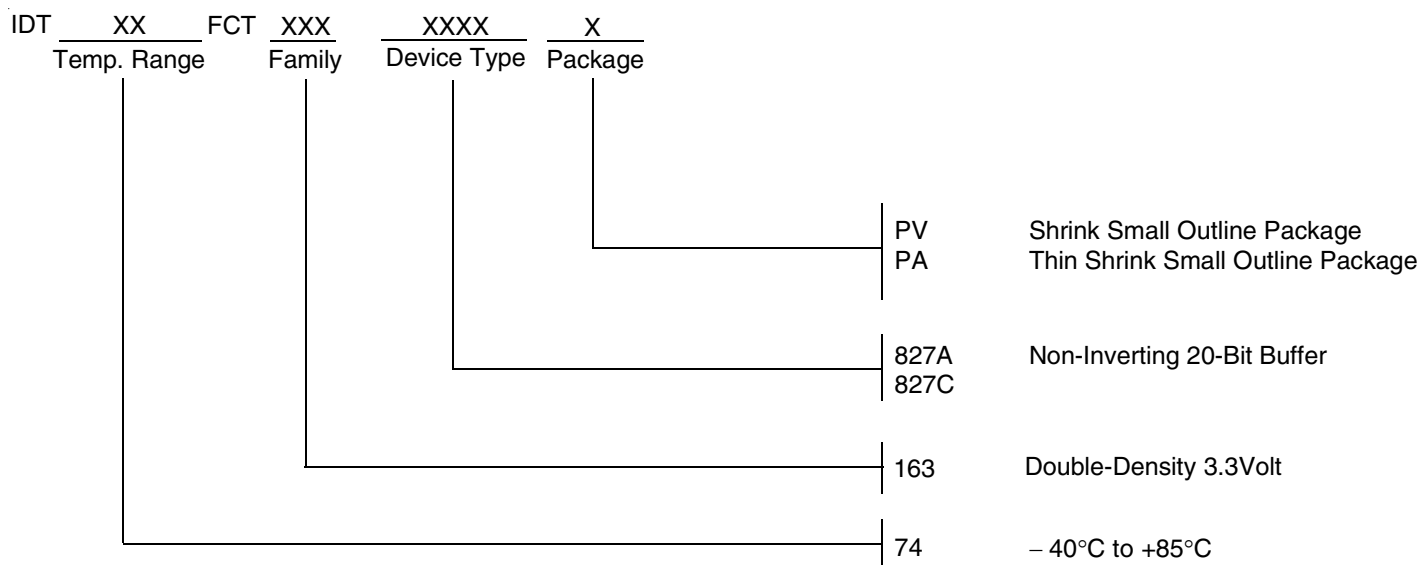

Pulse Width

Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. if V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

ORDERING INFORMATION

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IDT     XX      FCT   XXX      XXXX        X
     Temp. Range    Family   Device Type  Package
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PV   Shrink Small Outline Package
PA   Thin Shrink Small Outline Package

827A   Non-Inverting 20-Bit Buffer
827C

163   Double-Density 3.3Volt

74     $-40°C$ to $+85°C$

DATA SHEET DOCUMENT HISTORY

4/19/2002   Removed B speed grade
5/21/2002   Removed TVSOP package