

SYNCHRONOUS BURST SRAM FLOW-THROUGH

128K x 32 SRAM

+3.3V SUPPLY WITH CLOCKED,
REGISTERED INPUTS, BURST COUNTER

FEATURES

- Fast access times: 10 and 11ns
- Fast clock speed: 83 MHz
- Provide high performance 2-1-1-1 access rate
- Fast OE# access times: 5.0ns
- 3.3V -5% and +10% power supply
- Separate isolated output buffer supply compatible with 3.3V and 2.5V I/O (VCCQ): 2.375V to 3.6V
- 5V tolerant inputs except I/O's
- Clamp diodes to VSSQ at all inputs and outputs
- Common data inputs and data outputs
- BYTE WRITE ENABLE and GLOBAL WRITE control
- Three chip enables for depth expansion and address pipeline
- Address, data and control registers
- Internally self-timed WRITE CYCLE
- Burst control pins (interleaved or linear burst sequence)
- Automatic power-down for portable applications
- High density, high speed packages

OPTIONS

- Timing
 - 10ns access/12ns cycle
 - 11ns access/12ns cycle
- Packages
 - 100-pin TQFP

MARKING

-10
-11

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GENERAL DESCRIPTION

The Galvantech Synchronous Burst SRAM family employs high-speed, low power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high valued resistors.

The GVT71128B32 SRAM integrates 131,072x32 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable (CE#), depth-expansion chip enables (CE2# and CE2), burst control inputs (ADSC#, ADSP#, and ADV#), write enables (BW1#, BW2#, BW3#, BW4#, and BWE#), and global write (GW#).

Asynchronous inputs include the output enable (OE#), burst mode control (MODE), and sleep mode control (ZZ). The data outputs (Q), enabled by OE#, are also asynchronous.

Addresses and chip enables are registered with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

Address, data inputs, and write controls are registered on-chip to initiate self-timed WRITE cycle. WRITE cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. BW1# controls DQ1-DQ8. BW2# controls DQ9-DQ16. BW3# controls DQ17-DQ24. BW4# controls DQ25-DQ32. BW1#, BW2# BW3#, and BW4# can be active only with BWE# being LOW. GW# being LOW causes all bytes to be written.

The GVT71128B32 operates from a +3.3V core power supply and all outputs operate on a +2.5V supply. All inputs and outputs are JEDEC standard JESD8-5 compatible. The device is ideally suited for 486, Pentium™, 680x0, and PowerPC™ systems and for systems that are benefited from a wide synchronous data bus.