

CDB5451-1

# CDB5451-1 Evaluation Board and Software

### Features

- Direct Shunt Sensor and Current Transformer Interface for 3-Phase Power
- On-board Voltage Reference
- Supported by CDBCAPTURE+
  - RS-232 Serial Communication with PC
- Lab Windows/CVI<sup>™</sup> Evaluation Software
  - "Real-Time" RMS calculation
  - FFT Analysis
  - Time Domain Analysis
  - Noise Histogram Analysis

# **General Description**

The CDB5451-1 is an inexpensive tool designed to evaluate the functionality and performance of the CS5451. The CS5451 Data Sheet is required in conjunction with the CDB5451 Evaluation Board. The CDB5451-1 Evaluation Board requires use of a CDBCapture+ Board (also available from Cirrus Logic).

The CDB5451-1 includes a voltage reference, a digital level-shifter for interface to the CDBCAPTURE+ Board, and voltage regulator which allows for optional +5 V supply operation. The CDBCAPTURE+ accepts the serial output data from the evaluation board and communicates this to the PC via the firmware, enabling quick and easy access to the CS5451 output.

The CDB5451-1 includes PC software, allowing the user to perform for data capture (includes option for time domain analysis, histogram analysis, and frequency domain analysis). Real-Time RMS calculation/analysis can be performed on one voltage/current channel pair at a time.

ORDERING INFORMATION CDB5451-1

**Evaluation Board** 



Preliminary Product Information

This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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# **1. INTRODUCTION**

The CDB5451-1 Evaluation Board operates in conjunction with the Cirrus Logic CDBCAPTURE+ Board. The CS5451, CDB5451-1, and CDBCAP-TURE+ data sheets should be read thoroughly and understood before using the CDB5451-1 Evaluation Board.

The CDB5451-1 evaluation board provides a quick means of evaluating the CS5451. The CDB5451-1 interfaces to the CDBCAPTURE+ board. The CD-BCAPTURE+ board then interfaces to an IBM<sup>™</sup> compatible PC via an RS-232 interface. Analysis software supplied with the CDB5451-1 provides a means to display the performance of the CS5451 in the time domain or frequency domain.

# 1.1 CS5451

The CS5451 is a highly integrated six-channel Delta-Sigma Analog-to-Digital Converter (ADC) developed for the Power Metering Industry. The CS5451 combines six delta-sigma modulators with decimation filters, along with a master-mode serial interface on a single chip device. The CS5451 was designed with the intention of being able to perform as the A/D converter and analog front-end of a 3-phase power metering system. The six ADC channels can be thought of as three pairs of voltage/current-channel ADC's in a digital 3-phase power metering system. However the CS5451 has other potential uses, particularly in motor/servo control applications which require very high precision.

The CS5451 contains one three-channel programmable gain amplifier (PGA) for the three current input channels. The PGA sets the maximum input levels of the all three current channels at  $\pm$ 800 mV DC (for GAIN = 1) or  $\pm$  0 mV DC (for GAIN = 20). The voltage channel has only the x1 gain setting, and so the input levels on the voltage channel range is  $\pm$ -800 mV DC.

Additional features of CS5451 include a charge pump driver, on-chip 1.2 V reference, and a digital input that can select between two different output word rates. (The two output word rates are equal to XIN/2048 and XIN/1024.)

The CS5451 requires a 1.2 V reference input on VREFIN. The  $\Delta\Sigma$  modulators and high rate digital filters allow the user to measure instantaneous voltage and current at an output word rate of 3906 Hz (or 1953 Hz, depending on the state of the OWRS pin) when a 4.000 MHz clock source is used.

# **1.2 Data Flow on Evaluation Board**

The serial data from the CS5451 is sent through the 10-pin ribbon cable to the CDBCAPTURE+ Board. The data is shifted into parallel format by the CDBCAPTURE+ board, and is stored into SRAM memory. Calculations may be performed on the data before it is sent to the PC via the RS-232 cable, where it can be displayed on the LabWindows screens for viewing.

The software interface includes options for viewing a time-domain representation of the sampled waveform, from any one of the six A/D channels. Assuming that the number of samples taken is a whole-number power of 2, an FFT can be performed on the samples for spectral analysis. Histogram analysis can also be performed. The program also has an option to run a real-time rms calculation on one of the three voltage-/current-channel pairs. The resulting energy over each 'computation cycle' is also calculated. These results may be saved to file by the user, to allow for additional performance analysis and/or data processing.



# 2. HARDWARE

### 2.1 Evaluation Board Description

The CDB5451-1 board supplies power to the CS5451, provides six channels of analog input, and provides the six-channel A/D serial output data for further analysis. All of the actual data manipulation and calculations are performed by the DSP on the CDBCAPTURE+ Board, and by the LabWindows software. The following discussion introduces the various sections of the board.

# 2.2 Connecting the Boards

Three different cables are needed. The CDB5451-1 comes shipped with one cable: a 20-pin ribbon bus cable. The user should also have one RS-232 cable and one 10-pin ribbon bus cable that are supplied with the CDBCAPTURE+ board.

A simple connection diagram is shown in Figure 1. The evaluation board interfaces to the CDBCAP-TURE+ board through a 10-pin bus cable, as well as through a 20-pin bus cable. The user must make



**Figure 1. Connection Diagram** 

![](_page_5_Picture_0.jpeg)

sure that these cables are connected to the boards in the correct orientation.

Referring to Figure 1, first attach the 10-pin bus cable to "HDR1" on the CDBCAPTURE+ board such that the ribbon is extending away from the edge of the board. Connect the other end of this cable to "HDR16" on the CDB5451-1 board. Again make sure that the ribbon is extending outward from the CDB5451-1 board. Next connect the 20pin ribbon cable to "J18" on the CDBCAPTURE+ board, and connect the other end to "J17" on the CDB5451-1 board. Again, for both connections, make sure that the cable leads extend outward, away from the board. Finally, the RS-232 cable is shown connecting the CDBCAPTURE+ Board to the user's PC. The user should connect the RS-232 cable to an available COM port on the PC.

# **2.3 Power Supply Connections**

The CDB5451-1 can be used in several different power supply configurations. Table 1 shows the various possible power connections with the required jumper settings. There are various +3 V and +5 V options.

# 2.3.1 Analog Power Supply

Referring to Figure 2, the A+ post supplies power to the positive analog power input pin (VA+) of the CS5451. This post also supplies power to the LT1004 voltage reference (D3) and the optional

Power	Supplies	Power Post Connections							
Analog	Digital	A+	A-	GND	D+	+5 V	HDR9	HDR17	HDR18
+3	+3	+3	-2	0	+3	NC	A-	+5V_IN O O A+ (	VD+ 000 V+ 0 0
+3	+3	+3	-2	0	NC	NC	A-	+5V_IN O O A+	VD+OO V+
+3	+3	+3	NC	0	+3	NC	A- O O CPD ====	+5V_IN O O A+	VD+ 0-0 V+ 0 0
+3	+3	+3	NC	0	NC	NC	A- O O CPD CPD	+5V_IN O O A+	VD+OO V+
+3	+3	NC	-2	0	NC	+5	A-	+5V_IN A+ 0 0	VD+OO V+OO
+3	+3	NC	NC	0	NC	+5	A- O O CPD -	+5V_IN	VD+OO V+
+3	+5	+3	-2	0	+5	NC	A-	+5V_IN O O A+	VD+ <b>O</b> V+ O O
+3	+5	+3	NC	0	+5	NC	A- O O CPD 🗪	+5V_IN O O A+ G	VD+ 000 V+ 0 0
+3	+5	NC	-2	0	+5	+5	A-	+5V_IN A+ 0 0	VD+ 000 V+ 0 0
+3	+5	NC	NC	0	+5	+5	A- O O CPD	+5V_IN	VD+ <b>0</b> V+ O O
+5	+3	+5	0	+2	+5	NC	A-	+5V_IN O O A+ <b>G</b>	VD+ 0-0 V+ 0 0

**Table 1. Power Supply Connections** 

![](_page_6_Picture_1.jpeg)

+3V regulator (U5). If HDR9 is set to the "A-" setting, the A- post can supply the required negative voltage to the VA- pin of the CS5451.

Note that the evaluation board is equipped with a LM317 voltage regulator (U5), set to create +3 V from a +5 V supply. This option is useful if the user has only one power supply which must be used to power both the CDBCAPTURE+ and CDB5451-1 board. With HDR17 set to "+5V\_IN", one single +5 V supply can be used to provide both the +5 V power for the CDBCAPTURE+ Board, as well as +3 V for the CDB5451-1 board.

# 2.3.2 Digital Power Supply

The A+ post can be used to supply both the analog power (to CS5451 VA+ pin) as well as the digital power (to CS5451 VD+ pin). However if a separate supply voltage is desired for the digital power supply, the "VD+" banana connector post can be used to independently supply digital power to the input of the CS5451 (VD+ pin), the 4.000 MHz oscillator (U1), and tri-state buffer (U3). This is controlled by setting on HDR18.

# 2.3.3 Charge Pump Options

The output from CS5451's charge-pump driver pin (CPD) can be used to generate a -2V supply when the proper jumper settings are selected. The -2 V can be used as the negative power supply connection to the VA- pin. Referring to Figure 2, circuitry for a charge-pump circuit is included on-board. The charge pump circuit consists of capacitors C11, C12, and C36, and diodes D1 and D2.

As an alternative to using the charge pump circuit, the user can supply an off-board -2V DC power source to the "A-" banana connector. This option is controlled by switching HDR9.

# 2.4 Eval Board Control - Headers/Switches

Table 2 lists the various adjustable headers and switches on the CDB5451-1 Evaluation Board, as well as their default settings (as shipped from the factory). The header settings can be adjusted by the user to select various options on the evaluation board.

Name	Function Description	Default Setting	Default Jumpers
HDR1	Used to switch IIN3+ on the CS5451 between J2 and AGND.	IIN3+ Set to BNC J2	O O AGND
HDR2	Used to switch VIN3- on the CS5451 between J3 and AGND.	VIN3- Set to BNC J3	O O VIN3- AGND
HDR3	Used to switch VIN3+ on the CS5451 between J1 and AGND.	VIN3- Set to BNC J1	O O AGND
HDR4	Used to switch IIN3- on the CS5451 between J4 and AGND.	IIN3- Set to BNC J4	O O IIN3- Geographic Agnd
HDR5	Used to switch VIN2- on the CS5451 between J6 and AGND.	VIN2- Set to BNC J6	O O VIN2- Gene Agnd
HDR6	Used to switch IIN2+ on the CS5451 between J7 and AGND.	IIN2+ Set to BNC J7	O O AGND

Table 2. Defa	ult Header	Settings
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![](_page_7_Picture_0.jpeg)

Name	Function Description	Default Setting	Default Jumpers	
HDR7	Used to switch IIN2- on the CS5451 between J5 and AGND.	IIN2+ Set to BNC J5	O O IIN2- General Agnd	
HDR8	Used to switch VIN2+ on the CS5451 between J8 and AGND.	VIN2+ Set to BNC J8	O O AGND	
HDR9	Used to switch between external VA- and on-board CS5451 charge-pump circuit, CPD	CPD active	A- O O CPD G	
HDR10	Used to switch VIN1+ on the CS5451 between J9 and AGND.	VIN1+ Set to BNC J9	O O AGND	
HDR11	Used to switch IIN1- on the CS5451 between J12 and AGND.	IIN1- Set to BNC J12	O O IIN1- AGND	
HDR12	Used to switch IIN1+ on the CS5451 between J10 and AGND.	IIN1- Set to BNC J10	O O AGND	
S1	S1 settings valid ONLY when J17 is disconnected S1-1 is used to set CS5451 USE S1-2 is used to set CS5451 UOWRS S1-3 is used to set CS5451 GAIN	S1-1 Set to Enable S1-2 Set to 1 MHz S1-3 Set to GAIN = 1	1 2 3 OPEN	
HDR13	Used to switch VIN1- on the CS5451 between J11 and AGND.	VIN1- Set to BNC J11	O O VIN1- G	
HDR14	Used to switch the VREFIN from external VREF post connector, to the on board LT1004 reference, or to the on-chip reference VREFOUT. Refer to Table 3.	VREFIN Set to on- chip reference VREFOUT	O O LT1004 O VREFOUT O O EXT VREF	
HDR15	Controls the source for the CS5451 XIN clock input.	Set to on-board 4.000 MHz crystal (U1).	O O EXT XIN DGND O O 4.00 MHz OSC	
HDR16	Used as connector for 10-pin ribbon cable.	NA	NA	
HDR17	Determines whether the main analog supply will be powered from the A- post, or from the regulated 3V voltage (generated from the +5V_IN) post input.	Set to A-	0 0 +5V_IN A+	
HDR18	Choose whether the digital circuitry will be powered by main analog supply, or powered by separate dig- ital supply (through VD+ post).	Set to main analog supply	VD+ 0 0 V+	

 Table 2. Default Header Settings (Continued)

![](_page_8_Picture_1.jpeg)

# 2.4.1 Analog Inputs

The settings on the twelve analog input headers (2 per channel) determine which inputs will carry a signal, and which inputs may be grounded. They can be configured to accept either a single-ended or differential signal. Using the voltage channel #1 as an example (see Figure 3) note that HDR10 sets the input to the positive side of the first voltage channel input (VIN1+ pin). HDR13 sets the input to the negative side of the first voltage channel input (VIN1-pin). In a single-ended input configuration, HDR13 would be set to the "AGND" setting, and HDR10 would be set to "VIN1+" and would conduct the single-ended signal. In a differential input configuration, HDR13 would be set to "VIN1-" and HDR10 would be set to "VIN1+" and this pair of inputs would form the differential input pair into the VIN1+ and VIN1- pins of the CS5451.

Several patch-circuit areas are provided near the voltage/current input headers, in case the user wants to connect special sensor circuitry to the analog inputs (such as transformers, shunt resistors, etc., for monitoring a 3-phase power line). For each of the three channels, a Shunt Resistor or Current Transformer can be mounted in these areas and connections can be made to the individual currentchannel inputs. Likewise, for each of the three channels, a Voltage Divider or Voltage Transformer can be connected for each of the converter's three voltage inputs. Note from Figure 3 that a simple R-C network filters each sensor's output to reduce any interference picked up by the input leads. The 3 dB corner of the filter is approximately 50 kHz differential and common mode.

Other header options listed in Table 2 allow the user to set the source of the input clock signal and the source of the voltage reference (VREFIN) input, etc. The voltage reference options and clock input options are discussed next.

# 2.4.2 Voltage Reference Input

To supply the CS5451 with a suitable 1.2 V voltage reference input at the VREFIN pin, the evaluation board provides three voltage reference options: onchip, on-board, and external. See HDR14 as shown in figure 2. Table 3 illustrates the available voltage reference settings for HDR14. With HDR14's jumpers in position "VREFOUT," the CS5451's on-chip reference provides 1.2 volts. With HDR14 set to position "LT1004," the LT1004 provides 1.23 volts (the LT1004 temperature drift is typically 50 ppm/°C). By setting HDR14's jumpers to position "EXT VREF," the user can supply an external voltage reference to J16 connector post (VREF) and AGND inputs.

Reference	Description	HDR14		
LT1004	Selects on board LT1004 Reference (5 ppm/°C)	LT1004     O     O     VREFOUT     O     O     EXT VREF		
VREFOUT	Selects reference supplied by CS5451	O O LT1004 VREFOUT O O EXT VREF		
EXTVREF	Selects external reference	0 0 LT1004 0 0 VREFOUT EXT VREF		

 Table 3. Reference Selection

# 2.4.3 Clock Source for XIN

A 4.000 MHz crystal is provided to drive the XIN input of the CS5451. However, the user has the option to provide an external oscillator signal for XIN, by switching the setting of HDR15.

### 2.4.4 S1 DIP Switch

The S1 DIP switch is used if the user wants to remove the 20-pin cable from the CDBCAPTURE+ Board, in an effort to reduce noise from the CDB-CAPTURE+ Board that is transferred through the cable. Disconnecting this 20-pin cable would be done only for very low-noise, precision measurements. Slightly higher performance of the CDB5451-1 may be obtained when it is discon-

![](_page_9_Picture_1.jpeg)

nected. Note that the DIP switch settings on S1 are only valid when the J17 connector is disconnected from the CDB5451-1 board. When J17 is disconnected from CDB5451-1 board, the three switches on S1 independently control the logic levels of the SE pin, the OWRS pin, and the /GAIN pin on the CS5451. But when J17 is connected between the CDB5451-1 board and the CDBCAPTURE+ board, the S1 settings have no effect, and the pin logic levels are controlled instead by manipulating the on-screen switches in the PC software.

# 2.4.5 Reset Circuit

Circuitry has been provided which allows the user to execute a hardware reset on the CS5451. See Figure 4. By pressing on the S2 switch, the /RE-SET pin on the CS5451 will be held low until the switch is released.

![](_page_10_Figure_0.jpeg)

![](_page_10_Figure_1.jpeg)

Figure 2. Power Supply, CS5451, and Oscillator

CDB5451-1

1

![](_page_11_Figure_0.jpeg)

![](_page_11_Figure_1.jpeg)

![](_page_11_Figure_2.jpeg)

![](_page_11_Figure_3.jpeg)

Figure 3. Analog Inputs

![](_page_12_Figure_1.jpeg)

Figure 4. Digital Circuitry

CDB5451-1

![](_page_13_Picture_0.jpeg)

# **3. SOFTWARE**

The evaluation software was developed with Lab Windows/CVI<sup>TM</sup>, a software development package from National Instruments. The software is designed to run under Windows  $95^{TM}$  or later, and requires about 3 MB of hard drive space (2 MB for the CVI Run-Time Engine<sup>TM</sup>, and 1 MB for the evaluation software). After installing the software, read the readme.txt file for any last minute updates or changes. More sophisticated analysis software can be developed by purchasing the development package from National Instruments (512-794-0100).

# **3.1 Installing the Software**

Installation Procedure:

- 1) Turn on the PC, running Windows  $95^{\text{TM}}$  or later.
- 2) Insert the Installation Diskette #1 into the PC.
- 3) Select the Run option from the Start menu.
- 4) At the prompt, type: A:\SETUP.EXE <enter>.
- 5) The program will begin installation.
- 6) If it has not already been installed on the PC, the user will be prompted to enter the directory in which to install the LabWindows CVI Run-Time Engine<sup>™</sup>. The Run-Time Engine<sup>™</sup> manages executables created with Lab Windows/CVI<sup>™</sup>. If the default directory is acceptable, select OK and the Run-Time Engine<sup>™</sup> will be installed there.
- 7) After the Run-Time Engine<sup>™</sup> is installed, the user is prompted to enter the directory in which to install the CDB5451-1 software. Select OK to accept the default directory.
- Once the program is installed, it can be run by double clicking on the EVAL5451 icon, or through the Start menu.
- Note: The software is written to run with 640 x 480 resolution; however, it will work with 1024 x 768

resolution. If the user interface seems to be a little small, the user might consider setting the display settings to 640 x 480. (640x480 was chosen to accommodate a variety of computers).

### 3.2 Running the Software

### 3.2.1 Getting Started

The CDB5451-1 Evaluation software allows the user to obtain, display, and save data that is acquired by the CS5451 chip. First, connect the CDB5451-1 and CDBCAPTURE+ boards as described in Section 2., "*Hardware*". Apply power to the boards. To start the software, double click on the EVAL5451 icon, or initiate through the Start menu.

# 3.2.2 Selecting a COM Port

After launching the software, the user will be presented with the "Start-Up" Panel. A picture of the Start-Up Panel is shown in Figure 5. This panel indicates the name and version of the CDB54541 Evaluation Software. Also, a small pop-up dialogue box will appear which prompts the user to select a COM port. To select a COM port, first use the mouse to click on the "OK" button in this dialogue box. Next, use the mouse to click on the menu item "Select" and then choose the appropriate COM port setting (either COM1 or COM2). Note that the COM port settings on the host PC are configured to the following settings: 9600 baud, no parity, 8-bit data, and 1 stop bit. The COM port's Flow Control setting should be set to "Xon / Xoff." These settings should be set automatically by the LabWindows software. (The user may have to set the COM port settings manually if using Windows NT operating system. In this case, the user should run launch a Hyperterminal window to program the COM port settings, then exit Hyperterminal, then run the CDB5451-1 Software.)

![](_page_14_Picture_0.jpeg)

![](_page_14_Figure_2.jpeg)

![](_page_14_Figure_3.jpeg)

# 3.2.3 Resetting the Boards

After the COM port has been selected a second pop-up dialogue box will appear, to prompt the user to press the reset buttons on the CDB5451-1 board and on the CDBCAPTURE+ board before continuing. The user should follow these instructions: First, press on the button labeled "S2" on the CDB5451-1 board, and then press on the button labeled "S1" on the CDBCAPTURE+ board. Finally, use the mouse to click on the "OK" button to close this dialogue box. At this point, the mouse cursor will turn into the hour-glass shape while certain information is loaded from the PC software into the CDBCAPTURE+ board. This will take about 8 seconds. The user should wait until the mouse cursor has returned to its normal appearance before proceeding.

# 3.2.4 The Data Panel

The Data Panel is where all of the analysis tools are located. See Figure 6. To get to the Data Panel, go to the menu item called "Panel" and select the option called "Data Panel."

A new panel will appear on the screen. This is the Data Panel. Once in the data panel, the user has two options available: Capture and Real-Time.

# 3.2.5 Capture Mode

Capture mode allows user to capture waveform data from the CS5451. The data can be ported back to the PC and displayed as a graph. The functionality of each control in the Capture portion of the Data Panel is described below. In order to give the user an idea of the proper sequence of actions that should be taken to perform a data capture, a typical sequence of user-actions is listed below.

![](_page_15_Picture_1.jpeg)

![](_page_15_Figure_2.jpeg)

Figure 6. Data Panel

# 3.2.5.1. TYPICAL CAPTURE SEQUENCE:

- In the Data Panel, select Channel Pairs 1, 2, and/or 3 by switching the switches in the box labelled "Channel-Pair Selector."
- 2) Press on the button labelled "CAPTURE". Wait until the capture is completed.
- Determine how many data words should be ported up from the Capture+ Board's memory to the PC. Enter this number in the box labeled "Words"
- 4) Using the mouse, click on the "SRAM To PC" button.
- 5) Select one of the channel boxes that indicate the number of samples received. For instance, click inside the "V\_2 samples" box (assuming that the Channel 2 Pair was among the pairs

that had been selected for capture).

6) Using the mouse, press (click) on the "TIME-PLOT" button to view the sampled data, which shows the A/D conversions from the channel selected in the previous step.

# 3.2.5.2. DESCRIPTION OF DATA PANEL CONTROLS

### • "CAPTURE"

Capture initiates the data capture sequence. Depending on how many of the three channel pairs are selected, the user may capture data for all three channel pairs, two channel pairs, or just one channel pair (note that each pair represents one voltage channel and one current channel.) The software automatically determines the maximum number of frames that it can store in memory, and then adjusts the number indica-

![](_page_16_Picture_0.jpeg)

tor box that reads: "Frames of Data Being Stored."

Once the "CAPTURE" button is pressed (by using the mouse) it should turn red-colored, and the mouse cursor should change to an hourglass symbol. The CDBCAPTURE+ will now gather raw data from the CDB5451-1 board, and store the data into its on-board memory. Once the capture process has stopped, then the "CAPTURE" button should turn back to gray color. Now the data is in memory.

### "SRAM to PC"

After capturing the data (with the "CAPTURE" button), the data must be transferred from the memory on the CAPTURE+ board to the PC. To actually get the data from the CDBCAP-TURE+ board up to the PC, the user must now press on the "SRAM to PC" button. Before doing this, the user should observe the value in the number box labelled "Words." The user can change the value in this box. The user should make sure that the number of samples that are going to be brought up will be a 'reasonable' number. This mainly applies to the FFT analysis: If the user wants to get meaningful FFT results, the user must make sure that the number of samples loaded for one particular channel will be some whole-number power of 2 (...,8, 16, 32, 64, 128, 256,...).

### EXAMPLE 1:

- Capture data for all three channel pairs. This will set the value in the "Frames of Data Being Stored" box to 8192.
- 2) User can transfer up to 8192 pieces of data for each of the six channels. But suppose user only wants 4096 samples from each channel. Note that 4096 is a power of 2, so this is OK. So multiply 4096 x 6 = 24576. Enter this number into the "Words" box.

### EXAMPLE 2:

- Change the "Channel Pair Selector" buttons to capture data for channel pairs 1 and 3. This represents 4 channels worth of data (each pair has both voltage and current). After mouse-clicking on the "CAPTURE" button, note that the number in the "Frames of Data Being Stored" box changes to 16384.
- 2) After capture has completed, the user can transfer up to 16384 samples for each of the four channels. If user wants the maximum number of samples possible, multiply 16384 x 4 = 65536. Enter this number into the "Words" box. Then mouse-click on the "SRAM to PC" button. If user wants only 8192 samples, then transfer 8192 x 4 = 32678. Therefore, the user should enter "32678" into the "Words" box. Then use the mouse to click on the "SRAM to PC" button.
- "V\_1 samples"

This box indicates how many channel 1 voltage samples were transferred from the CDBCAP-TURE+ board up to the PC. To make channel 1 voltage samples the *active data array*, just click the mouse once inside this box.

- Note: The "active data array" indicates which collection of samples is now stored in the array that will be plotted/saved if certain other commands/functions are initiated. For example, after running "SRAM to PC", if the user clicks inside the box called "V\_1 samples", then these samples will be loaded in as the active data array.•
- "I\_1 samples"

This box indicates how many channel 1 current samples were transferred from the CDBCAP-TURE+ board up to the PC. To make channel 1 current samples the active data array, just click inside this box.

![](_page_17_Picture_1.jpeg)

### • "V\_2 samples"

This box indicates how many channel 2 voltage samples were transferred from the CDBCAP-TURE+ board up to the PC. To make channel 2 voltage samples the active data array, just click inside this box.

### • "I\_2 samples"

This box indicates how many channel 2 current samples were transferred from the CDBCAP-TURE+ board up to the PC. To make channel 2 current samples the active data array, just click inside this box.

# • "V\_2 samples"

This box indicates how many channel 2 voltage samples were transferred from the CDBCAP-TURE+ board up to the PC. To make channel 2 voltage samples the active data array, just click inside this box.

### • "I\_2 samples"

This box indicates how many channel 2 current samples were transferred from the CDBCAP-TURE+ board up to the PC. To make channel 2 current samples the active data array, just click inside this box.

• "FFT"

Performs an FFT on the active data array and displays it in the graph window. For this function to work correctly, the number of samples in the active data array must be equal to some whole-number power of 2.

• "TIMEPLOT"

Graphs the samples of the active data array. The x-axis indicates the sample number. The y-axis indicates the coded word values from the CS5451 A/D converter.

### "HISTOGRAM"

Performs a statistical histogram analysis of the active data array, then plots the results in the

graph window. The user can set the number of bins for the histogram in the box called "Number of Bins in Histogram."

### • "Minimum"

This indicator box displays the minimum value of the active data array, after the HISTOGRAM analysis has been run on the active data array.

# • "Maximum"

This indicator box displays the maximum value of the active data array, after the HISTOGRAM analysis has been run on the active data array.

• "Mean"

This indicator box displays the mean value of the active data array, after the HISTOGRAM analysis has been run on the active data array.

# • "Sample Freq"

This indicator box displays the sampling rate of the CS5451. The CDB5451-1 has two different sampling rates: 3906 Hz and 1953 Hz. These two sampling rates correspond to the logic level of the OWRS pin of the CS5451. See CS5451 data sheet for more details.

After the "FFT" function is executed, this indicator box calculates the signal-to-noise ratio with respect to the fundamental of the active data array, after the "FFT" function is executed.

"S/N + D"

After the "FFT" function is executed, this indicator box displays the result of the calculation of signal-to-noise plus distortion with respect to the fundamental, of the active data array.

• "S/D"

After the "FFT" function is executed, this indicator box displays the result of the calculation of signal-to-distortion with respect to the fundamental, of the active data array.

<sup>• &</sup>quot;S/N"

![](_page_18_Picture_1.jpeg)

### • "SAVE To File"

Clicking on this button will save the data that is plotted in the graph window to a text file. A pop-up window will appear which prompts the user to specify a path and file name to which the data will be stored.

### 3.2.6 Real-Time Mode

The real-time functions are located in the top-right corner of the Data Panel. Real-Time allows the user to calculate the rms values of the current and voltage signals from one channel pair. Note that this mode can only be run on one of the three channel pairs at a time. The user must select which channel pair is to be analyzed, by manipulating the "Channel Pair Selector" switches on the right-hand side of the Data Panel. In addition to rms calculation, the energy is calculated as well. Each instantaneous pair of voltage and current samples is multiplied together, and these voltage-current product terms are summed together to create the energy reading.

### • "Real-Time Capture"

Setting this switch to the "On" position will initiate the real-time data collection sequence. To end the real-time sequence, change the switch back to the "Off" position (using the mouse).

# "Cycle Count"

This box is used to set the duration of the *computation cycle*. The computation cycle is defined as the number of samples over which the rms and energy calculations are performed. If this box is set to 4000, then the rms and energy results will be updated every 4000 samples. If the sampling frequency is at 3906 Hz, one computation cycle lasts for ~1.024 seconds. The value in this box sets the number of samples to use for one computation cycle. This box can be modified by the user. The larger the value of the computation cycle, the more accurate the rms results will be. The computation cycle

should not be set to less than 275. Errors may occur in the rms and energy calculations if this value is less than 275.

### • "# of R-T Samples to Collect"

This box is used to set the number of computation cycles to calculate before stopping the realtime sequence. For example, suppose that this box is set (by the user) to a value of 200, then real-time will run for 200 computation cycles, and then it will stop on its own. If the value of this box is set to -1, then real-time will run continuously or until the user turns real-time off by mouse-clicking on the "Real-Time Capture" switch.

### "Real-Time Samples Count"

This indicator box displays the number of computation cycles that have elapsed/transpired since the "Real-Time Capture" switch was set to the "On" position.

### "RMS Voltage"

Displays the result of the latest rms calculation for the voltage samples. This box will be updated after each computation cycle. Note that the scale of the values in this box are based on a normalized scale, where the maximum value is +1 and the minimum value is -1. Note that to obtain a value of +1 in this box, the user must set the voltage level to the CS5451's voltagechannel inputs to a DC level that is equal to the full-scale input level of the CS5451 (800mV). (Actually the maximum possible value is just less than +1, more like 0.9999...)

### • "RMS Current"

Displays the result of the latest rms calculation for the current samples. This box will be updated after each computation cycle. Note that the scale of the values in this box are based on a normalized scale, where the maximum value is +1 and the minimum value is -1. A value of +1

![](_page_19_Picture_0.jpeg)

is obtained in this box is obtained by setting the CS5451 current-channel input voltage to a DC level that is equal to the full-scale input level of the CS5451. (Actually the maximum value is just less than +1, more like 0.9999... and the minimum value is -0.9999...)

### • "Energy"

Displays the results of the latest energy calculation. The energy calculation is obtained by summing the most recent N voltage-current product terms, where N is the value in the "Cycle-Count" box.

### • "Save Real-Time To File"

Clicking on this button (with the mouse) will allow the user the save the results of the most recent real-time sequence to a file. The user will be prompted for a path and filename to which the results will be saved.

The CS5460A serial interfaces are  $SPI^{\mathbb{M}}$  and  $Microwire^{\mathbb{M}}$  compatible. The interface control lines ( $\overline{CS}$ , SDI, SDO, and SCLK) are connected

to the 80C51 microcontroller via port one. To interface an external microcontroller, these control lines are also connected to HDR6 (Header 6). However to accomplish this, the evaluation board must be modified in one of three ways: 1) cut the interface control traces going to the microcontroller, 2) remove resistors R4, R7, R8, and R13, or 3) remove the microcontroller.

![](_page_19_Figure_9.jpeg)

![](_page_20_Picture_1.jpeg)

![](_page_20_Figure_2.jpeg)

SILKSCREEN - TOP

Figure 7. Silkscreen

![](_page_21_Picture_1.jpeg)

![](_page_21_Figure_2.jpeg)

\$

TOP SIDE

Figure 8. Circuit Side

![](_page_22_Picture_1.jpeg)

### CRYSTAL SEMICONDUCTOR CDB5451 TSOP/Socket Version CDB5451-1C.Ø

![](_page_22_Figure_3.jpeg)

BOTTOM SIDE

Figure 9. Solder Side

![](_page_23_Picture_0.jpeg)

# 4. ADDENDUM

# 4.1 Errata for CDBCAPTURE+

Recently the CDBCAPTURE+ board was updated with one additional 120 pF capacitor between the CKOUT line and the /IRQA line. This addition

improves noise problems on the board. Figure 10 is a diagram which illustrates where this capacitor needs to be placed, in case the user has an older version of the CDBCAPTURE+ board. The user should add this capacitor to the board if it is not there already.

![](_page_23_Figure_6.jpeg)

To eliminate noise (from PLD) on IRQA, Solder ~120 pF cap as shown.

Figure 10. Recent ECO to CDBCapture+ Board

![](_page_24_Picture_0.jpeg)

# • Notes •

![](_page_25_Picture_0.jpeg)