

# BUK98150-55A

TrenchMOS™ logic level FET

Rev. 02 — 25 March 2002

Product data

## 1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™<sup>1</sup> technology, featuring very low on-state resistance.

Product availability:

BUK98150-55A in SOT223 (SC-73).

## 2. Features

- TrenchMOS™ technology
- Q101 compliant
- 150 °C rated
- Logic level compatible.

## 3. Applications

- Automotive and general purpose power switching:
  - ◆ 12 V and 24 V loads
  - ◆ Motors, lamps and solenoids.

## 4. Pinning information

Table 1: Pinning - SOT223 (SC-73), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d)		
3	source (s)		
4	drain (d)		

**SOT223 (SC-73)**

1. TrenchMOS is a trademark of Koninklijke Philips Electronics N.V.



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## 5. Quick reference data

**Table 2: Quick reference data**

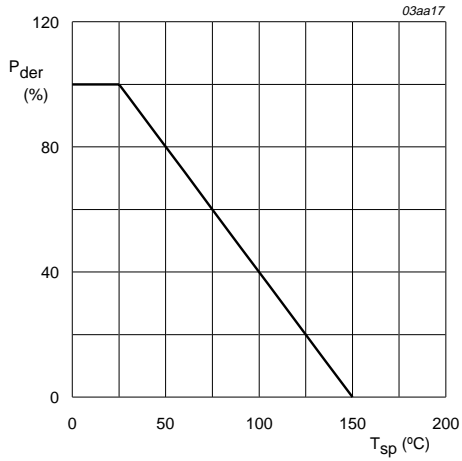
Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DS}$	drain-source voltage (DC)		-	55	V
$I_D$	drain current (DC)	$T_{sp} = 25\text{ °C}; V_{GS} = 5\text{ V}$	-	5	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$	-	8	W
$T_j$	junction temperature		-	150	°C
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 5\text{ A}$	128	150	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 5\text{ A}$	-	161	mΩ
		$V_{GS} = 10\text{ V}; I_D = 5\text{ A}$	116	137	mΩ

## 6. Limiting values

**Table 3: Limiting values**

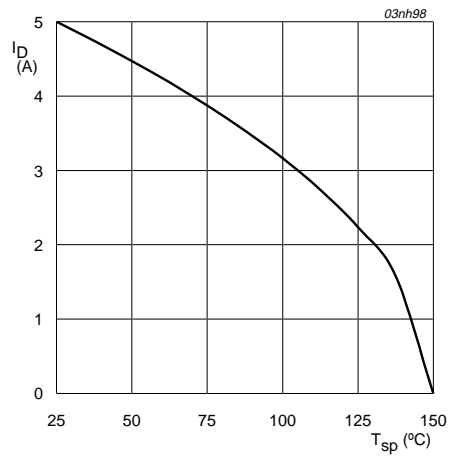
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)		-	55	V
$V_{DGR}$	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$V_{GS}$	gate-source voltage (DC)		-	±15	V
$I_D$	drain current (DC)	$T_{sp} = 25\text{ °C}; V_{GS} = 5\text{ V};$ <b>Figure 2 and 3</b>	-	5	A
		$T_{sp} = 100\text{ °C}; V_{GS} = 5\text{ V};$ <b>Figure 2</b>	-	3	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ <b>Figure 3</b>	-	22	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C};$ <b>Figure 1</b>	-	8	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	operating junction temperature		-55	+150	°C
<b>Source-drain diode</b>					
$I_{DR}$	reverse drain current (DC)	$T_{sp} = 25\text{ °C}$	-	5	A
$I_{DRM}$	peak reverse drain current	$T_{sp} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	22	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive avalanche energy	unclamped inductive load; $I_D = 5\text{ A};$ $V_{DS} \leq 55\text{ V}; V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega;$ starting $T_j = 25\text{ °C}$	-	31	mJ



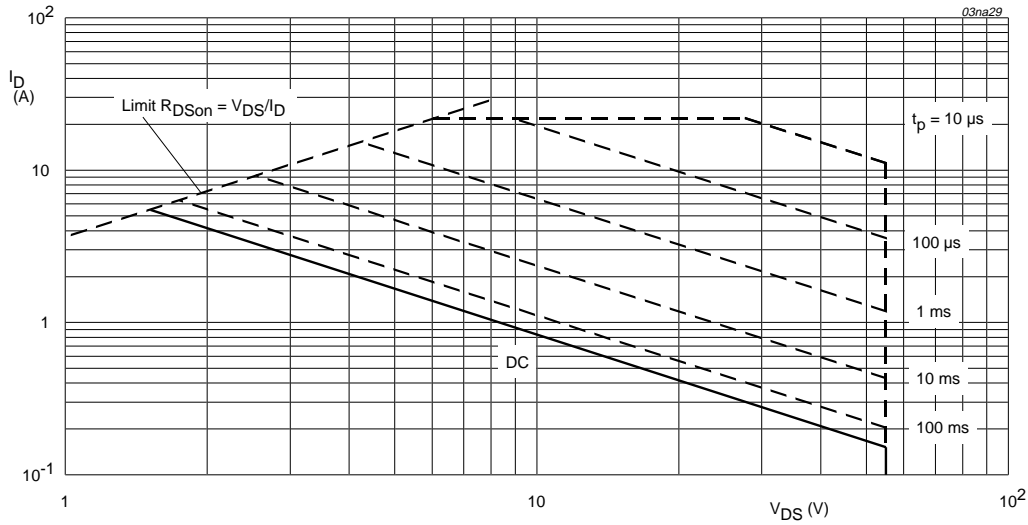
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of solder point temperature.**



V<sub>GS</sub> ≥ 4.5 V

**Fig 2. Continuous drain current as a function of solder point temperature.**



T<sub>sp</sub> = 25 °C; I<sub>DM</sub> is single pulse.

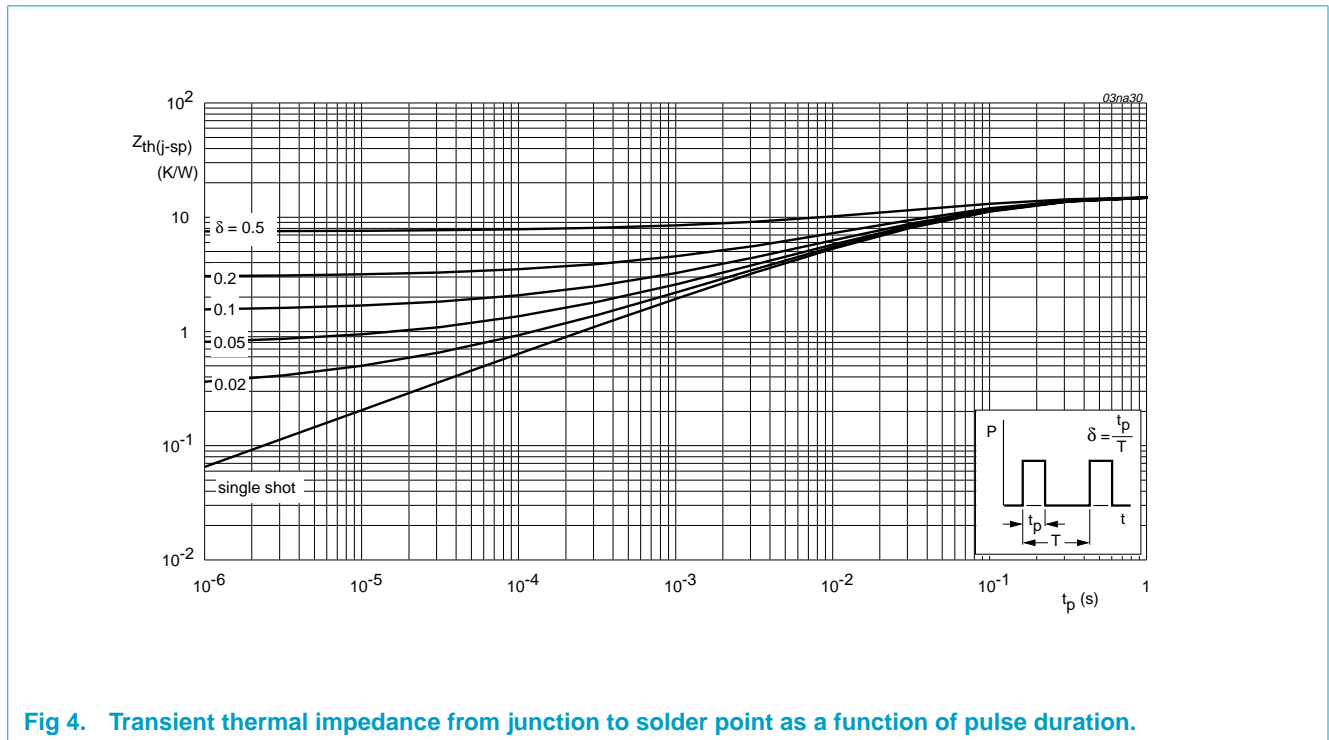
**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

## 7. Thermal characteristics

**Table 4: Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	70	-	K/W

### 7.1 Transient thermal impedance



**Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.**

## 8. Characteristics

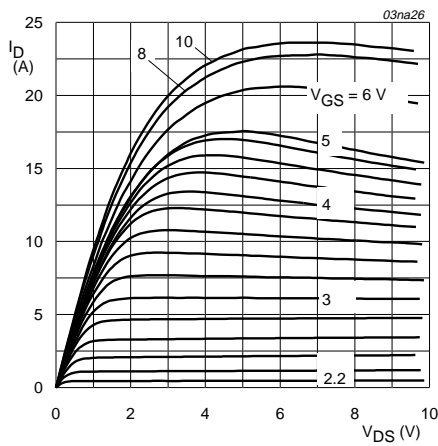
**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	55	-	-	V
		T <sub>j</sub> = -55 °C	50	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; Figure 9				
		T <sub>j</sub> = 25 °C	1	1.5	2	V
		T <sub>j</sub> = 150 °C	0.6	-	-	V
		T <sub>j</sub> = -55 °C	-	-	2.3	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 55 V; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	-	0.05	10	μA
		T <sub>j</sub> = 150 °C	-	-	500	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±10 V; V <sub>DS</sub> = 0 V	-	2	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 5 A; Figure 7 and 8				
		T <sub>j</sub> = 25 °C	-	128	150	mΩ
		T <sub>j</sub> = 150 °C	-	-	276	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 5 A;	-	-	161	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 5 A;	-	116	137	mΩ
<b>Dynamic characteristics</b>						
Q <sub>g(tot)</sub>	total gate charge	V <sub>GS</sub> = 5 V; V <sub>DD</sub> = 44 V;	-	5.3	-	nC
Q <sub>gs</sub>	gate-to-source charge	I <sub>D</sub> = 5 A; Figure 14	-	1.0	-	nC
Q <sub>gd</sub>	gate-to-drain (Miller) charge		-	2.8	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V;	-	240	320	pF
C <sub>oss</sub>	output capacitance	f = 1 MHz; Figure 12	-	40	48	pF
C <sub>rss</sub>	reverse transfer capacitance		-	25	34	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DD</sub> = 20 V; R <sub>L</sub> = 3.3 Ω;	-	8	-	ns
t <sub>r</sub>	rise time	V <sub>GS</sub> = 5 V; R <sub>G</sub> = 10 Ω;	-	57	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	16	-	ns
t <sub>f</sub>	fall time		-	13	-	ns

Table 5: Characteristics...continued

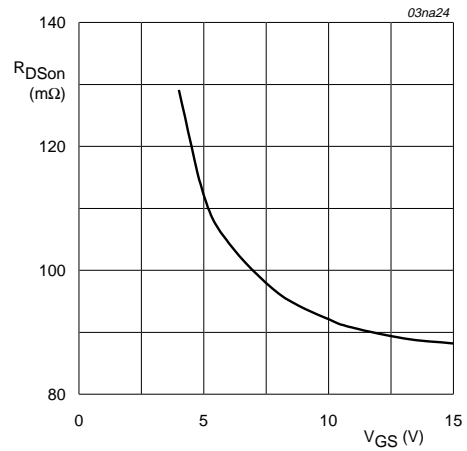
$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 5\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; Figure 15	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 5\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$	-	24	-	ns
$Q_r$	recovered charge	$V_{GS} = -10\text{ V}$ ; $V_{DS} = 30\text{ V}$	-	30	-	nC



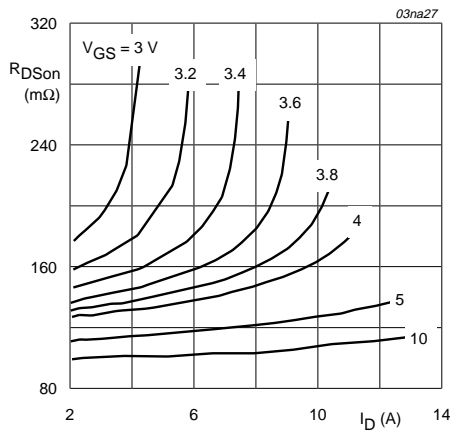
$T_j = 25\text{ }^\circ\text{C}$ ;  $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



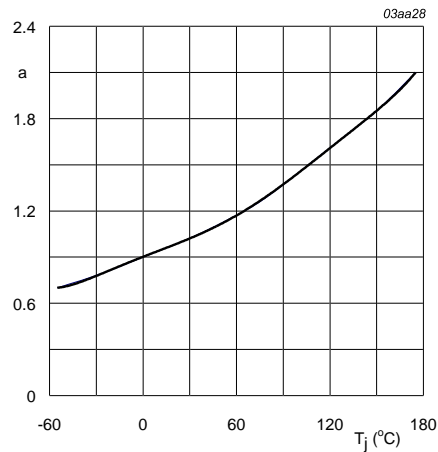
$T_j = 25\text{ }^\circ\text{C}$ ;  $I_D = 5\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



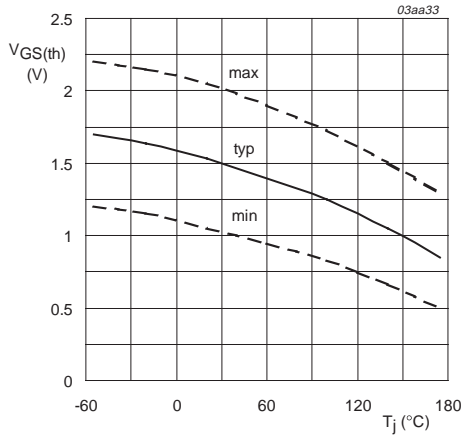
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



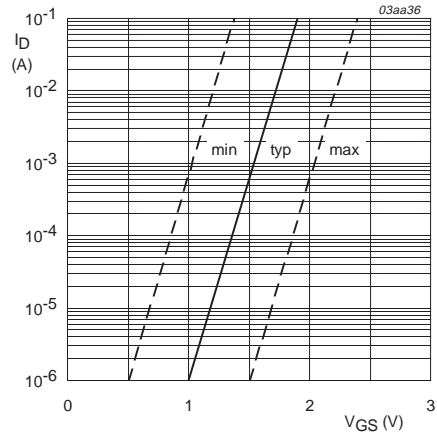
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



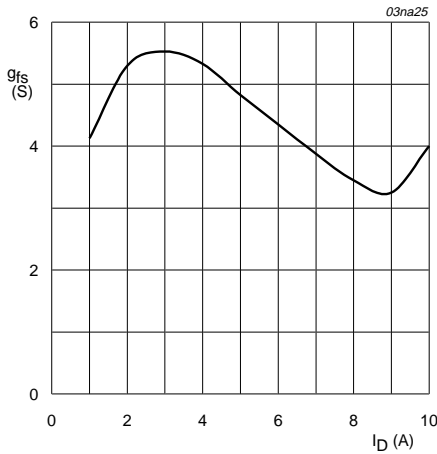
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



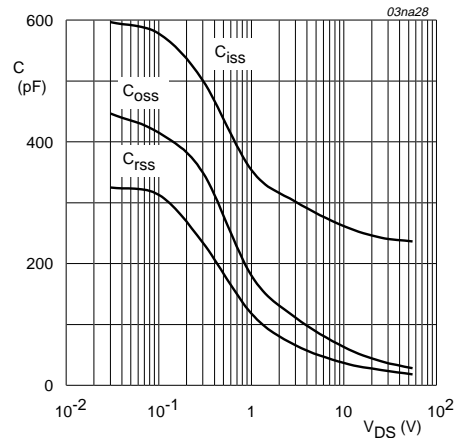
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



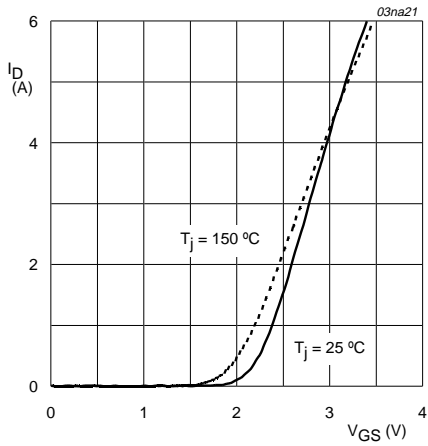
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



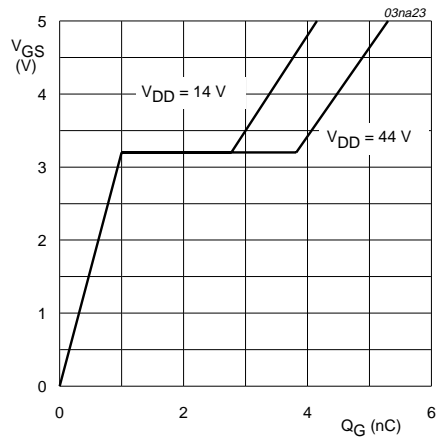
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



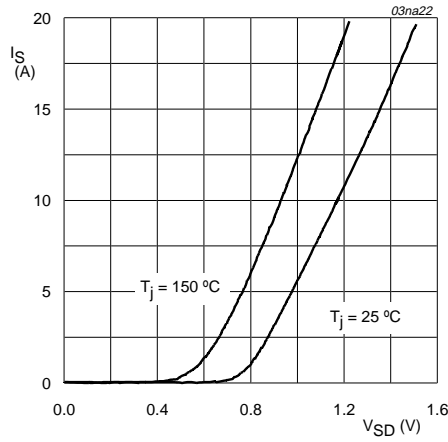
$V_{DS} = 25 \text{ V}$

**Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



$T_j = 25 \text{ °C}; I_D = 5 \text{ A}$

**Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.**



$V_{GS} = 0 \text{ V}$

**Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.**



**9. Package outline**

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223

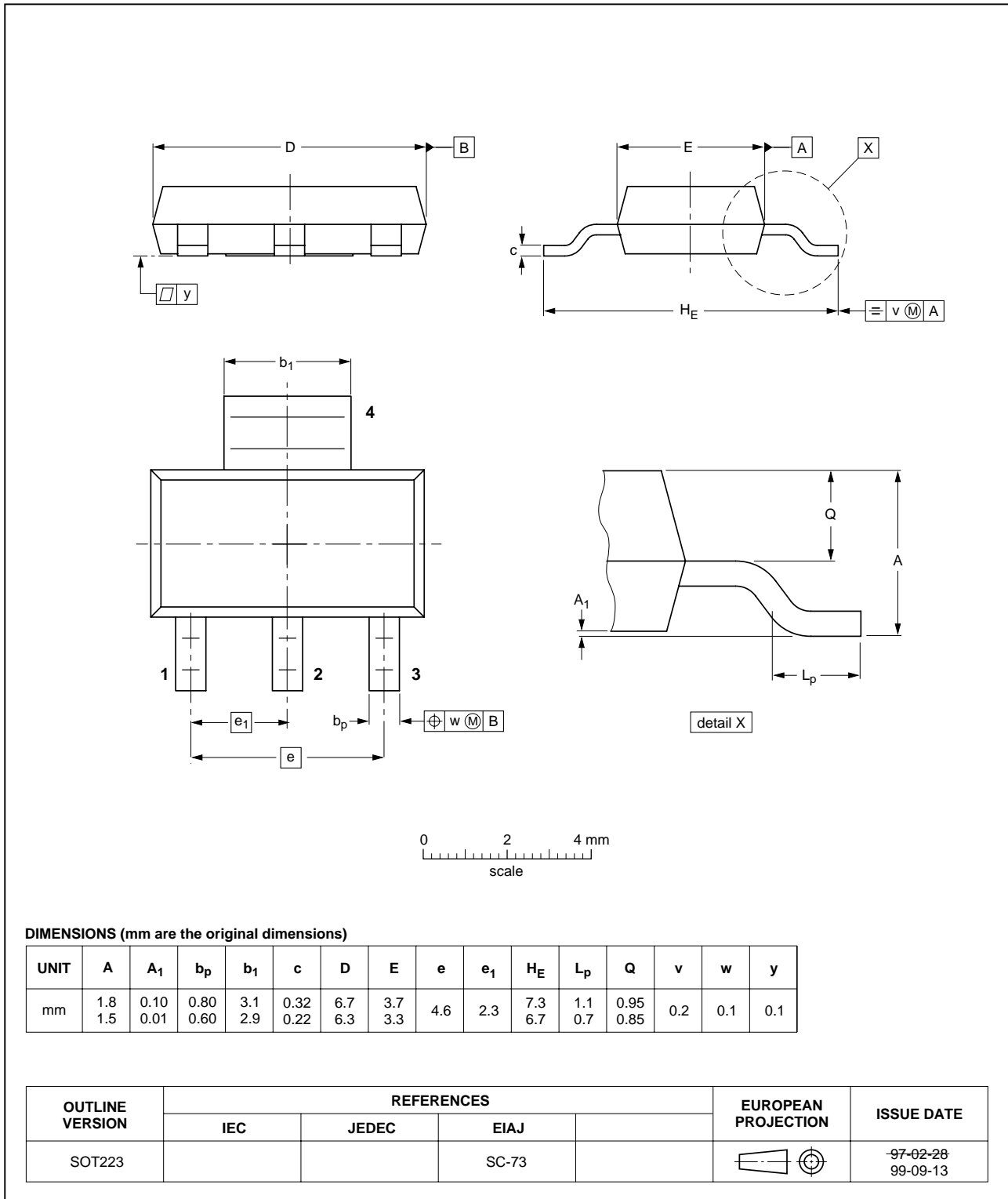
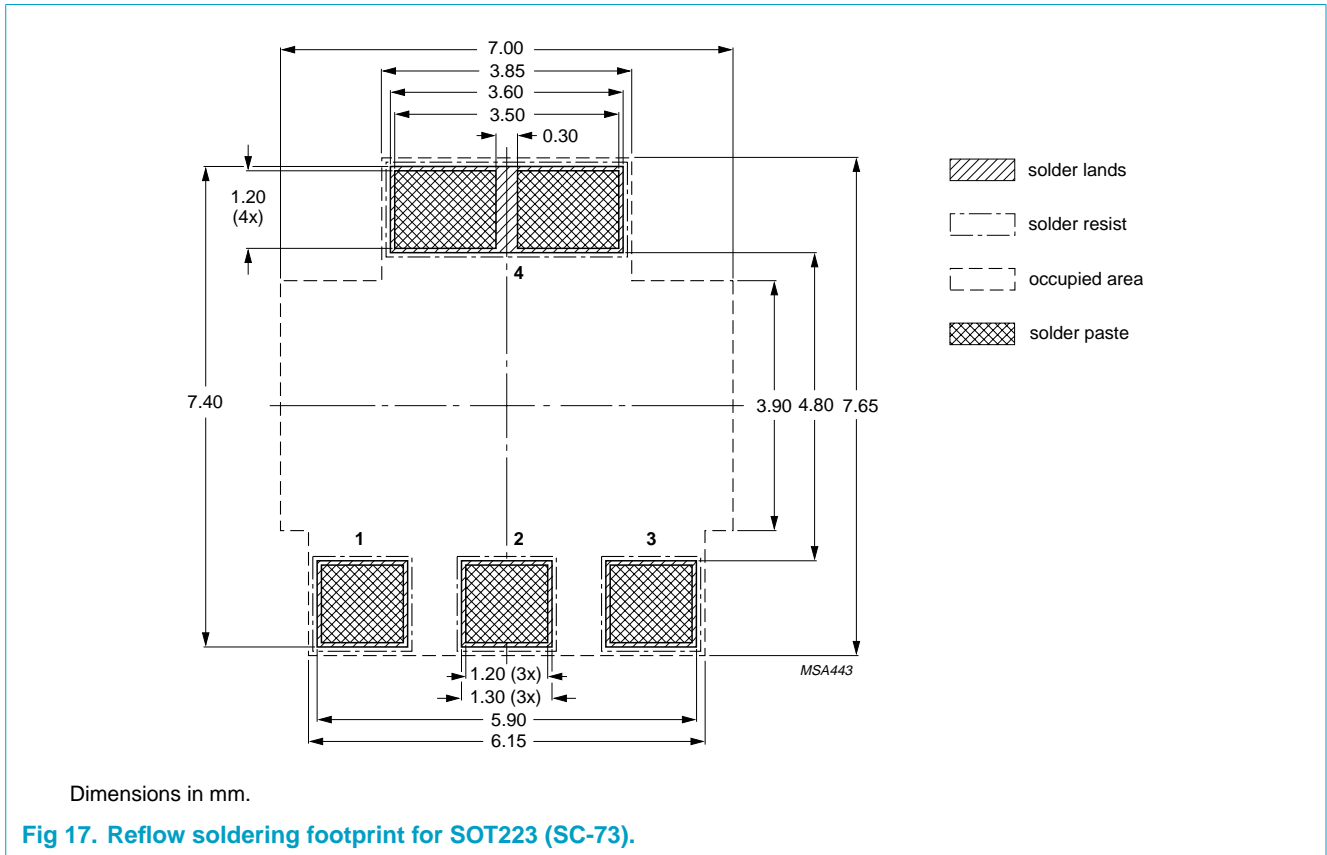


Fig 16. SOT223 (SC-73).

## 10. Soldering



## 11. Revision history

**Table 6: Revision history**

Rev	Date	CPCN	Description
02	20020325	-	<b>Product data; second version, supersedes Rev 01 of 20001003. Modifications:</b> <ul style="list-style-type: none"> <li>• Gate-source voltage maximum increased from 10 to 15 V in limiting values table.</li> <li>• <math>R_{th(j-sp)}</math> maximum decreased from 20 K/W to 15 K/W in thermal characteristics table.</li> <li>• Switching speed measurements updated in characteristics table.</li> <li>• Total power dissipation, peak drain current, peak reverse drain current, and non-repetitive avalanche energy figures updated in quick reference data and limiting values.</li> </ul>
01	20001003	-	<b>Product specification; initial version.</b>

## 12. Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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