14/12/10-Bit, 1200 MSPS D/A Converters

Preliminary Technical Data

AD9736/AD9735/AD9734

FEATURES

- 1.8/3.3 V Single Supply Operation
- AD9736 SFDR > 53 dBc to f_{OUT} = 600 MHz
- AD9736 IMD > 65 dBc to f_{OUT} = 600 MHz
- AD9736 DNL = ± 1.0 LSB
- AD9736 INL = ± 2.0 LSB
- Low power: 380 mW (I_{OUTFS} = 20 mA; f_{OUT} = 330 MHz)
- LVDS data interface with on-chip 100 Ω terminations
- Analog Output: Adjustable 10-30mA (RL=25 Ω to 50 Ω)
- On-Chip 1.2 V Reference
- 160 pin BGA Package

APPLICATIONS

- Instrumentation
- Automatic Test Equipment
- RADAR
- Avionics
- Wideband Communications Systems:
  - Point-to-Point Wireless
  - LMDS
  - PA Linearization

PRODUCT DESCRIPTION

The AD9736, AD9735, and AD9734 are high performance, high frequency DACs that provide sample rates of up to 1200 MSPS, permitting multi-carrier generation up to their Nyquist frequency. The AD9736 is the 14 bit member of the family, while the AD9735 and the AD9734 are the 12 and 10 bit members, respectively. They include a serial port interface (SPI) that provides for programming many internal parameters and also enables read-back of status registers. They use a reduced specification LVDS interface to minimize data interface that may degrade performance. The output current can be programmed over a range of 10mA to 30mA. The AD9736 family is manufactured on a 0.18µm CMOS process and operates from 1.8V and 3.3V supplies for a total power consumption of 380mW in bypass mode. It is supplied in a 160 pin BGA package for reduced package parasitics.

FUNCTIONAL BLOCK DIAGRAM

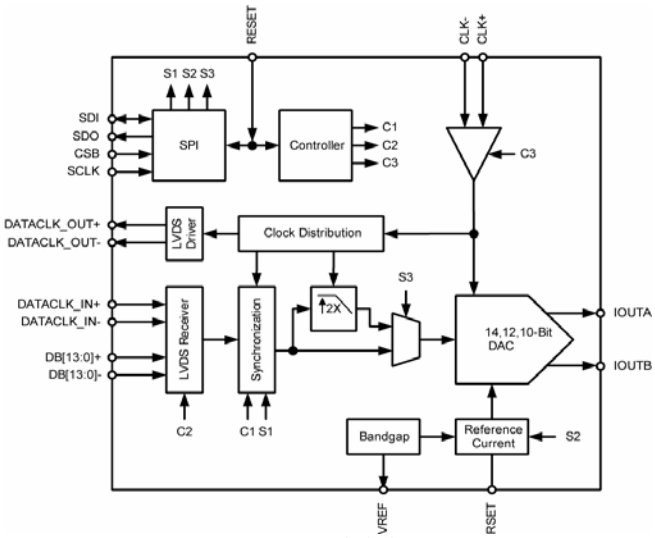


Figure 1. Functional Block Diagram

PRODUCT HIGHLIGHTS

Ultra-low Noise and Intermodulation Distortion (IMD) enable high quality synthesis of wideband signals at intermediate frequencies up to 600 MHz.

LVDS receivers support Double Data Rate (DDR) input format, with the maximum conversion rate of 1200 MSPS.

Manufactured on a CMOS process, the AD9736 family uses a proprietary switching technique that enhances dynamic performance.

The current output(s) of the AD9736 family can be easily configured for various single-ended or differential circuit topologies.

Rev. PrC 4/05/2004

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

REVISION HISTORY

Revision PrA: Initial Version

Revision PrB: Updated data based on initial evaluation results

Revision PrC: Updated data for web display and ongoing evaluation results

AD9736/35/34—SPECIFICATIONS[1]

DC SPECIFICATIONS

(VDD33 = 3.3 V, VDD18 = 1.8 V, MAXIMUM SAMPLE RATE, 25 OHM 1% BALANCED LOAD, UNLESS OTHERWISE NOTED)

Parameter		Temp	Test Level	AD9736			AD9735			AD9734			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION					14			12			10		Bits
ACCURACY	Integral Nonlinearity (DNL)				± 2.0								LSB
	Differential Nonlinearity (INL)				± 1.0								LSB
ANALOG OUTPUTS	Offset Error				TBD			TBD			TBD		% FSR
	Gain Error (With Internal Reference)				± 0.5			± 0.5			± 0.5		% FSR
	Gain Error (Without Internal Reference)				± 0.5			± 0.5			± 0.5		% FSR
	Full Scale Output Current			10	20	30	10	20	30	10	20	30	mA
	Output Compliance Range			1.0			1.0			1.0			V
	Output Resistance				TBD			TBD			TBD		kΩ
	Output Capacitance				TBD			TBD			TBD		pF
TEMPERATURE DRIFT	Offset				TBD			TBD			TBD		ppm/°C
	Gain				TBD			TBD			TBD		ppm/°C
	Reference Voltage				TBD			TBD			TBD		ppm/°C
REFERENCE	Internal Reference Voltage				1.2			1.2			1.2		V
	Output Current				100			100			100		nA
ANALOG SUPPLY VOLTAGES	VDDA33			3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
	VDDA18			1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
DIGITAL SUPPLY VOLTAGES	VDDD33			3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
	VDDD18			1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
	VDDCLK			1.70	1.8	1.90	1.70	1.8	1.90	1.70	1.8	1.90	V
POWER CONSUMPTION	Bypass Mode				380			380			380		mW
	FIR Filter Enabled				550			550			550		mW
	Standby Power												mW

Table 1: DC Specifications

[1] Specifications subject to change without notice

DIGITAL SPECIFICATIONS[1]

(VDD33 = 3.3 V, VDD18 = 1.8 V, MAXIMUM SAMPLE RATE, 25 OHM 1% BALANCED LOAD, UNLESS OTHERWISE NOTED)

Parameter		Temp	Test Level	AD9736,35,34			Unit
				Min	Typ	Max	
LVDS DATA INPUTS (DB[13:0]+, DB[13:0]-)	Input voltage range, Via or Vib			825		1575	mV
	Input differential threshold			-100		100	mV
	Input differential hysteresis			25			mV
	Receiver differential input impedance			80		120	Ω
	LVDS input rate			1200			MSPS
	LVDS data Bit Error Rate				10^{-9}		Err/Bit
LVDS CLOCK INPUT (DATACLK_IN+, DATACLK_IN-)	Input voltage range, Via or Vib			825		1575	mV
	Input differential threshold			-100		100	mV
	Input differential hysteresis			25			mV
	Receiver differential input impedance			80		120	Ω
	Maximum Clock Rate			600			MHz
LVDS CLOCK OUTPUT (DATACLK_OUT+, DATACLK_ OUT-)	Output voltage high, Voa or Vob					1375	mV
	Output voltage low, Voa or Vob			1025			mV
	Output differential voltage			180	200	220	mV
	Output offset voltage			1150		1250	mV
	Output impedance, single ended			80	100	120	Ω
	Ro mismatch between A & B					10	%
	Change in |Vod| between '0' and '1'					25	mV
	Change in Vos between '0' and '1'					25	mV
	Output current – Driver shorted to ground					3	mA
	Output current – Drivers shorted together					3	mA
	Power-off output leakage					TBD	mA
	Maximum Clock Rate			600			MHz
DAC CLOCK INPUT (CLK+, CLK-)	Differential peak-to-peak Voltage				800		mV
	Common Mode Voltage				400		mV
	Maximum Clock Rate			1200			MHz
SERIAL PERIPHERAL INTERFACE	Maximum Clock Rate (SCLK)					40	MHz
	Maximum Pulse width high					TBD	ns
	Maximum pulse width low					TBD	ns

Table 2: Digital Specifications

[1] LVDS Drivers and Receivers are compliant to the IEEE-1596 Reduced Range Link, unless otherwise noted

AC SPECIFICATIONS

(VDD33 = 3.3 V, VDD18 = 1.8 V, MAXIMUM SAMPLE RATE, 25 OHM 1% BALANCED LOAD, UNLESS OTHERWISE NOTED)

Parameter		Temp	Test Level	AD9736			AD9735			AD9734			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE	Maximum Update Rate				1200			1200			1200		MSPS
	Output Settling Time (tst) (to 0.025%)				TBD			TBD			TBD		ns
	Output Rise Time (10% to 90%)				TBD			TBD			TBD		ns
	Output Fall Time (90% to 10%)				TBD			TBD			TBD		ns
	Output Noise (IoutFS=20mA)				TBD			TBD			TBD		pA/rtHz
SPURIOUS FREE DYNAMIC RANGE (SFDR)	f_{DAC} = 1200 MSPS, f_{OUT} = 50 MHz				80								dBc
	f_{DAC} = 1200 MSPS, f_{OUT} = 100 MHz				77								dBc
	f_{DAC} = 1200 MSPS, f_{OUT} = 316 MHz				63								dBc
	f_{DAC} = 1200 MSPS, f_{OUT} = 550 MHz				55								dBc
Two Tone Intermodulation Distortion (IMD)	f_{DAC} = 1200 MSPS, f_{OUT} = 50 MHz				85								dBc
	f_{DAC} = 1200 MSPS, f_{OUT} = 100 MHz				84								dBc
	f_{DAC} = 1200 MSPS, f_{OUT} = 316 MHz				74								dBc
	f_{DAC} = 1200 MSPS, f_{OUT} = 550 MHz				65								dBc
Noise Spectral Density (NSD)	f_{DAC} = 1200 MSPS, f_{OUT} = 50 MHz				-165								dBm/Hz
	f_{DAC} = 1200 MSPS, f_{OUT} = 100 MHz				-164								dBm/Hz
	f_{DAC} = 1200 MSPS, f_{OUT} = 316 MHz				-158								dBm/Hz
	f_{DAC} = 1200 MSPS, f_{OUT} = 550 MHz				-155								dBm/Hz

Table 3: AC Specifications

EXPLANATION OF TEST LEVELS

TEST LEVEL

I 100% production tested.

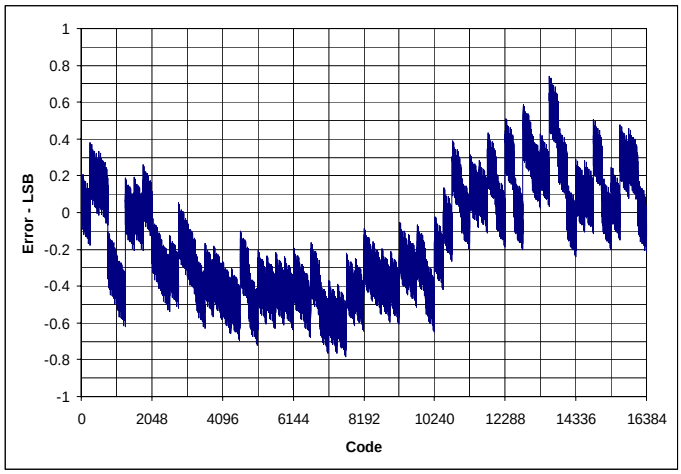
II 100% production tested at +25°C and guaranteed by design and characterization at specified temperatures.

III Sample Tested Only

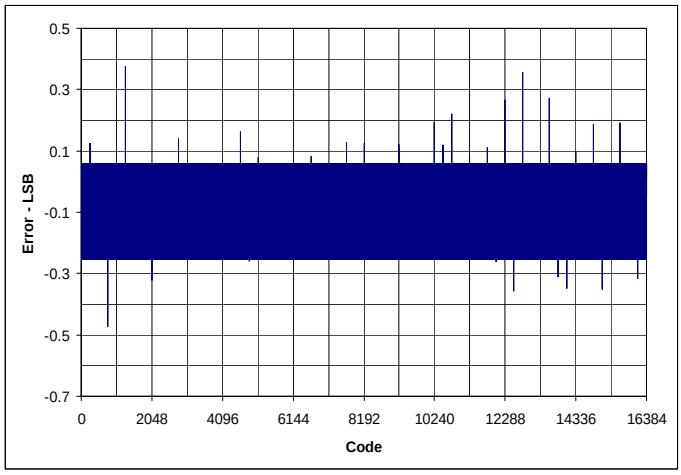
IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C and guaranteed by design and characterization for industrial temperature range.

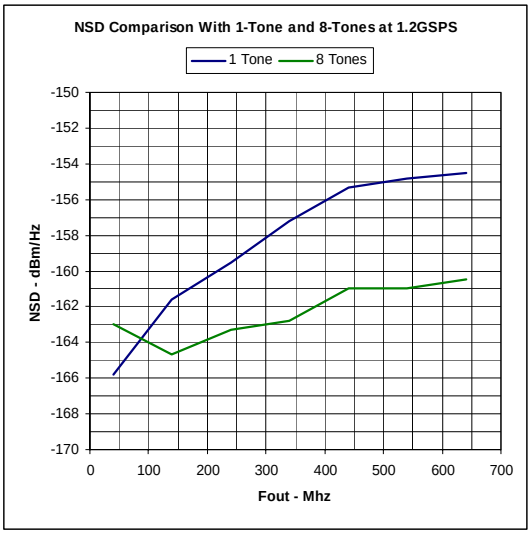


TPC1. AD9736, Typical INL

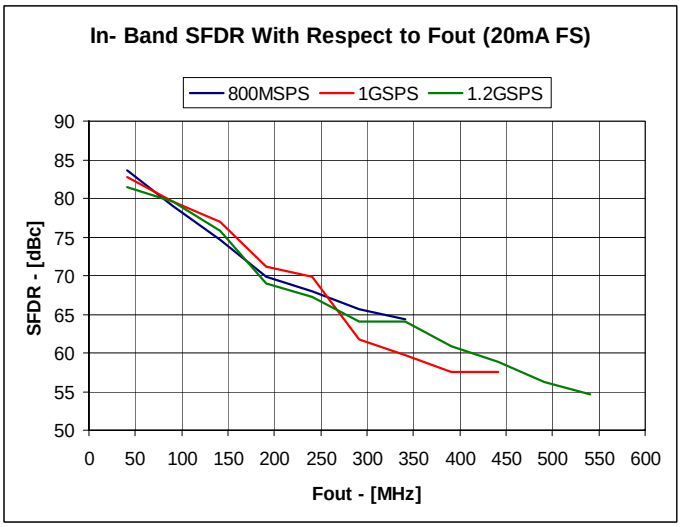


TPC2. AD9736, Typical DNL

TPC3. AD9736, 3rd Order IMD vs. Fout and Sample Rate



TPC4. AD9736, Noise Spectral Density vs Fout at 1.2GSPS



TPC5. AD9736, In Band SFDR vs Fout