a

Dual Channel, 14-Bit, 10 MSPS A/D Converter with Analog Input Signal Conditioning

PRELIMINARY TECHNICAL DATA AD10410

For current information contact (336) 605-4385

PERFORMANCE FEATURES

Dual, 10 MSPS minimum sample rate
- **Channel-channel matching, +/- .1% gain error**
- **Channel-channel isolation, >80dB**
- **DC-Coupled Signal conditioning included**

Selectable Bipolar Input Voltage Range (+/- 0.5V, +/- 1.0V, +/- 2.0V)
Gain flatness up to Nyquist: < 0.2dB
85dB Spurious-Free Dynamic Range
Straight binary output format
3.3 / 5V CMOS-Compatible Output Levels
.75W Per Channel
Industrial and Military Grade

APPLICATIONS
Phased Array Receivers
Communications Receivers
FLIR Processing
Secure Communications
GPS Anti-Jamming Receivers
Multichannel, Multimode Receivers

PRODUCT DESCRIPTION

The AD10410 is a full channel ADC solution with on-module signal conditioning for improved dynamic performance and fully matched channel-to-channel performance. The module includes two wide dynamic range AD9240 ADCs. Each AD9240 has a dc-coupled amplifier front end including a low distortion, high bandwidth amplifier, providing a high input impedance and gain, and driving a single to differential amplifier. The AD9240s have on-chip track-and- hold cirucutry and utilize an innovative multipass architecture to achieve 14-bit, 10MSPS performance. The AD10410 uses innovative high-density circuit design and laser-trimmed thin-film resistor networks to achieve exceptional matching and performance while still maintaining excellent isolation, and providing for significant board area savings.

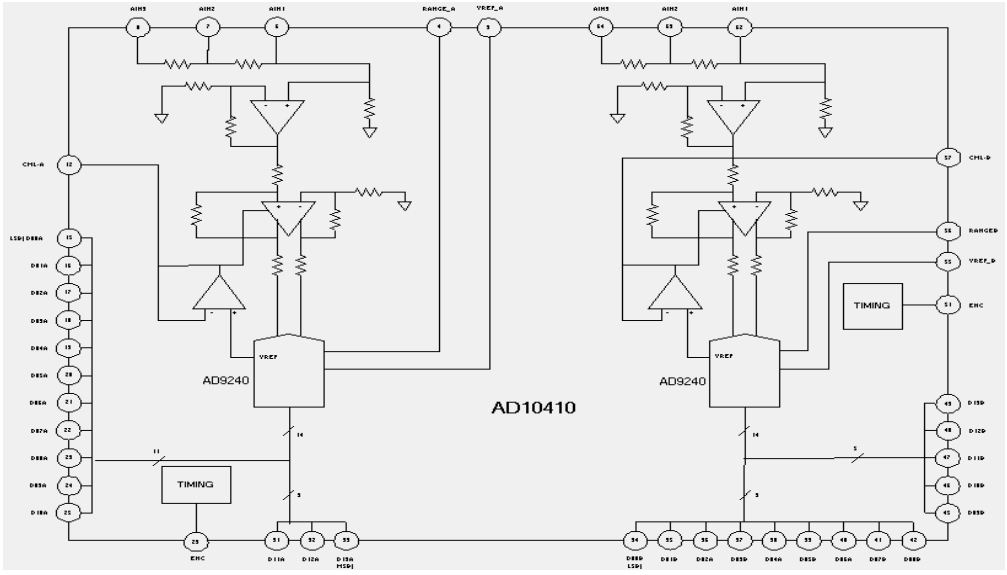
The AD10410 operates with +/- 5.0V for the Analog signal conditioning with a separate +5.0V/3.3V supply for the digital output phase. Each channel is completely independent allowing operation with independent Encode and Analog Inputs. The AD10410 also offers the user a choice of Analog Input Signal ranges to further minimize additional external signal conditioning, while still remaining general-purpose.

The AD10410 is packaged in a 68-lead Ceramic Gull Wing Package, footprint compatible with the earlier generation AD10242 (12-bit, 40 MSPS) and AD10265 (12-bit, 65MSPS). Manufacturing is done on Analog Devices, Inc. Mil-38534 Qualified Manufacturers Line (QML) and components are available up to Class-H (-55 to 125C).

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate of 10 MSPS.
2. Input amplitude options, user configurable.
3. Input signal conditioning included; both channels matched for gain.
4. Fully tested/characterized performance for full channel.
5. Footprint compatible family; 68-pin LCC.

FUNCTIONAL BLOCK DIAGRAM



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TARGET SPECIFICATIONS AD10410

Electrical Characteristics (AV_{CC}=5V; AV_{EE}=-5V; DV_{CC}=+3.3V applies to each ADC unless otherwise noted

Parameter	Temp	Test Level	Mil Sub-Group	AD10410BZ/QML-H Min	Typ	Max	Units
RESOLUTION					14		Bits
DC ACCURACY							
No Missing Codes	Full	VI	1,2,3		Guaranteed		
Offset Error	+25°C	I	1		±2.2		%FS
	Full	VI	2,3		±2.2		%FS
Offset Error Channel Match	Full	V			±0.1		%
Gain Error[1]	+25°C	I	1		±0.5		%FS
	Full	VI	2,3		±0.8		%FS
Gain Error Channel Match	Full	V			±0.1		%
ANALOG INPUT (A_{IN})							
Input Voltage Range							
$A_{IN}1$	Full	I	1,2,3		±0.5		V
$A_{IN}2$	Full	I	1,2,3		±1.0		V
$A_{IN}3$	Full	I	1,2,3		±2		V
Input Resistance							
$A_{IN}1$	Full	IV	12	99	100	101	Ω
$A_{IN}2$	Full	IV	12	198	200	202	Ω
$A_{IN}3$	Full	IV	12	396	400	404	Ω
Input Capacitance[2]	+25°C	IV	12	0	4.0	7.0	pF
Analog Input Bandwidth[3]	Full	V			30		MHz
ENCODE INPUT[4,5]							
High Level Input Voltage	Full	I	1,2,3		+3.5		V
Low Level Input Voltage	Full	I	1,2,3		+1.0		V
High Level Input Current (V_{IN}) = (AVCC)	Full	I	1,3,3		±10		µA
Low Level Input Current (V_{IN}) = (0 V)	Full	I	1,2,3		±10		µA
Input Capacitance					5		pF
SWITCHING PERFORMANCE							
Maximum Conversion Rate[6]	Full	VI	4,5,6	10			MSPS
Minimum Conversion Rate[6]	Full	V	12				MSPS
Aperture Delay (t_A)	+25°C	V			TBD		MSPS
Aperture Delay Matching	+25°C	V			TBD		ns
Aperture Uncertainty (Jitter)	+25°C	V			0.3		ps rms
ENCODE Pulse With High	+25°C	IV	12				ns
ENCODE Pulse With Low	+25°C	IV	12				ns
Output Delay (t_{OD})	Full	IV	12		TBD		ns
SNR							
Analog Input @ 1MHz	+25°C	V	4		73		dB
Analog Input @ 5MHz	Full	II	5,6		73		dB
SINAD[8]							
Analog Input @ 1MHz	+25°C	V	4		70		dB
Analog Input @ 5MHz	Full	II	5,6		70		dB

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Parameter	Temp	Test Level	Mil Sub-Group	AD10410BZ/QML-H Min	Typ	Max	Units
SPURIOUS-FREE DYNAMIC RANGE[9]							
Analog Input @ 1MHz	+25°C	V	4		85		dBFS
Analog Input @ 5MHz	Full	II	5,6		85		dBFS
Two-tone IMD Rejection[10]							
FI, F2@ -7 dBFS	Full	II	4,5,6			-80	dBFS
CHANNEL-TO-CHANNEL ISOLATION[11]	+25°C	IV	12		80dB		dB
TRANSIENT RESPONSE	+25°C	V			TBD		nS
LINEARITY							
Differential Non-Linearity	+25°C	IV	12		TBD		LSB
(Encode = 20MHz)	Full	IV	12		TBD		LSB
Intergal Nonlinearity	+25°C	V			TBD		LSB
(Encode = 20MHz)	Full	V			TBD		LSB
OVERVOLTAGE RECOVERY TIME[12]							
VIN = 2.0 x FS	Full	IV	12		TBD		nS
VIN = 4.0 x FS	Full	IV	12		TBD		nS
DIGITAL OUTPUTS							
High Level Output Voltage (I_{OH}) = 50µA)	Full	I	1,2,3		+4.5		V
Low Level Output Voltage (I_{OH}) = 0.5mA)	Full	I	1,2,3		+2.4		V
High Level Output Voltage (I_{OL}) = 1.6mA)	Full	I	1,3,3		+0.4		V
Low Level Output Voltage (I_{OL}) = 50µA)	Full	I	1,2,3		+0.1		V
Output Capacitance					5		pF
POWER SUPPLY							
AV_{CC} Supply Voltage	Full	VI		4.75	+5.0	5.25	V
I (AV_{CC}) Current	Full	V			TBD		mA
AV_{EE} Supply Voltage	Full	VI			-5.0		V
I (AV_{EE}) Current	Full	V			TBD		mA
DV_{CC} Supply Voltage	Full	VI		3.0	3.3V	5.25	V
I (DV_{CC}) Current	Full	V			TBD		mA
I_{CC} (Total) Supply Current	Full	I	1,2,3		TBD		mA
Power Dissipation (Total)	Full	I	1,2,3		1.5		W
Power Supply Rjection Ratio (PSRR)	Full	I	7,8			0.02	%FSR/%Vs
Pass Band Ripple to 10MHz		IV	12			0.2	dB

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Electrical Characteristics (AV_{CC}=5V; AV_{EE}=-5V; DV_{CC}=+3.3V applies to each ADC unless otherwise noted)

NOTES

1. Gain tests are performed on Ain2 input voltage range.
2. Input Capacitance spec. combines AD8037 die capacitance + Ceramic package capacitance.
3. Full Power Bandwidth is the frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis is reduced by 3dB.
4. All AC specifications tested by driving single ended ENCODE .
5. ENCODE driven by single-ended source; ENCODE bypassed to ground through .1 µF capacitor.; see "Encoding the AD10410" for details.
6. Minimum and Maximum conversion rates allow for variation in Encode Duty Cycle of 50% ±5%.
7. Analog Input signal power at -1 dBFS; signal-to-noise ratio (SNR) is the ratio of signal level to total noise (first 5 harmonics removed). Encode = 19MSPS.
8. Analog Input signal power at -1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics. Encode = 10MSPS.
9. Analog Input signal power swept from -1 dBFS to -60 dBFS; SFDR is ratio of converter fullscale to worst spur.
10. Both input tones at -7 dBFS; two tone intermodulation distortion (IMD) rejection is the ratio of either tone to the worst 3rd order intermod product. f1=2.5MHz ± 100kHz, 50kHz ≤ f1-f2 ≤ 300kHz.
11. Channel to Channel Isolation tested with A channel grounded and a Fullscale signal applied to B channel.
12. Input driven to 2x and 4x Ain1 range for > 4 clock cycles. Output recovers inband in specified time with Encode = 10MSPS.
13. Outputs are sourcing TBD µA.
14. Outputs are sinking TBD µA.

All specifications guaranteed within 100mS of initial power up regardless of sequencing.

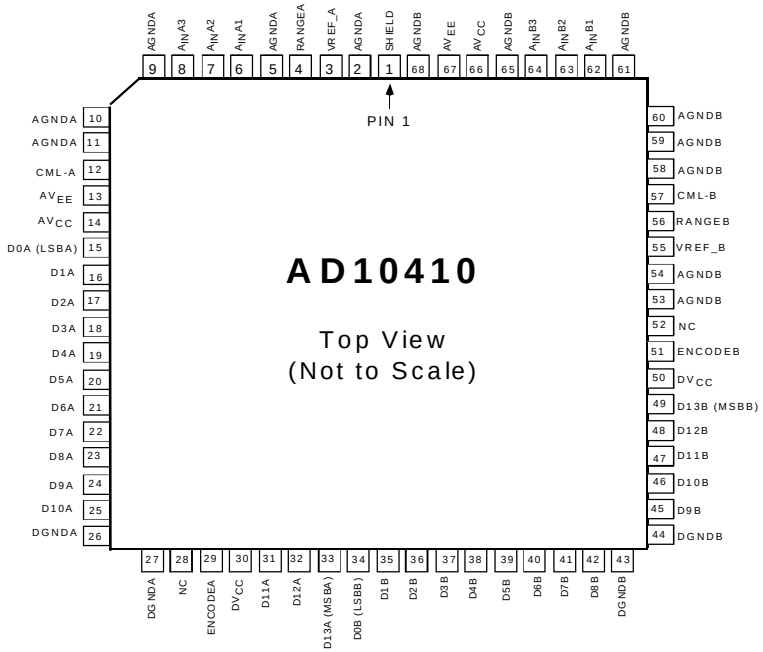
TEST LEVEL

I 100% Production Tested
II 100% Production Tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis
III Sample Tested only
IV Parameter is guaranteed by design and characterization testing
V Parameter is a typical value only
VI 100% production tested at temperature at 25°C: sample tested at temperature extremes

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1	SHIELD	Internal Ground Shield between channels
2,5,9-11	AGNDA	A Channel Analog Ground. A and B grounds should be connected as close to the device as possible
3	VREF_A	A Channel Internal Voltage Reference
6	$A_{IN}A1$	Analog Input for A side ADC (nominally ± 0.5V)
7	$A_{IN}A2$	Analog Input for A side ADC (nominally ± 1.0V)
8	$A_{IN}A3$	Analog Input for A side ADC (nominally ± 2.0V)
4	RANGEA	
12	CML-A	
13	AV_{EE}	Analog Negative Supply Voltage (nominally -5.0V)
14	AV_{CC}	Analog Positive Supply Voltage (nominally +5.0V)
26,27	DGNDA	A Channel Digital Ground
15-25, 31-33	D0A-D13A	Digital Outputs for ADC A. D0 (LSB)
28	NC	
29	ENCODEA	Data conversion initiated on rising edge of ENCODE input
30	DV_{CC}	Digital Positive Supply Voltage (nominally +5.0V / + 3.3V)
43,44	DGNDB	B Channel Digital Ground
34-42,45-49	D0B-D13B	Digital Outputs for ADC B. D0 (LSB)
53-54,58-61,65,68	AGNDB	B Channal Analog Ground. A and B grounds should be connected as close to the device as possible
50	DV_{CC}	Digital Positive Supply Voltage (nominally +5.0V / + 3.3V)
51	ENCODEB	Data conversion initiated on rising edge of ENCODE input
52	NC	
55	VREF-B	
57	CML-B	
56	RANGEB	B Channel Internal Voltage Reference
62	$A_{IN}B1$	Analog Input for B side ADC (nominally ± 0.5V)
63	$A_{IN}B2$	Analog Input for B side ADC (nominally ± 1.0V)
64	$A_{IN}B3$	Analog Input for B side ADC (nominally ± 2.0V)
66	AV_{CC}	Analog PositiveSupply Voltage (nominally +5.0V)
67	AV_{EE}	Analog Negative Supply Voltage (nominally -5.0V)

PIN CONFIGURATION
68-Lead Leaded Ceramic Chip Carrier



PLANNED GRADES

Model	Temperature Range	Package Description
AD10410BZ	-40°C to 85°C (Case)	68-pin Leaded Ceramic Chip Carrier
SMD/QML-H	-55°C to 125°C (Case)	68-pin Leaded Ceramic Chip Carrier
AD10410/PCB		Evaluation Board with AD10410BZ

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