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P1 98.2

SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE

DESCRIPTION

The 2SK1748 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance  
 $R_{DS(on)} = 0.11 \Omega$  ( $V_{GS} = 10 V, I_D = 4 A$ )  
 $R_{DS(on)} = 0.16 \Omega$  ( $V_{GS} = 4 V, I_D = 4 A$ )
- Low  $C_{iss}$   $C_{iss} = 850 pF$  TYP.
- Built-in G-S Gate Protection Diode

QUALITY GRADE

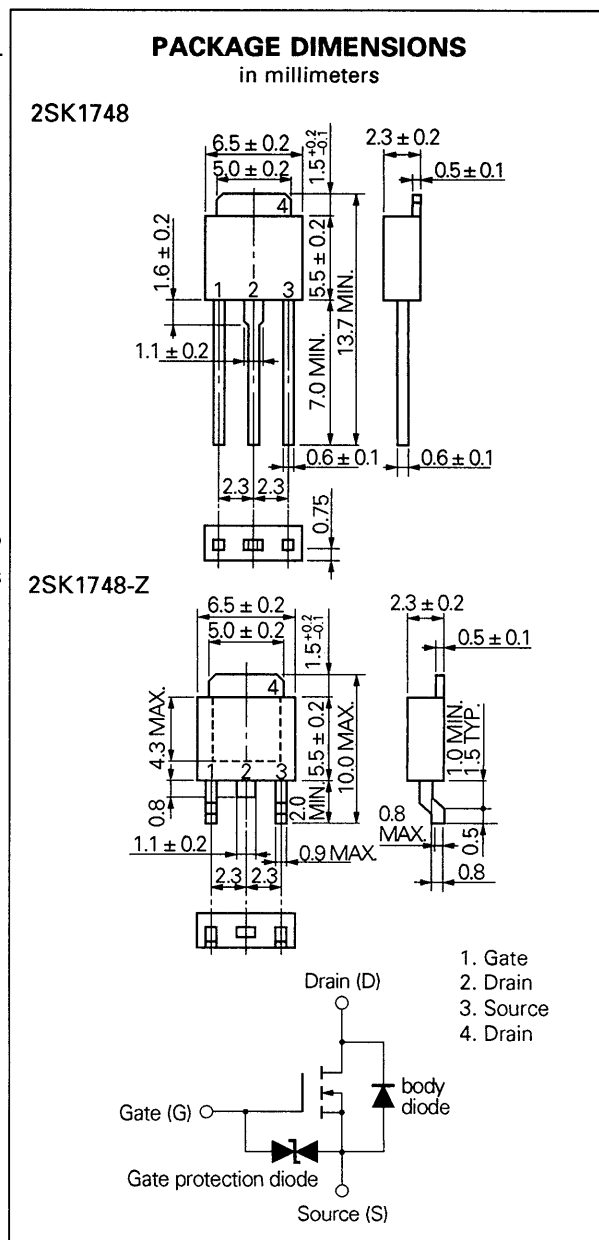
Standard

Please refer to "Quality grade on NEC Semi-conductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ C$ )

Drain to Source Voltage	$V_{DSS}$	60	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 8.0$	A
Drain Current (pulse)	$I_{D(pulse)^*}$	$\pm 24$	A
Total Power Dissipation ( $T_c = 25^\circ C$ )	$P_{T1}$	20	W
Total Power Dissipation ( $T_a = 25^\circ C$ )	$P_{T2}$	1.0	W
Channel Temperature	$T_{ch}$	150	$^\circ C$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ C$

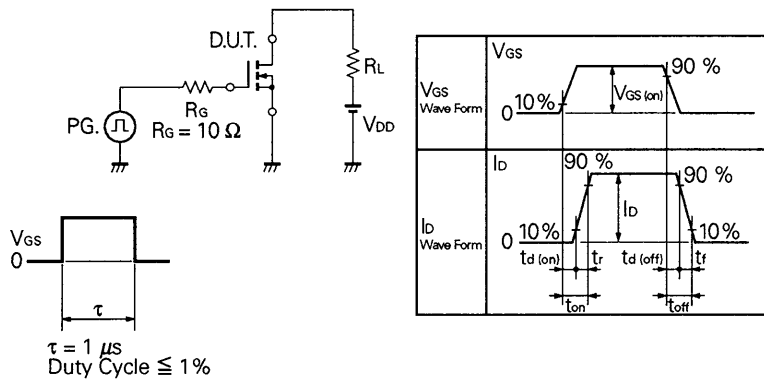
\*  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1\%$



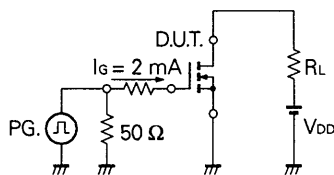
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.08	0.11	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4 A
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.11	0.16	Ω	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 4 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0		2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	5.0			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4 A
Drain Leakage Current	I <sub>DSS</sub>			10	μA	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		850		pF	V <sub>DS</sub> = 10 V V <sub>GS</sub> = 0 f = 1 MHz
Output Capacitance	C <sub>oss</sub>		350		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		100		pF	
Turn-On Delay Time	t <sub>d(on)</sub>		15		ns	V <sub>GS(on)</sub> = 10 V V <sub>DD</sub> = 30 V I <sub>D</sub> = 4 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 7.5 Ω
Rise Time	t <sub>r</sub>		60		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		100		ns	
Fall Time	t <sub>f</sub>		45		ns	
Total Gate Charge	Q <sub>G</sub>		3		nC	
Gate to Source Charge	Q <sub>GS</sub>		7		nC	V <sub>GS</sub> = 10 V I <sub>D</sub> = 8 A V <sub>DD</sub> = 48 V
Gate to Drain Charge	Q <sub>GD</sub>		25		nC	
Reverse Recovery Time	t <sub>rr</sub>		120		ns	I <sub>F</sub> = 8 A, V <sub>GS</sub> = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q <sub>rr</sub>		200		nC	

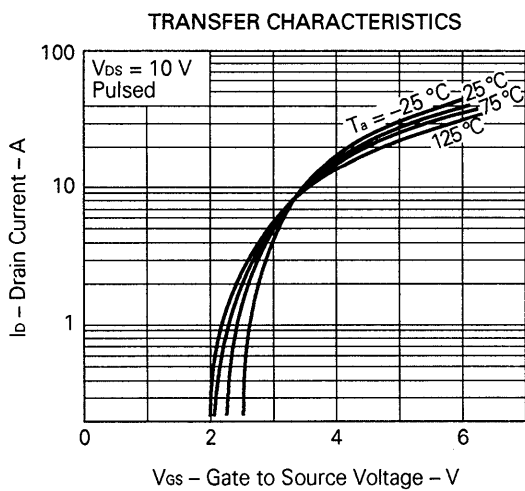
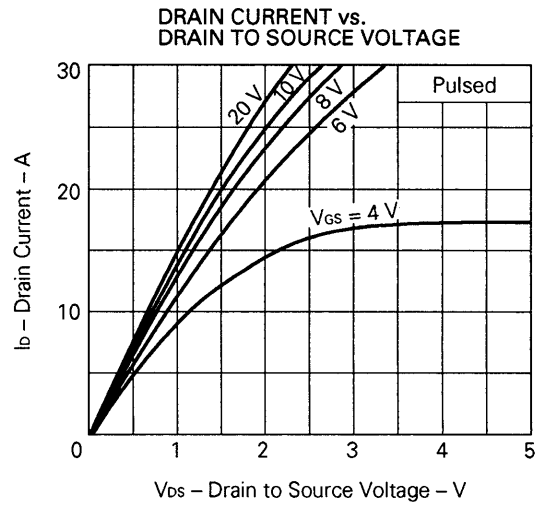
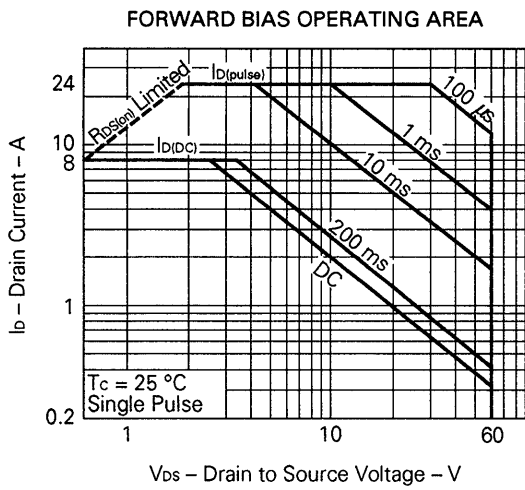
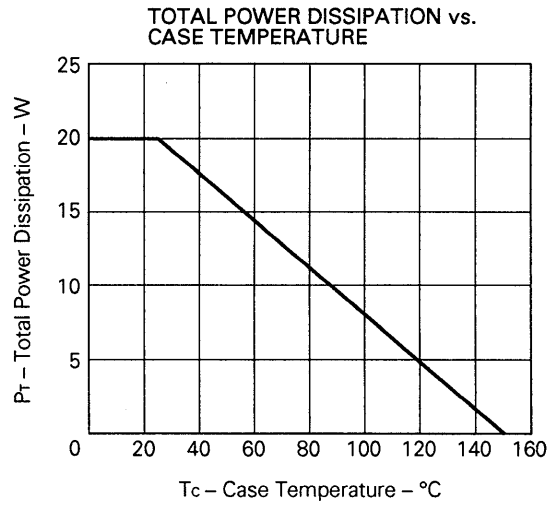
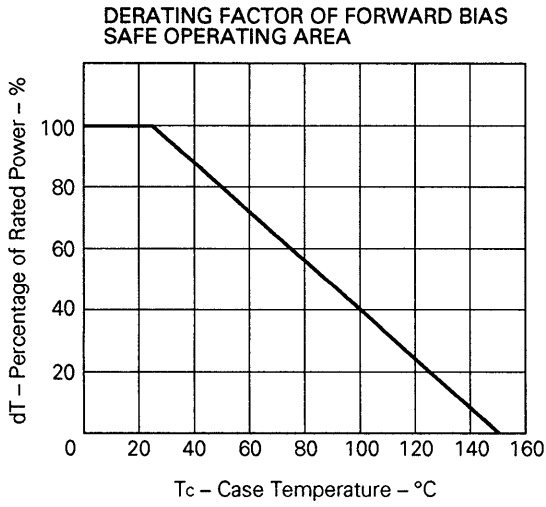
**Test Circuit 1: Switching Time**



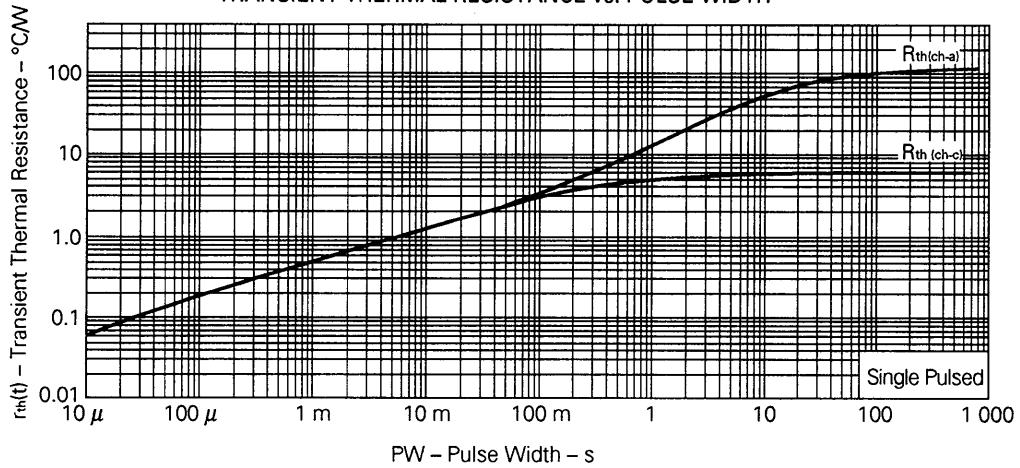
**Test Circuit 2: Gate Charge**



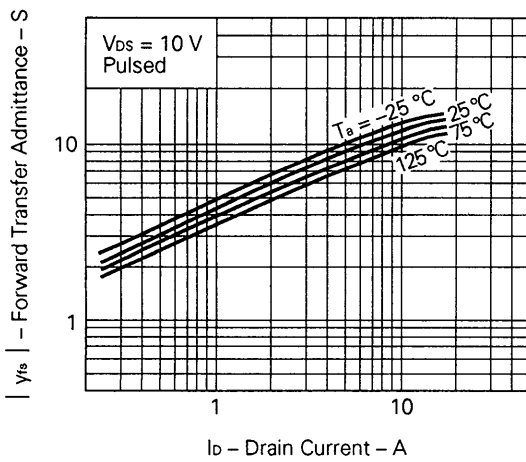
TYPICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)



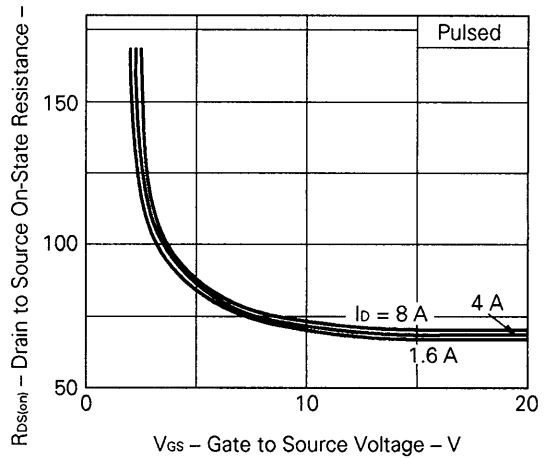
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



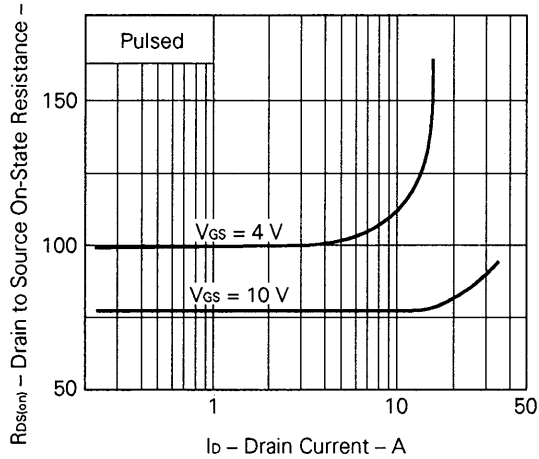
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



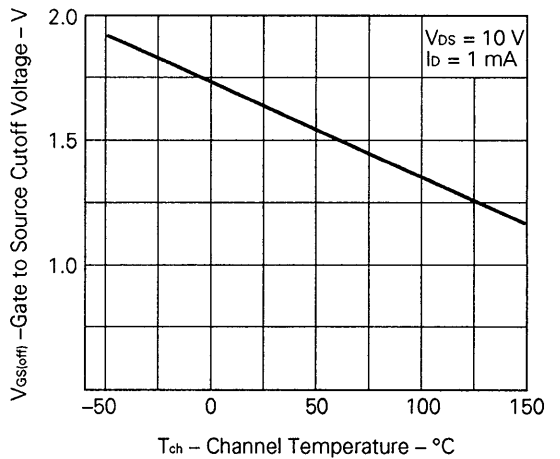
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

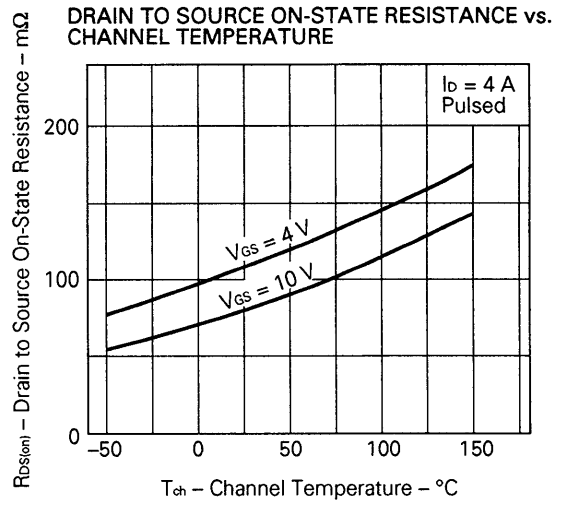
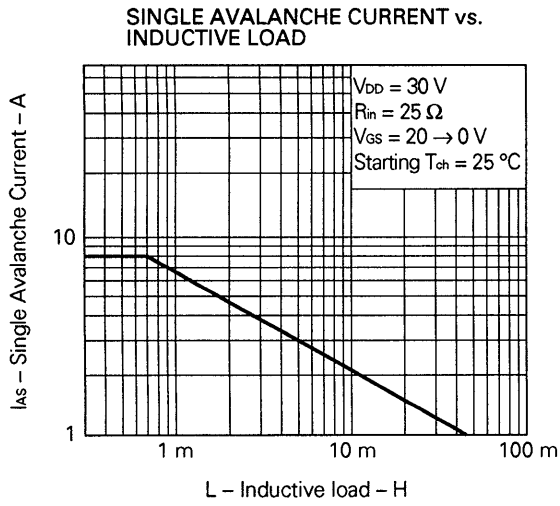


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.