# PM4354

# COMET-QUAD

# COMET-QUAD EVALUATOR BOARD DESIGN

**PRELIMINARY**

**ISSUE 2: JANUARY 2001**

## PUBLIC REVISION HISTORY

| Issue No. | Issue Date | Details of Change |
|---|---|---|
| 1 | Feb 2000 | Document created. |
| 2 | January 2001 | Revised Line Protection.<br>Updated Schematics.<br>Updated Layout.<br>Updated BOM. |

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# 1 INTRODUCTION

The COMET-QUAD Evaluator Board is part of the COMET-QUAD Evaluator Kit and allows for the evaluation and demonstration of PMC-Sierra's PM4354 COMET-QUAD device. It also provides a platform for the development and integration of software.

The COMET-QUAD Evaluator Board is configured, monitored, and powered through the PCI edge connector. Software drivers are available from PMC-Sierra, Inc. to fully control and utilize the COMET-QUAD Evaluator Board.

## 1.1 Purpose

The COMET-QUAD Evaluator Board is designed to assist engineers in designing their products using PMC-Sierra's COMET-QUAD device. The purpose of this document, hence, is to provide a detailed hardware specification for the COMET-QUAD Evaluator Board. The specification detailed here is sufficient to allow design implementation and verification.

## 1.2 Scope

This document describes the design for the COMET-QUAD Evaluator Board. A general description of the device is given, along with a block diagram for the design. A description for each of the functional blocks of the design is given followed by a detailed account of design issues, including physical and mechanical descriptions, implementation descriptions and layout.

## 1.3 Application

The COMET-QUAD device is suitable in the following applications:

- T1/E1 Wireless Digital Loop Carriers (DLC's) and Cellular Base Stations
- T1/E1 Internet Access Equipment
- T1/E1 Channel Service Units (CSU)
- T1/E1 Frame Relay Interfaces
- T1/E1 ATM Interfaces
- T1/E1 Multiplexers (CPE MUX)

- Digital Private Branch Exchanges (PBX)
- Digital Access Cross-Connect Systems (DACS) and Electronic DSX Cross-Connect Systems (EDSX)
- ISDN Primary Rate Interfaces (PRI)
- Test Equipment

Figure 1 illustrates the COMET-QUAD device in a wireless base transceiver station (BTS) application and Figure 2 illustrates the device in a V5.2 Interface Application.

**Figure 1: Wireless Base Station Application**

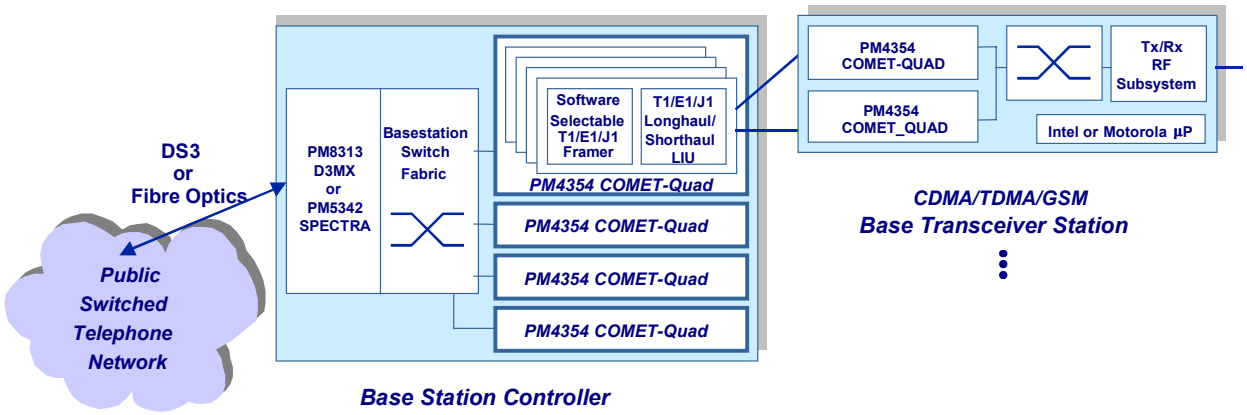
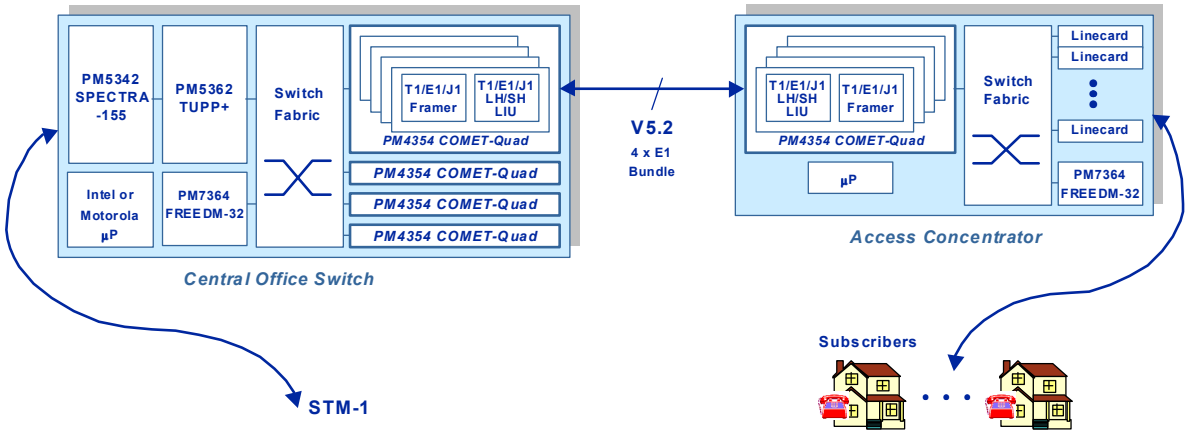



**Figure 2: V5.2 Interface Application**



# 2 FEATURES

## General

- PCI Interface – allows for microprocessor access to the COMET-QUAD via a host PC
- Provides a platform for the demonstration of the COMET-QUAD's functions and performance.
- Provides software-selectable E1, T1, J1 rate selection.

## T1 Mode

- Interface to 4 short haul and long haul T1 lines
- Frames to ESF and SF formats
- Integral HDLC controller for Facilities Data Link Support
- Serial PCM interfaces to each framer to support 1.544 Mbit/s ingress/egress system interfaces
- Detect loss of signal, pulse density violation, Red alarm, Yellow alarm, and AIS alarm
- Performance monitoring with accumulation of CRC-6 errors, framing bit errors, line code violations, and loss of frame events
- Provides synchronous backplane systems 8Mbit/s H-MVIP interfaces for access channel associated signaling (CAS) and common channel signaling (CCS) for each line
- Per channel payload loopback
- Automatic gain control to accommodate distances with up to 36 dB of cable attenuation at nominal conditions using PIC 22 gauge cable emulation
- Programmable Line build outs of DSX-1 as well as CSU of –7.5dB, -15dB and –22dB
- Line interface capable of generating G.703 wave shapes for 100Ω T1 lines

- Provides a programmable PRBS test pattern generator, receiver and analyzer.

**E1 Mode**

- Interface to 4 short haul and long haul E1 lines
- Frames to FAS, CAS and CRC-4 formats
- Integral HDLC controller for Facilities Data Link Support
- Detect loss of signal, loss of frame, loss of signaling multiframe and loss of CRC
- Performance monitoring with accumulation of CRC-4 errors, far end block errors, framing bit errors, and line code violation
- Provides synchronous backplane systems 8Mbit/s H-MVIP interfaces for access channel associated signaling (CAS) and common channel signaling (CCS) for each line
- Per channel payload loopback
- Automatic gain control to accommodate distances with up to 36 dB of cable attenuation at nominal conditions using PIC 22 gauge cable emulation
- Line interface capable of generating G.703 wave shapes for 120Ω E1 lines
- Provides a programmable PRBS test pattern generator, receiver and analyzer.

# 3 GENERAL DESCRIPTION OF THE COMET-QUAD EVALUATOR KIT

## 3.1 The COMET-QUAD Evaluator Kit

The COMET-QUAD Evaluator Kit is a self-contained hardware and software reference design tool, designed to operate on a Pentium-based PC running Windows 95/98/2000/NT. The kit provides a platform for the engineers to develop and integrate software with a state-of-the-art T1/E1/J1 design.

## 3.2 Hardware

The kit is supplied with a 4 channel COMET-QUAD Evaluator Board that has been developed to fit into a PCI-based desktop computer. This board consists of a PM4354 COMET-QUAD device, the necessary interface circuitry, magnetics, and line protection for long haul and short haul operation in either T1 or E1 mode. The board is configured, monitored, and powered through the PC's motherboard.

## 3.3 Software

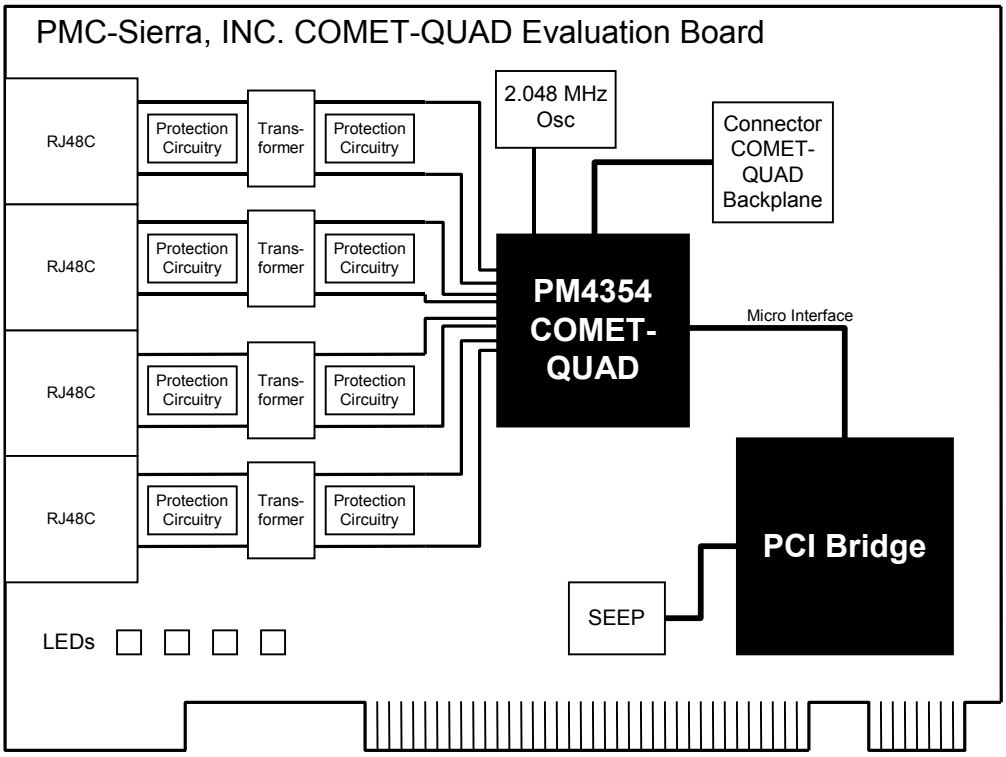
The kit contains an interactive program, complete with a graphical user interface (GUI), and a set of scripts to configure the COMET-QUAD device. The software, installed from the kit's CD-ROM, provides a visual interface to control and monitor the COMET-QUAD functions. Direct access to the COMET-QUAD device is provided to read or write any of the COMET-QUAD registers, perform a hardware reset of the COMET-QUAD, and observe the status of the hardware interrupt pin of the COMET-QUAD.

# 4 BLOCK DESCRIPTION

## 4.1 Block Diagram

The following section describes in detail the function of each hardware block shown in Figure 3.

**Figure 3: Block Diagram**




## 4.2 COMET-QUAD

The PM4354 Four Channel Combined E1/T1/J1 Transceiver and Framer (COMET-QUAD) is a feature-rich monolithic integrated circuit suitable for use in long haul and short haul T1, J1 and E1 systems with a minimum of external circuitry. The COMET-QUAD is software configurable, allowing feature selection without changes to external wiring.

Analog circuitry is provided to allow direct reception of long haul E1 and T1 compatible signals with up to 36 dB cable loss (at 1.024 MHz in E1 mode) or up

to 36 dB cable loss (at 772 kHz in T1 mode) using a minimum of external components. Typically, only line protection, a transformer and a line termination resistor are required.

The COMET-QUAD recovers clock and data from the line and frames to incoming data. In T1 mode, it can frame to SF and ESF signal formats. In E1 mode, the COMET-QUAD frames to basic G.704 E1 signals and CRC-4 multiframe alignment signals, and automatically performs the G.706 interworking procedure. AMI, HDB3 and B8ZS line codes are supported.

The COMET-QUAD supports detection of various alarm conditions such as loss of signal, pulse density violation, Red alarm, Yellow alarm, and AIS alarm in T1 mode and loss of signal, loss of frame, loss of signaling multiframe and loss of CRC multiframe in E1 mode. The COMET-QUAD also supports reception of remote alarm signal, remote multiframe alarm signal, and alarm indication signal in E1 mode. The presence of Yellow and AIS patterns in T1 mode and remote alarm and AIS patterns in E1 mode is detected and indicated. In T1 mode, the COMET-QUAD integrates Yellow, Red, and AIS alarms as per industry specifications. In E1 mode, the COMET-QUAD integrates Red and AIS alarms.

Performance monitoring with accumulation of CRC-6 errors, framing bit errors, line code violations, and loss of frame events are provided in T1 mode. In E1 mode, CRC-4 errors, far end block errors, framing bit errors, and line code violation are monitored and accumulated.

The COMET-QUAD provides one receive HDLC controller per channel for the detection and termination of messages in the ESF facility data link (T1), national use bits (E1), or in any arbitrary timeslot (T1 or E1). In T1 mode, the COMET-QUAD also detects the presence of in-band loop back codes and ESF bit oriented codes. Detection and optional debouncing of the 4-bit Sa-bit codewords defined in ITU-T G.704 and ETSI 300-233 is supported. An interrupt may be generated on any change of state of the Sa codewords.

Dual (transmit and receive) elastic stores for slip buffering and rate adaptation to backplane timing are provided, as is a signaling extractor that supports signaling debounce, signaling freezing, idle code substitution, digital milliwatt tone substitution, data inversion, and signaling bit fixing on a per-channel basis. Receive side data and signaling trunk conditioning is also provided.

In T1 mode, the COMET-QUAD generates framing for SF and ESF formats. In E1 mode, the COMET-QUAD generates framing for a basic G.704 E1 signal. The signaling multiframe alignment structure and the CRC multiframe structure may be optionally inserted. Framing can be optionally disabled.

Internal analog circuitry allows direct transmission of long haul and short haul T1 and E1 compatible signals using a minimum of external components. Typically,

only line protection, a transformer and an optional line termination resistor are required. Digitally programmable pulse shaping allows transmission of DSX-1 compatible signals up to 655 feet from the cross-connect, E1 short haul pulses into 120 ohm twisted pair or 75 ohm coaxial cable, E1 long haul pulses into 120 ohm twisted pair as well as long haul DS-1 pulses into 100 ohm twisted pair with integrated support for LBO filtering as required by the FCC rules. In addition, the programmable pulse shape extending over 5-bit periods allows customization of short haul and long haul line interface circuits to application requirements.

In the transmit path, the COMET-QUAD supports signaling insertion, idle code substitution, digital milliwatt tone substitution, data inversion, and zero code suppression on a per-channel basis. Zero code suppression may be configured to Bell (bit 7), GTE, or DDS standards, and can also be disabled. Transmit side data and signaling trunk conditioning is also provided. Signaling bit transparency from the backplane may be enabled.

The COMET-QUAD provides one transmit HDLC controller per channel. These controllers may be used for the transmission of messages in the ESF data link (T1), national use bits (E1), or in any timeslot (T1 or E1). In T1 mode, the COMET-QUAD can be configured to generate in-band loop back codes and ESF bit oriented codes. In E1 mode, transmission of the 4-bit Sa codewords defined in ITU-T G.704 and ETSI 300-233 is supported.

To provide for V5 applications where up to three HDLC channels are contained in each E1, the COMET-QUAD provides a CCS H-MVIP interface. This interface allows the HDLC channels to be inserted or extracted for external processing.

Each channel of the COMET-QUAD can generate a low jitter transmit clock from a variety of clock references, and also provides jitter attenuation in the receive path. A low jitter recovered T1 clock can be routed outside the COMET-QUAD for network timing applications.

Serial PCM interfaces to each T1/E1 framer allow 1.544 Mbit/s or 2.048 Mbit/s backplane receive/backplane transmit system interfaces to be directly supported. Tolerance of gapped clocks allows other backplane rates to be supported with a minimum of external logic.

For synchronous backplane systems, 8.192 Mbit/s H-MVIP interfaces are provided for access to PCM data, channel associated signaling (CAS) and common channel signaling (CCS) for each T1 or E1. The CCS signaling H-MVIP interface is independent of the 64 Kbit/s PCM and CAS H-MVIP access. The use of the H-MVIP interface requires that common clocks and frame pulse be used along with T1/E1 elastic stores.

The COMET-QUAD is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be masked and acknowledged through the microprocessor interface.

For a complete description of the COMET-QUAD, please refer to PMC-Sierra's COMET-QUAD data sheet, PMC-1990315 [1].

## 4.3 PCI Bridge

The PCI Bridge used is PLX Technology's PCI9050 PCI Bus Target Interface Chip. The PCI9050 provides a target only interface, and as such does not initiate PCI bus transactions.

The PCI9050 has a 16 long word write FIFO and 8 long word read FIFO allowing the PCI bus to burst data to and from the COMET-QUAD. The local address space is configured to be 32-bit non-multiplexed, big endian, non-burst, and non-prefetchable. Even though the COMET-QUAD has only an 8-bit data bus, the PCI9050 is configured as a 32-bit data bus. This was done to simplify the hardware design. Prefetching is not possible in this application because the COMET-QUAD has a number of registers with read side affects (e.g. interrupt status registers).

The local bus is clocked at 33MHz by looping the buffered PCI clock output (BCLKO) available from the PCI9050 back to the local bus clock input.

The local address spaces are allocated in the following fashion:

**Table 1 PCI9050 Local Address Space Allocation**

| Address Space | Function |
|---|---|
| 0 | COMET-QUAD Registers |
| 1 | unused |
| 2 | unused |
| 3 | unused |

Please refer to the PCI9050 datasheet [5] for more information.

## 4.4 SEEP

The NM93CS46 Serial EEPROM from National Semiconductor is used to store configuration information for the PCI9050 bridge. This specific SEEP (or

equivalent) is required by PCI9050 because it supports sequential read operations.

The SEEP is 1Kbit deep, 800 bits of which are occupied by the PCI9050 configuration data, leaving 224 bits (28 bytes) unused.

Refer to the PCI9050 datasheet [5] for information on the format of the configuration data stored in the SEEP.

## 4.5 Oscillators

The COMET-QUAD can run in either T1 or E1 mode. In T1 mode, oscillator Y1 should be populated with a 1.544 MHz oscillator. In E1 mode, oscillator Y1 should be populated with a 2.048 MHz oscillator. The COMET-QUAD can also optionally run in T1 mode with a 2.048 MHz oscillator.

## 4.6 Transmit and Receive Line Interface

A transmit and receive line interface is required for each of the 4 channels.

Each transmit and receive line interface consists of line connectors, line protection circuitry and magnetics.

The magnetics used on this design is a quad package that contains both a receive and transmit transformer. Both the receive and transmit transformers have a 1:2.42 turns ratio with the “1” always on the chip side. Please refer to Table 16 for a list of manufacturers.

The evaluator board provides one set of line interface connectors, a RJ-48C, for the receive and transmit of T1/E1 signals to and from the COMET-QUAD device for each channel. The RJ48C has been provided according to the ANSI T1.403 standard for a Universal Service Ordering Code (USOC) connector. Table 2 below details the pinout for the RJ-48C connector.

**Table 2: RJ-48C Pinout**

| Pin | Signal |
|---|---|
| 1 | RXRING |
| 2 | RXTIP |
| 3 | N.C. |
| 4 | TXRING |
| 5 | TXTIP |

| | |
|---|---|
| 6 | N.C. |
| 7 | N.C. |
| 8 | N.C. |

## 4.7 Line Termination

The line interface provides one termination scheme for both T1 and E1 rates. A termination of 110Ω is used to allow the interface to be compatible with both 100Ω T1 and 120Ω E1. This provides a software switchable reference board for both T1 and E1 by simply configuring the COMET-QUAD device.

## 4.8 Protection Circuitry

The protection circuitry prevents damage to telecommunications equipment caused by over-voltage and over-current power surges due to lightning strikes and AC power cross disturbances.

The circuit is composed of two sections. The primary circuit protection consists of circuit protection for digital transmission equipment. The circuit is a proven solution that is currently used in the industry today. The configuration has passed Bellcore GR 1089-CORE, FCC Part 68 and UL 1459 & 1950.

The TECCOR F1250T Telelink Fuse used in combination with the TECCOR P1800SC SIDACtor and P0720SC SIDACtor provide a solution for the regulatory requirements without the use of any additional series resistance. The two fuses provide over current protection and the three SIDACtors provide over voltage protection.

The SIDACtors provide transient over voltage protection. In the standby mode, the device exhibits high off-state impedance eliminating excessive leakage currents and appears transparent to the circuits they protect. When the voltage across the device exceeds the switching voltage, SIDACtors will crowbar and simulate a short circuit. During this state, current gets driven into the ground, thereby reducing some of the voltage that shows across the transformer and eventually at the equipment. The device stays in this state until the current flowing through the SIDACtor falls below the holding current of the device. When this occurs, the device resets and returns to its' high off-state impedance.

Secondary protection is provided using a combination of transformers and a diode array. The quad transformer with diode array module from Pulse further clamps any voltages.

The transformers provide 1500Vrms line isolation and serves to impedance match the lines to the transceiver line interface. Any remaining high positive or high negative voltage signals are further clamped by the diode array configuration. If the positive voltage signal is larger than the reference voltage plus the diode voltage, then the top diode becomes forward biased and steers the excess voltage into the power supply. If the negative voltage signal exceeds the diode voltage, then the bottom diode becomes forward biased and directs the excess negative voltage signals to ground. The transformer with diode array module chosen for this application is a quad package that contains one set of receive and transmit transformer and diode array for each of the four channels.

Figure 6 shows an external protection circuit for designs required to meet major surge immunity and electrical safety standards including Bellcore GR 1089-CORE, FCC Part 68 and UL 1459 & 1950. This circuit uses a part from Pulse that combines eight transformers (4 transmit and 4 receive) and the diode array module (equivalent to the diode array provided by Semtech) into a single module. This is an alternative way of implementing the circuit while reducing the number of required components.

**Figure 6: External Analog Interface Circuit for One Channel**

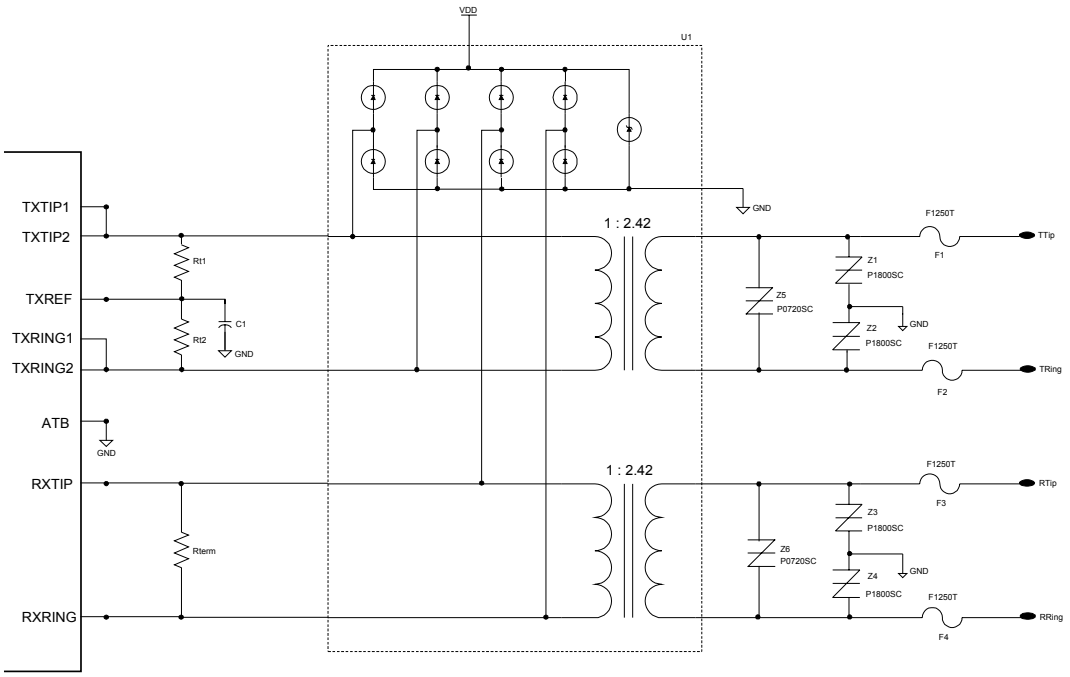


**Table 5: External Components Description**

| Component | Description | Part Number | Source |
|---|---|---|---|
| Rt1 & Rt2 | Typically 12.7Ω ±1% Resistors | | |
| Rterm | 18.2Ω ±1% Resistor for T1 & 120Ω E1 13Ω ±1% Resistor for 75Ω E1 (assuming a 1:2.42 transformer) | | |
| C1 | 4.7µF±10% Capacitor | | |
| F1 – F4 | Surge Resistant, Time Lag Fuse | F1250T Telelink | Teccor |
| Z1 – Z4 | Bi-directional Transient Surge Protectors | P1800SC | Teccor |
| Z5, Z6 | Bi-directional Transient Surge Protectors | P0720SC | Teccor |
| D1 | Surge Protector Diode Array | SRDA3.3-4 | Semtech |
| T1&T2 | Generally 1:2.42CT Transformers | 50436 (single)<br>T1137<br>TG23-1505NS (single)<br>TG23-1505N1 (dual) | Midcom<br>Pulse<br>Halo<br>Halo |
| U1 (replaces both D1 and T1 & T2) | Combined 1:2.42CT Transmit (quantity=4) and Receive (quantity=4) Transformers and Surge Protector Diode Array | T9021 | Pulse |

## 4.9 Power Supply

The COMET-QUAD evaluator design contains components that operate at 2.5V, 3.3V, or 5V, referenced to ground. The 5V supply is provided to the board through the PCI connector. The 2.5V and 3.3V supply is generated on the board via DC-DC voltage regulators.

It is recommended that 5V power is provided before both 2.5V and 3.3V power to avoid device latchup. Please refer to the COMET-QUAD datasheet [1] for further details of powering up the COMET-QUAD device.

## 4.10 PCI Edge Connector

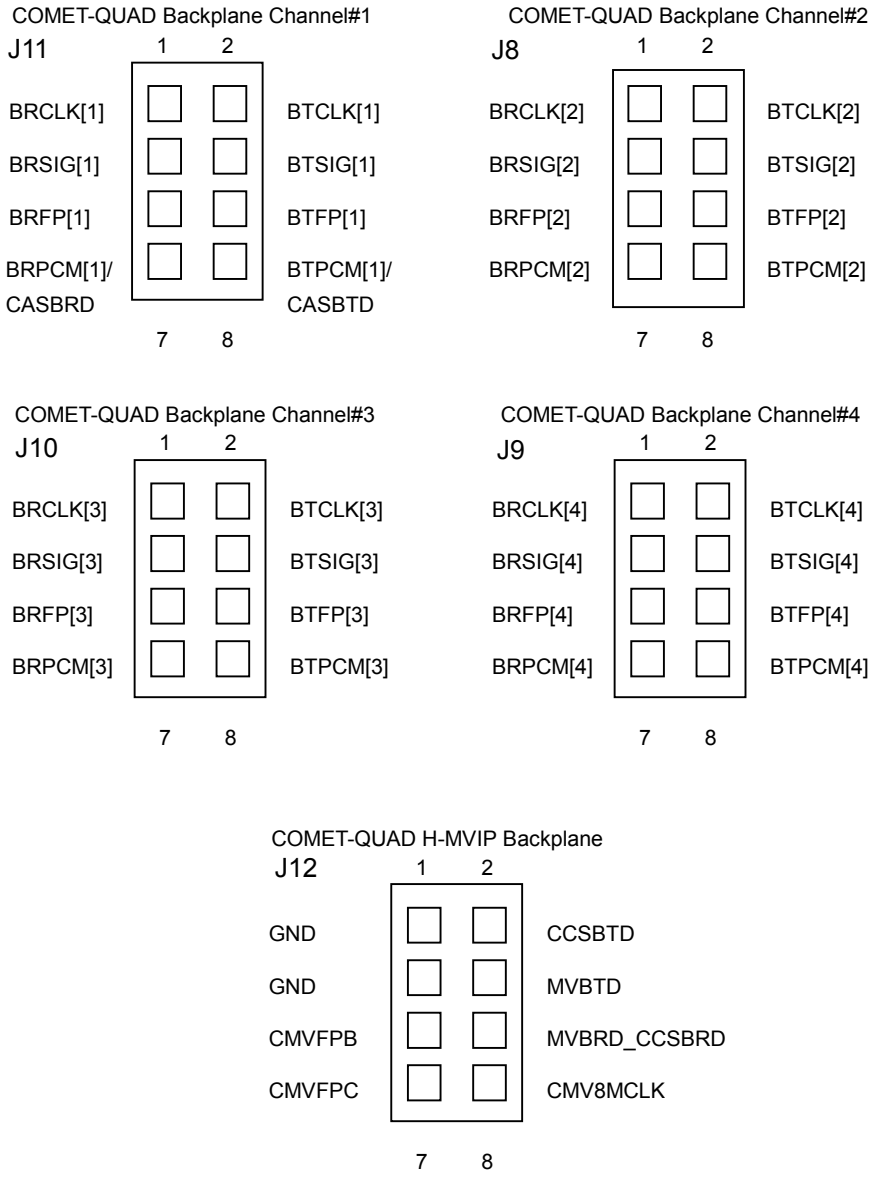
The PCI Edge Connector has been implemented as a standard Universal, 32 bit PCI connector. The system board designer must leave all reserved and Vio pins unconnected as voltage rail safety precautions. The universal expansion board is capable of detecting the signaling environment in use, and adapting itself to that environment accordingly. It can be plugged into either 3.3V or 5.0V connector type.

## 4.11 Backplane Bus Connector

The Backplane bus connectors, as shown in Figure 7, provide system side serial clock and data access as well as H-MVIP access for up to four T1 or E1 streams to the COMET-QUAD. This is provided to allow for easy access to the backplane signals. By simply connecting across the jumpers(connecting pins 1 to 2, 3 to 4, etc), the backplane channel connectors also allow for easy configuration of external payload loopback. The H-MVIP backplane connectors, on the other hand, provide useful input/output test ports for testing the system signals.

Note that when in H-MVIP mode, BTPCM[1] and BRPCM[1] act as CASBTD and CASBRD respectively.

## Figure 7: System Bus Connectors



# 5 DESIGN ISSUES

The following sections describe design considerations of the evaluator board.

## 5.1 COMET-QUAD Design Considerations

### 5.1.1 Power Supply

Analog power pins must be applied after VDD or they must be current limited to the maximum latch-up current of 100mA. A simple solution is to use a small filtering network between the VDD and the analog power pins to delay power to each AVD pin.

### 5.1.2 Decoupling

A 0.01μF capacitor is required for every two digital power pins, placed between alternating power and ground. A 0.1μF capacitor required for every two digital power pins, placed between alternating power and ground. The capacitors should be placed as close to the actual pin as possible.

The AVD pins require a filtering network between the GND plane and the 3.3V plane. The network is a single RC network with the resistor between the 3.3V plane and the AVD pin and the capacitor from the AVD pin to the GND plane. Please refer to the schematics and bill of materials for component values.

### 5.1.3 Internal FDL Transmitter

It is important to note that access rate to the TDPR registers is limited by the rate of the XCLK crystal clock input. Consecutive accesses to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register should be accessed (with respect to WRB rising edge and RDB falling edge) at a rate no faster than the XCLK clock rate. (In T1 mode with a 2.048 MHz XCLK reference, accesses should be no faster than XCLK x 193/256.) This time is used by XCLK to sample the event, write the FIFO, and update the FIFO status. Instantaneous variations in the XCLK clock frequency (e.g. jitter in XCLK) must be considered when determining the procedure used to read and write the TDPR registers.

Upon reset of the COMET-QUAD, the TDPR should be disabled by setting the EN bit in the TDPR Configuration Register to logic 0 (default value). An HDLC all-ones idle signal will be sent while in this state. The TDPR is enabled by setting the EN bit to logic 1. The FIFOCLR bit should be set and then cleared to initialize the TDPR FIFO before the TDPR is ready to transmit.

### 5.1.4 Internal Data Link Receiver

It is important to note that the access rate to the RDLC registers is limited by the rate of the XCLK crystal clock input. Consecutive accesses to the RDLC Status and RDLC Data registers should be accessed (with respect to WRB rising edge and RDB falling edge) at a rate no faster than 8/10 that of the XCLK clock rate. (In T1 mode with a 2.048 MHz XCLK reference, accesses should be no faster than XCLK x (193 x 8)/2560.) This time is used by XCLK to sample the event and update the FIFO status. Instantaneous variations in the XCLK clock frequency (e.g. jitter in XCLK) must be considered when determining the procedure used to read RDLC registers.

On power up of the system, the RDLC should be disabled by setting the EN bit in the Configuration Register to logic 0 (default value). The RDLC Interrupt Control register should then be initialized to enable the INTB output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic 1, the RDLC Status register must be continuously polled to check the interrupt status (INTR) bit.

### 5.1.5 Per-Channel Serial Controllers

Proper initialization of the internal registers must be performed to eliminate erroneous control data from being produced on the outputs of the TPSC (RPSC) block. The output control streams should be disabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register to logic 0. Then, all 96 locations of the TPSC (RPSC) must be filled with valid data. Finally the output streams can be enabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register to 1.

Direct access mode to the TPSC or RPSC is not used in the COMET-QUAD. However, direct access mode is selected by default whenever the COMET-QUAD is reset. The IND bit within the TPSC and RPSC Configuration Registers must be set to logic 1 after a reset is applied.

### 5.1.6 T1/E1 Framer Loopback Modes

The COMET-QUAD provides four loopback modes to aid in network and system diagnostics. The network loopbacks (Payload and Line) can be initiated at any time via the µP interface, but are usually initiated once an inband loopback activate code is detected. The system Diagnostic Digital loopback can be initiated at any time by the system via the µP interface to check the path of system data through the framer. The Per-DS0 loopback permits the payload to be looped-back on a per-DS0 basis to allow network testing without taking an entire link off-line. Please refer to Table 6 for a summary of the loopback

operations. Note that only one of Payload Loopback, Line Loopback and Diagnostic Digital Loopback can be enabled at any one time.

**Table 6: COMET-QUAD Loopback Modes**

| Loopback Mode | Addr | Register | Bit | Set |
|---|---|---|---|---|
| Line Loopback | 00AH,10AH, 20AH,30AH | Master Diagnostics Register | LINELB | Logic 1 |
| Payload Loopback | 00AH,10AH, 20AH,30AH | Master Diagnostics Register | PAYLB | Logic 1 |
| Per-Channel Loopback | 06FH,16FH, 26FH,36FH | TPSC Internal Register | LOOP | Logic 1 |
| Per-Channel Loopback | 06CH,16CH, 26CH,36CH | TPSC Configuration Register | PCCE | Logic 1 |
| Diagnostic Digital Loopback | 00AH,10AH, 20AH,30AH | Master Diagnostics Register | DDLB | Logic 1 |

## 5.2 PCI Bridge

### 5.2.1 Dual Environment Compliance

The PCI-9050 must use I/O buffers that can be compliant with either the 5.0V or 3.3V signaling environment. While there are multiple buffer implementations that can achieve this dual environment compliance, it is intended that they be dual voltage buffers – i.e. capable of operating from either power rail. They should be powered from “I/O” designated power pins on PCI connectors that will always be connected to the power rail associated with the signaling environment in use. This means that in the 5.0V signaling environment, these buffers are powered on the 5.0V rail. When the board is plugged into a 3.3V connector, these buffers are powered on the 3.3V rail. This enables the COMET-QUAD Evaluator Board to be compliant with either signaling environment.

### 5.2.2 PCI 9050 Initialization

The PCI-9050 is used in the Evaluator Board to provide a compact high performance PCI bus target (slave) interface to the PCI bus.

During power up, the PCI RST# signal resets the default values of the PCI 9050-1 internal registers. In return, the PCI 9050 outputs the local reset signal (LRESET#) and checks for the existence of the serial EEPROM. If a serial EPROM is installed, and the first 16-bit word is not FFFF, the PCI 9050 loads the

internal registers from the serial EEPROM. Otherwise, default values are used. The PCI 9050 configuration registers can be written only by the optional serial EEPROM or the PCI host processor. During the serial EEPROM initialization, the PCI 9050 response to PCI target accesses is RETRYs.

### 5.2.3 Internal Register Access

The PCI 9050 chip provides several internal registers, allowing maximum flexibility in bus interface design and performance. All of the PCI and the local configuration registers are accessible from the PCI bus and EEPROM.

### 5.2.4 Direct Data Transfer Modes

The PCI host processor can directly access devices on the local bus for reads and writes. Configuration registers within the PCI 9050 control decoding and remapping of these accesses to local address space.

## 5.3 Line Protection

Line protection circuitry is implemented to protect the Evaluator Board from damage caused by over-voltage and over-current power surges due to lightning strikes and power cross disturbances.

Using the combination of the F1250T Telelink fuse, the P1800SC SIDACtor and the P0720SC SIDACtor eliminates the need for additional series line resistance. The elimination of the additional resistance allows the signal to maintain its' integrity. The resistance of the F1250T Telelink fuse is $0.109\Omega \pm 15\%$. The low resistance results in negligible signal degradation, which allows the signal to remain within the required pulse shape template. Another advantage resulting from the removal of additional series line resistance is that it enables longer loop lengths. Adding the F1250T fuse is an economical solution. The fuse eliminates the need for costly power resistors and PTCs.

Adding the P1800SC and P0720SC SIDACtors results in absolute surge protection regardless of the available surge current and the rate of applied voltage (dV/dt). The SIDACtor also can not be damaged by voltage, eliminates hysteresis and heat dissipation typically found with a clamping device, eliminates voltage overshoot caused by fast rising transients, and has negligible capacitance. The fuse is robust enough to live through lightning surges without causing unwanted openings, but interrupts correctly during situations involving power cross. The P1800SC SIDACtors are chosen because of the switching voltage of 220V.

The diode array protects high-speed data interfaces from over voltages caused by ESD (electrostatic discharge), EFT (electrical fast transients), and lightning. During transient conditions, the diodes steer the transient to either the positive side of the power supply line or to the ground. The TVS diode used in the array is very important because it prevents over voltage on the power line, thereby protecting components that exist further down the line. Also, the capacitance of the diode array from Semtech has a very low capacitance (<15pF). Since the driving capacity of the transmitter can not handle a large load, this diode array is very suitable. The combination of the transformers and a built in diode array from Pulse was chosen because they have made a diode array obtaining low capacitance.

## 5.4 Jumper Configuration

Jumpers are used at the system bus connector to manually configure external payload loopback of the Evaluator Board.

## 5.5 Power Estimates

**Table 7: Power Estimates**

| | Power (Watts) | Current (mA) |
|---|---|---|
| **+2.5V** | | |
| COMET-QUAD | 0.300 | 120 |
| **+3.3V** | | |
| COMET-QUAD | 1.7 | 500 |
| 2.5V Regulator | 1.5 | 160 |
| **+5V** | | |
| PLX 9050 | 0.650 | 130 |
| MAX 701 | 0.005 | 1 |
| 74HC08 | 0.005 | 1 |
| NM93CS46 (EEPROM) | 0.005 | 1 |
| Misc | 1 | 200 |

| | | |
|---|---|---|
| **TOTAL** | **1.665** | **333** |

## 5.6 Voltage Regulators - Current and Thermal Calculations

Power Dissipation in the Regulators:

For 2.5V Regulator:

Using worst case,

$V_{in}$ = 3.3 + 5% = 3.465V

$V_{out}$ = 2.5 – 2% = 2.45V

$I_{out}$ = 160mA x 100% (for safety) = 320mA

Therefore, the dissipated power at the junction is,

$P_j = (V_{in} – V_{out}) (I_{out}) + (V_{in}) (I_{gnd})$

= (3.465 – 2.45) (320) + (3.465) (2)

= 0.3248 + 0.0069

= 0.332 W

Assumptions:

- maximum junction temperature = 125°C
- ambient temperature (no airflow) = 70°C

Therefore,

$T_{jmax} – T_{ja} = P_d \times \phi$

$125 – 70 = 0.332 \times \phi$

$\phi$ = 166 °C/W

for a 500 $mm^2$ of copper, $\phi \cong 60$ °C/W

$P_d \times \phi = 0.332 \times 60 = 19.9$°C

$T_{jmax} = T_{ja} + (P_d \times \phi)$

$= 70 + 20$

$= 90°C$

Therefore, a 500 $mm^2$ area of copper is sufficient to dissipate the heat.

In the 3.3V Regulator:

Using worst case,

Vin = 5 + 10% = 5.5V

Vout = 3.3 – 5% = 3.135V

Iout = 460mA x 100% (for safety) = 920mA

Therefore, the dissipated power at the junction is,

$P_j = (V_{in} – V_{out}) (I_{out}) + (V_{in}) (I_{gnd})$

$= (5.5 – 3.135) (920mA) + (5.5) (2509mA)$

$= 2.176 + 1.375$

$= 3.6$ W

Assumptions:

- maximum junction temperature = 125°C
- ambient temperature (no airflow) = 70°C

Therefore,

$T_{jmax} – T_{ja} = P_d \times \phi$

$125 – 70 = 3.6 \times \phi$

$\phi = 15.28$ °C/W

for a 5000 $mm^2$ of copper, $\phi \cong 15$ °C/W

$P_d \times \phi = 3.7 \times 15 = 55°C$

$T_{jmax} = T_{ja} + (P_d \times \phi)$

= 70 + 55

= 125°C

Therefore, a 5000 $mm^2$ area of copper is sufficient to dissipate the heat.

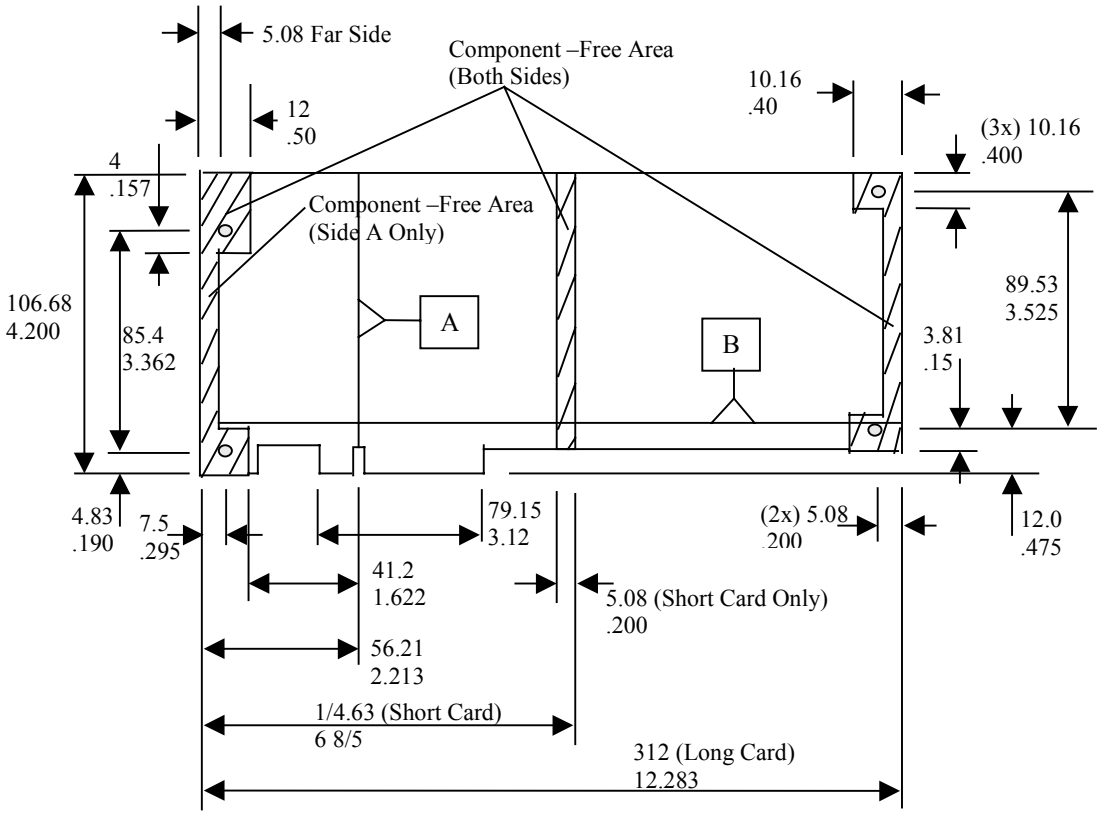
Therefore, the total copper needed is 5000 $mm^2$ + 500 $mm^2$ = 5500 $mm^2$. Note that the area of copper on the ground and power planes is more than the required amount.

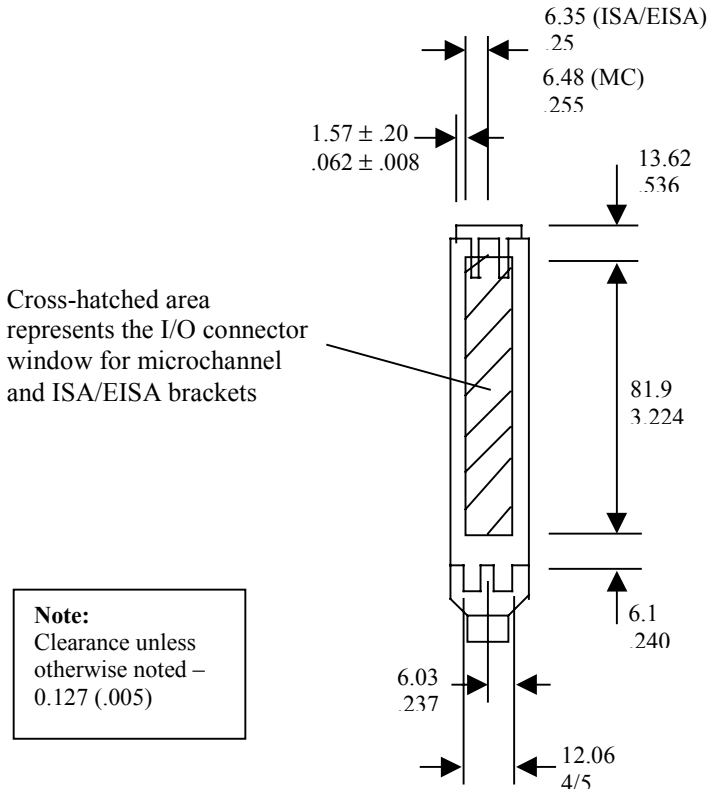
# 6 PHYSICAL AND MECHANICAL DESCRIPTIONS

## 6.1 Form Factor

The following figures show the mechanical outline and dimensions of the COMET-QUAD Evaluator Board design.

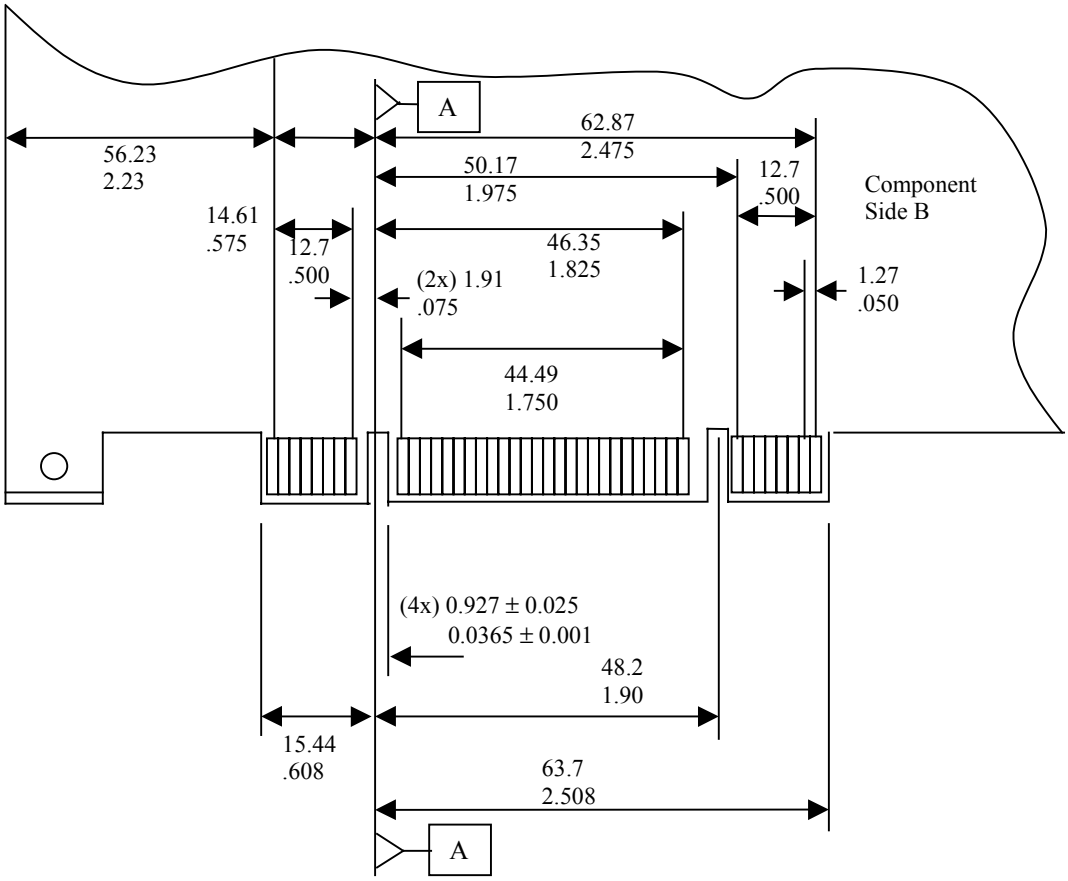
**Figure 8: PCI Universal 32-bit Card Mechanical Outline**






**Note:**
Clearance unless otherwise noted – 0.127 (.005)

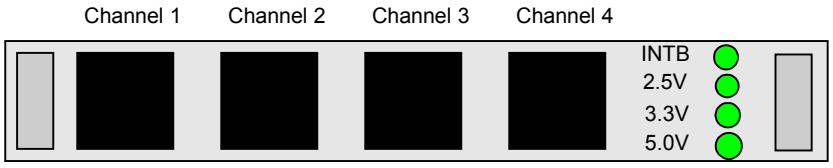
**Figure 9: PCI Universal 32-bit Card Edge Connector Dimensions and Tolerances**




## 6.1.1 Face Plate

The following figure shows the proposed faceplate for the COMET-QUAD Evaluator Board design.

**Figure 10 - Face Plate**



## 6.2 Connectors

### 6.2.1 Line Interface Connectors

Only one set of line interface connectors is provided with the evaluator board. These are the RJ48C connectors. Shielded jacks are used to help reduce EMI radiation and increase EMI tolerance.

### 6.2.2 System Bus Connector

The System Bus Connector allows access to configure the COMET-QUAD and control the external payload loopback.

### 6.2.3 PCI Edge Connector

The PCI Edge Connector is a standard Universal, 32 bit PCI connector.

## 6.3 LEDs

### 6.3.1 COMET-QUAD Interrupt LED

A PCB mounted LED is connected to the INTB pin to allow for visual indication of interrupts being generated by the COMET-QUAD.

- INTB, green – indicates presence of interrupts

### 6.3.2 Power Status LEDs

Three LEDs are provided to display the status of power to the COMET-QUAD board, one for 5.0V, one for 3.3V, and one for 2.5V.

- +5V, green – indicates presence of +5V
- +3.3V, green – indicates presence of +3.3V
- +2.5V; green – indicates presence of +2.5V

# 7 SOFTWARE INTERFACES

## 7.1 Memory Map

**Table 8: System Memory Map**

| PCI9050 Local Address Space | Address | Device | R/W | Description |
|---|---|---|---|---|
| CS_0 | 0000-00FF | PM4354 COMET-QUAD | R/W | COMET-QUAD Registers |

## 7.2 PCI 9050 Configuration

The following sets of tables specify the values that should be programmed into the SEEP. These values will be loaded into the PCI9050 registers on power-up. Please refer to the PCI9050 datasheet [5] for further details.

NOTE: The checksum of the SEEP is 0x230D.

**Table 9: PCI Local Address Space Register**

| Register | Address | Description | Value |
|---|---|---|---|
| PCIIDR | 0x000 | Device_ID/Vendor_ID | 0x905010B5 |
| PCIREV | 0x004 | Class_Code | 0x06800000 |
| PCISVID | 0x008 | Subsystem_ID/Subsystem_Vendor_ID | 0x000311F8 |
| PCIILAR | 0x00C | Maximum Latency MinimumGrant IntPin Routing | 0x00000000 |

**Table 10: PCI Local Address Space**

| Register | Address | Description | Value |
|---|---|---|---|
| LAS0RR | 0x010 | Local_Address_Space_0_Range | 0x0FFFFC00 |
| LAS1RR | 0x014 | Local_Address_Space_1_Range | 0x00000000 |
| LAS2RR | 0x018 | Local_Address_Space_2_Range | 0x00000000 |
| LAS3RR | 0x01C | Local_Address_Space_3_ | 0x00000000 |
| EROMRR | 0x020 | Expansion_ROM_Range | 0x00000000 |

**Table 11: PCI Local Address Space Re-Map**

| Register | Address | Description | Value |
|---|---|---|---|
| LAS0BA | 0x024 | LocalAddressSpace_0_Base_Address(Re-Map) | 0x00000001 |
| LAS1BA | 0x028 | LocalAddressSpace_1_Base_Address(Re-Map) | 0x00000000 |
| LAS2BA | 0x02C | LocalAddressSpace_2_Base_Address(Re-Map) | 0x00000000 |
| LAS3BA | 0x030 | LocalAddressSpace_3_Base_Address(Re-Map) | 0x00000000 |
| EROMBA | 0x034 | Expansion_ROM_Base_Address(Re-Map) | 0x00000000 |

**Table 12: PCI Local Address Space Region Descriptors**

| Register | Address | Description | Value |
|---|---|---|---|
| LAS0BRD | 0x038 | LocalAddressSpace0_Bus_Region_Descriptors | 0x1681A1A0 |
| LAS1BRD | 0x03C | LocalAddressSpace1_Bus_Region_Descriptors | 0x00000000 |
| LAS2BRD | 0x040 | LocalAddressSpace2-Bus_Region_Descriptors | 0x00000000 |
| LAS3BRD | 0x044 | LocalAddressSpace3_Bus_Region-Descriptors | 0x00000000 |
| EROMBRD | 0x048 | Expansion_ROM_Bus_Region_Descriptors | 0x00000000 |

**Table 13: PCI Chip Select Base**

| Register | Address | Description | Value |
|---|---|---|---|
| CS0BASE | 0x04C | Chip_Select_0_Base | 0x00010001 |
| CS1BASE | 0x050 | Chip_Select_1_Base | 0x00000000 |
| CS2BASE | 0x054 | Chip_Select_2_Base | 0x00000000 |
| CS3BASE | 0x058 | Chip_Select_3_Base | 0x00000000 |

**Table 14: PCI Local Address Space Registers**

| Register | Address | Description | Value |
|---|---|---|---|
| INTCSR | 0x05C | Interrupt_Control/Status | 0x00000041 |
| CNTRL | 0x060 | User_I/O\| EEPROM\|Init_Control | 0x00024492 |
| NULL | 0x064 | Null_data | 0xFFFFFFFF |
| NULL | 0x068 | Null_data | 0xFFFFFFFF |
| NULL | 0x06C | Null_data | 0xFFFFFFFF |
| NULL | 0x070 | Null_data | 0xFFFFFFFF |
| NULL | 0x074 | Null_data | 0xFFFFFFFF |
| NULL | 0x078 | Null_data | 0xFFFFFFFF |
| NULL | 0x07C | Null_data | 0xFFFFFFFF |

# 8 CONFORMANCE SPECIFICATION

The Evaluator Board utilizes PCI 9050-1, which is compliant with PCI Local Bus Specification 2.1 [6], supporting low cost slave adapters. The chip allows simple conversion of ISA adapters to PCI.

The design of the Evaluator Board, including the external protection circuitry, are designed to meet the major surge immunity and electrical safety standards including FCC Part 68, UL1459 and 1950, and Bellcore TR-NWT-001089. Note that this board has not been tested yet.

# 9 LAYOUT DESCRIPTION

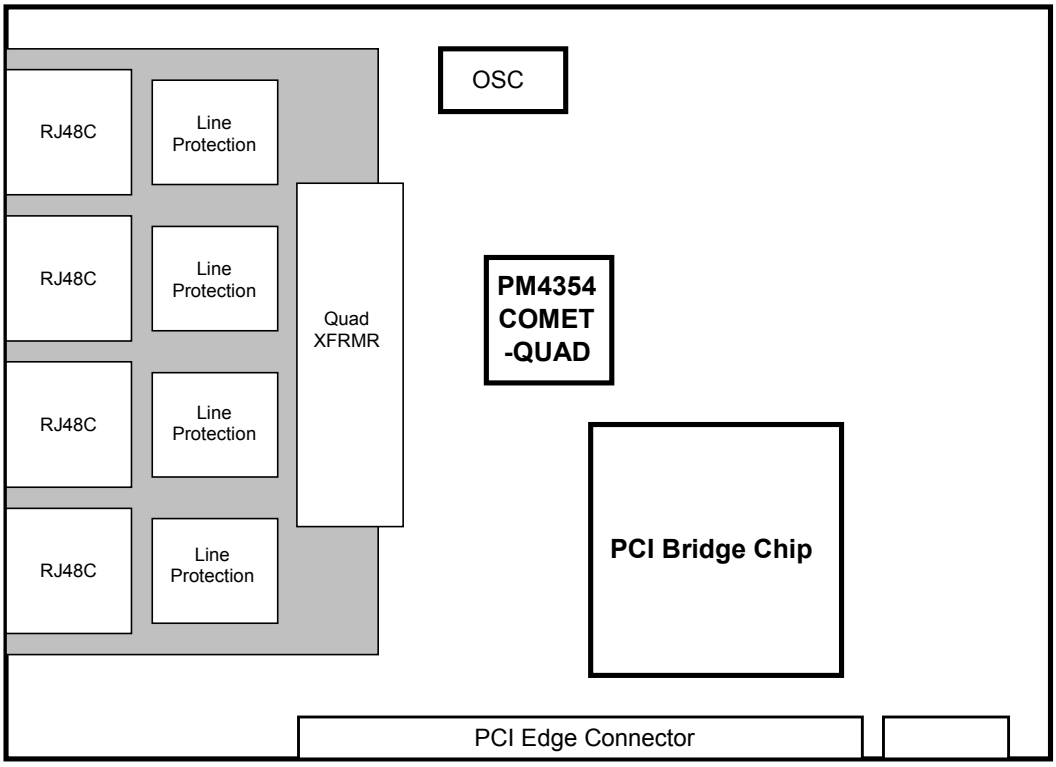
## 9.1 Component Placement

The overall placement strategies of the components are:

- Place the analog circuitry away from the digital circuitry.
- Keep analog transmit side components separate from the analog receive side components.
- The PCI Bridge device is placed such that all the PCI interface traces are within the specified length limits of the PCI Rev. 2.1 Specification.
- The oscillator is placed in a quiet digital section as noise on its power supply will cause jitter on the output, and the oscillator itself generates noise that may affect sensitive analog circuits.
- All source termination resistors are placed near the outputs and load termination resistors are placed near the inputs.
- All pull up/down resistors are placed near the output pins.
- All decoupling capacitors are placed near the power supply pins.

The overall placement is as follows:

**Figure 12: Main Component Placement Diagram**




## 9.2 Layer Stacking and Transmission Line Impedance Control

The COMET-QUAD Evaluator card has six layers: (from the top down) layer 1 is the top layer for signals, layer 2 for ground, layer 3 for Vcc signals, layer 4 for the 2.5V power plane, layer 5 for the 3.3V power plane and layer 6 is the bottom layer for signals. The dimension of the card conforms to the 5V PCI Raw Short Card, with custom mounting hole locations. The layer configurations are shown below:

**Figure 13: Layer Stack**

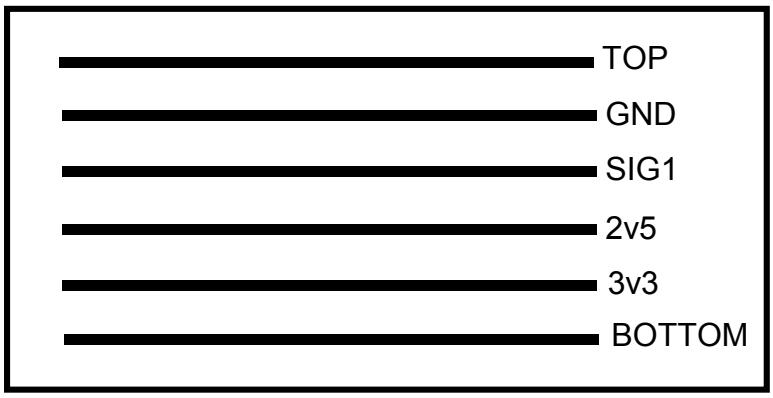
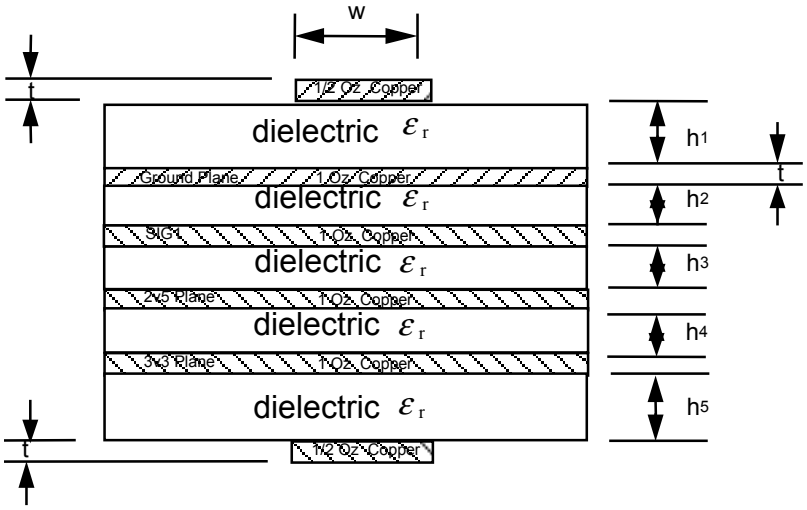



**Figure 14: PCB Cross Section**




where

$\varepsilon_t$ = relative dielectric constant, nominally 5.0 for G –10 fibre –glass epoxy

t = thickness of the copper, fixed according to the weight of copper selected. For 1 oz copper, the thickness is 1.44 mil. For ½ oz copper, the thickness is 0.72 mil. This thickness can be ignored if w is large enough.

h1, h2, h3, h4, h5 = thickness of dielectric.

w = width of copper

The PCB related parameters are shown in Table 15:

**Table 15: PCB parameters**

| Parameters | Nominal |
|---|---|
| Board Thickness (mil) | 62 (including copper thickness) |
| dielectric thickness between layers 1 and 2 (mil) (h1) | 7 |
| dielectric thickness between layers 2 and 3 (mil) (h2) | 8 |
| dielectric thickness between layers 3 and 4 (mil) (h3) | 24 |
| dielectric thickness between layers 4 and 5 (mil) (h4) | 8 |
| dielectric thickness between layers 5 and 6 (mil) (h5) | 7 |
| Relative dielectric constant | 4.2 |

To reduce signal degradation due to reflection and radiation, the traces that carry high speed signals should be treated as micro strip transmission lines with controlled impedance and matched resistive termination. The trace impedance is calculated using the formula:

$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \times \ln\left(\frac{5.98 \times h}{0.8 \times w + t}\right)$$

| Parameter | Data |
|---|---|
| $\varepsilon_r$ | 4.2 |
| h1 (mil) | 7 |
| t (mil) (2 Oz copper) | 2.88 |
| Zo (Ohm) | 50 |
| W (mil) | 10 |

Given characteristic impedance Zo, the dielectric thickness h1 is proportional to trace width. A small h1 will result in the traces being too thin to be accurately fabricated. Wider traces can be more precisely manufactured, but they take up too much board space. Therefore, the thickness of the board for a given trace impedance and adequate trace width should be chosen so that the traces take up as little board space as possible yet still leaving enough margin to allow accurate fabrication.

Using the same h1, thickness of copper, and dielectric constant, a 10 mil traces has a characteristic impedance of approximately 50 Ohms while an 3 mil trace has a characteristic impedance of 75 Ohms. We are using controlled impedance of 75 Ohms on this Evaluator Board.

## 9.3 Power and Ground

The following diagrams illustrates the power and ground plane distribution:

**Figure 15: GND Plane**

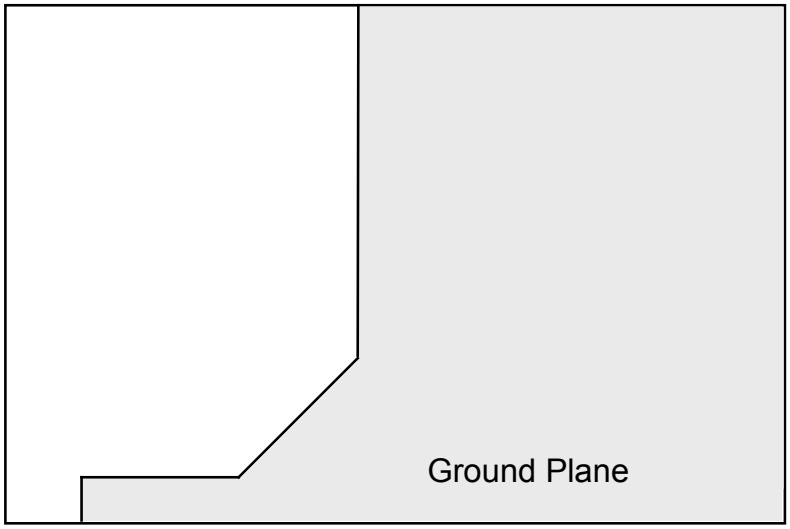



**Figure 16: VCC Plane**

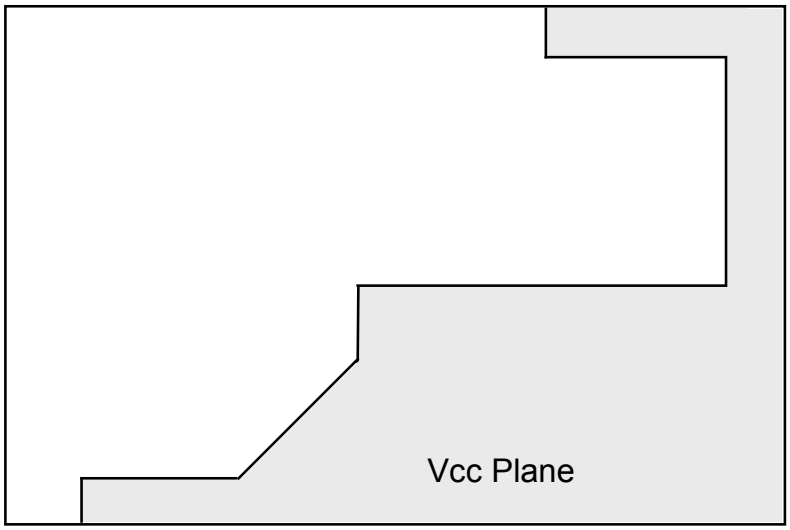


**Figure 17: 2.5V Plane**

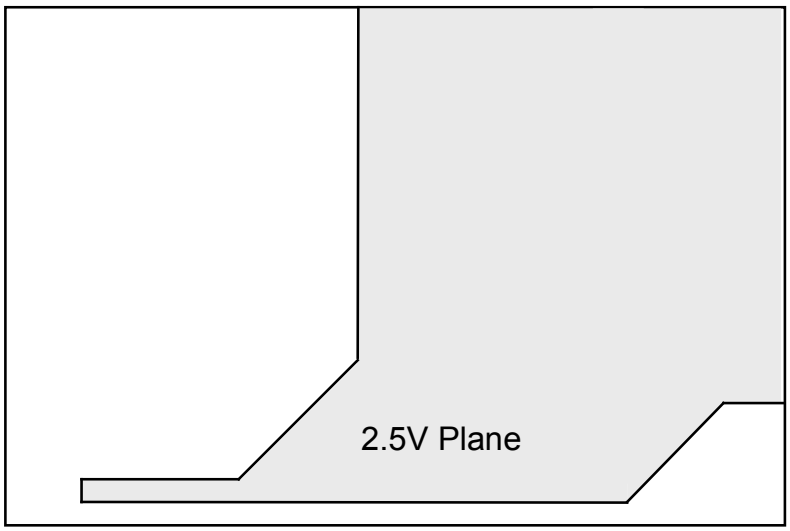
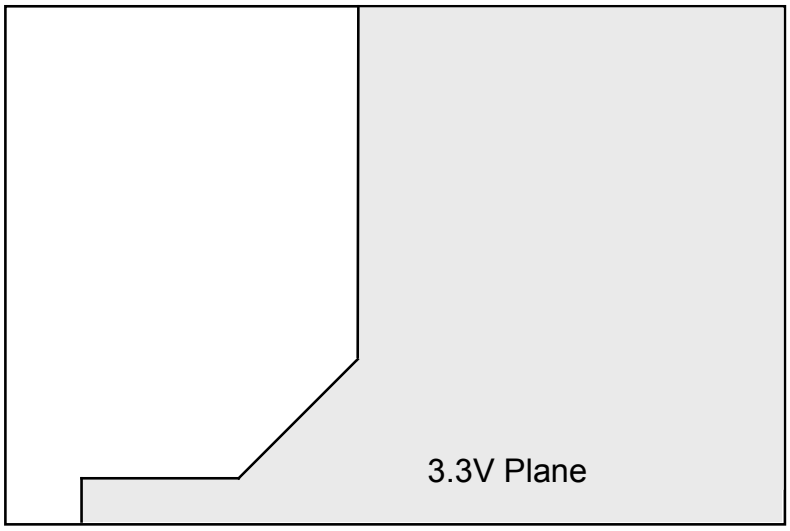



**Figure 18: 3.3V Plane**




The introduction of ground slots within the ground plane must be avoided as they will increase trace inductance and increase crosstalk. Making clear-out holes too large can accidentally create these slots.

## 9.4 PCI Bus Signal Specification

This layout follows the PCI Rev. 2.1 Specification layout restrictions. The PCI SIG specification has stringent and detailed rules on decoupling, power consumption, trace length limits, routing, trace impedance, as well as signal

loading. Therefore, it is essential to check the latest PCI specification before proceeding with new designs and layouts.

The COMET-QUAD Evaluator design board conforms to the following PCI Specification/Recommendations:

- Component height on the component side does not exceed 0.570 inches, and on the solder side does not exceed 0.105 inches.
- PCI CLK signal trace is 2.5 inches +/- 0.1 inches and is connected to only one load.
- All 32-bit interface signals have the maximum trace length of 1.5 inches.
- Trace impedance for shared PCI signals are within 60 - 100 Ohm range, and trace velocity is between 150 and 190 ps/inch.
- 20 mil wide traces are used to connect the power and ground pins on PCI connector to their respective planes and the trace lengths are limited to 250 mil.

## 9.5 Routing

- All power and ground traces are as wide and short as possible to minimize trace inductance.
- All high speed traces are routed over continuous image planes (power or ground planes).
- All traces carrying transmit and receive line rate data should be routed on the same side and kept as short as possible.
- Both signals of a differential pair are of equal length and routed close to each other.

# 10 GLOSSARY

| | |
|---|---|
| CompactPCI | Compact Peripheral Component Interconnect. A bus standard based on the PCI standard that defines a more rugged mechanical form factor for industrial use. |
| CSU | Channel Service Unit. |
| DS1 | Off-premise T1 interface level provided by CSU. |
| DSX-1 | Digital Cross-connect T1 interface level. |
| E1 | European First Order transmission format. This is the standardized (ITU-T G.704) base format of the European Pleisosynchronous Digital Hierarchy. It operates at 2.048Mbps. The E1 format consists of frames consisting of 32 octets, or timeslots (numbered 0 to 31). Timeslot 0 alternates between containing an FAS and containing the National Use bits (Sa[8:4]) and an A-bit for RAI. Timeslot 0 also contains an International Use Bit (Si) which can be used to support CRC Multiframe. |
| HDLC | High Level Data Link Control. A family of bit-oriented protocols providing frames of information with address, control and frame check sequence fields. |
| H-MVIP | High Capacity MVIP |
| MVIP | Multi-Vendor Integration Protocol. A TDM bus standard that is an extension of Mitel's ST-BUS. The MVIP bus is used in computer telephony integration applications. |
| PCI | Peripheral Component Interconnect – A bus standard that defines 32 bit transfers over a defined electrical interface. |
| PCI Host | An adapter board for a PCI system which acts as a PCI Master and performs the additional functions of clock distribution and bus arbitration. |
| PCI Target | An adapter board for a PCI system which does not initiate bus transactions. Also known as a slave. |
| ESF | Extended Super Frame format. |

| | |
|---|---|
| RJ-48C | An 8 pin RJ-45 modular connector with a standardized pinout used for 100 ohm T1 and 120 ohm E1 interfaces. |
| SEEP | Serial EEPROM (Electrically Erasable Programmable Read Only Memory) – A type of non-volatile memory which is programmed and read using a serial interface. |
| T1 | A level 1 digital trunk operating at 1.544 Mbit/s that is popular in North America and Japan. It is made up of 193 bits, grouped as 1 framing bit followed by 24 DS-0 channels of 8 bits each. |
| T1.403 | A standard specifying a DS1-rate metallic interface, referred to as the network interface (NI), between the network and a customer installation. |
| TDM | Time Division Multiplexed – A TDM signal consists of several channels of data which are multiplexed together in time so that a byte (or word, etc.) of one channel of data is transferred, following by a byte of the second, etc. |

## 11 REFERENCES

1. PMC-Sierra, Inc., PMC-1990315, ”COMET-QUAD Data Sheet”, Issue 5, December 2000.
2. PMC-Sierra, Inc., PMC-1970624, “Combined E1/T1 Transceiver Standard Product Datasheet”, Issue 9, September 2000.
3. PMC-Sierra, Inc., PMC-1981210, “COMET Reference Design Rev. 2.0”, Issue 1, November 1998.
4. PMC-Sierra, Inc., PMC-1980815, “COMET Evaluation Board Rev. 2.0”, Issue 4, June 2000.
5. PLX Technology, PCI 9050-1 Data Book, Version 1.01, April 17, 1997.
6. PCI Local Bus Specification Revision 2.1s, June 1, 1995.

# 12 DISCLAIMER

This document is a paper reference design, and as such, has not been built or tested as of this date.

Note that the protection circuitry provided in this document has not been tested to date. Therefore, there are no guarantees that it meets FCC Part 68, UL 1459 and 1950, and Bellcore TR-NWT-001089.

Please check the PMC-Sierra website regularly for updates to this document.

# 13 APPENDIX A: BILL OF MATERIALS

**Table 16: Major Components List**

| Ref. No | Component | Manufacturer | Package Type | Quantity |
|---|---|---|---|---|
| S1-S16 | P1800SC SIDACtor | Teccor Electronics 972-580-7777 | DO-214 SMB | 16 |
| S17-S24 | P0720SC SIDACtor | Teccor Electronics 972-580-7777 | DO-214 SMB | 8 |
| U1 | T9021 | Pulse Inc. 619-674-8100 | | 1 |
| F1-F16 | F1250T Telelink Fuse | Teccor Electronics 972-580-7777 | SMD | 16 |
| U7 | LM3940 | National Semiconductor 408-721-5000 | SOT-223 | 1 |
| U4 | NM93CS46EN | Fairchild Semiconductor 1-800-364-3577 | 8-pin DIP | 1 |
| U6 | PCI-9050 | PLX Technology 800-759-3735 | 160 pin PQFP | 1 |

**Table 17: Bill of Materials**

| | Part Name - Value | Part Number | Ref Des | Qty |
|---|---|---|---|---|
| 1 | 74HC08_SOIC-BASE | Fairchild Semiconductor MM74HC08M | U3 | 1 |
| 2 | CAPACITOR-0.01UF, 50V,X7R_603 | Various | C4,C10,C12,C13,C15,C17, C19,C20,C22-C25,C28,C30,C32,C34,C36, C45,C49,C51,C52,C55-C57,C59-C61,C65,C66,C68,C70,C71 | 32 |

| | | | | |
|---|---|---|---|---|
| 3 | CAPACITOR-0.1UF,16V, X7R_603 | Various | C1-C3,C11,C18,C21,C29,C31, C35,C37,C43,C44,C46-C48,C50,C53,C54,C58,C62-C64,C67,C69,C72 | 25 |
| 4 | CAPACITOR-0.47UF, 25V,TANTTHE | Various | C40 | 1 |
| 5 | CAPACITOR-10UF,10V,TANTTHE | Various | C42 | 1 |
| 6 | CAPACITOR-22UF,6.3V,TANTTHE | Various | C9,C26,C27 | 3 |
| 7 | CAPACITOR-4.7UF,10V,TANTTHE | Various | C5-C8 | 4 |
| 8 | CAPACITOR-47UF,6.3V,TANTTHE | Various | C14,C16,C33,C38,C39 | 5 |
| 9 | CAPACITOR-68UF,6.3V,TANTTHE | Various | C41 | 1 |
| 10 | COMET-QUAD_PBGA-BASE | PMC PM4354-PI | U5 | 1 |
| 11 | FUSE SMD – 500A @ 2X10mailto:FUSE_SMD-500A@2X10 | Teccor Electronics – F1250T | F1-F16 | 16 |
| 12 | FUSE__SMD_SOCKET-1.000A,SLO-BLO | DIGI-KEY -- F1303CT-ND | F17 | 1 |
| 13 | HEADER4_100MIL-BASE | Sullins Electronics – PZC36SAAN | J7 | 1 |
| 14 | HEADER_4X2_SMT_2MM-BASE | 87267-0850 | J8-J13 | 6 |
| 15 | LM3940_SOT-BASE | LM3940IMP-3.3 | U7 | 1 |

| | | | | |
|---|---|---|---|---|
| 16 | MAX701_SOIC-BASE | MAXIM MAX701ESA | U2 | 1 |
| 17 | MIC39150_T0220-2.5V | MICREL – MIC39150-2.5BT | U8 | 1 |
| 18 | MMBT3906_SOT23-BASE | MMBT3906LT1 | Q1 | 1 |
| 19 | NM93CS46_DIP8_SOCKET-BASE | Fairchild Semiconductor NM93CS46 | U4 | 1 |
| 20 | OSC_TTL_DIP-2.048MHZ,50 PPM,CHA | Champion K1150BA-2.048MHz MMD MA050T-2.048MHz | Y1 | 1 |
| 21 | P0720SC_SMB-BASE SIDACtor | Teccor Electronics P0720SC | S17-S24 | 8 |
| 22 | P1800SC_SMB-BASE SIDACtor | Teccor Electronics P1800SC | S1-S16 | 16 |
| 23 | PBSWITCH-BASE Pushbutton switch | PBSWITCH DIGI-KEY P8007S-ND | SW1 | 1 |
| 24 | PCI9050_PQFP-BASE | PCI9050-1 | U6 | 1 |
| 25 | PCI_UNIV_32_CARD_CON N-PCI_UNIVA | EDGE CONNECTOR | P1 | 1 |
| 26 | RESISTOR-0,5%,603 | Various | R23,R44,R48,R50 | 4 |
| 27 | RESISTOR-1,5%,603 | Various | R26-R29,R33,R36-R38,R42,R43,R45,R47 | 12 |
| 28 | RESISTOR-100,5%,603 | Various | R3 | 1 |
| 29 | RESISTOR-100K,5%,603 | Various | R30-R32,R46 | 4 |
| 30 | RESISTOR-10K,1%,603 | Various | R6 | 1 |
| 31 | RESISTOR-10M,5%,1206 | Various | R5 | 1 |

| | | | | |
|---|---|---|---|---|
| 32 | RESISTOR-12.7,1%,603 | Various | R15-R22 | 8 |
| 33 | RESISTOR-150,5%,603 | Various | R2 | 1 |
| 34 | RESISTOR-18.2,1%,603 | Various | R11-R14 | 4 |
| 35 | RESISTOR-330,5%,603 | Various | R1,R4,R51 | 3 |
| 36 | RESISTOR-4.7,5%,603 | Various | R25,R34,R35 | 3 |
| 37 | RESISTOR-4.7K,5%,603 | Various | R7-R10,R24,R41,R49 | 7 |
| 38 | RESISTOR-56,5%,603 | Various | R39,R40 | 2 |
| 39 | RES_ARRAY_4_SMD-4.7K | DIGI-KEY -- Y44.7KCT-ND Panasonic EXB-V8V4K7JV | RN1-RN13 | 13 |
| 40 | RJ45_SHIELD_UNIVERSAL | STEWART or AMP | J1-J4 | 4 |
| 41 | SSF_LXH5147-LGD | LUMEX – SSF-LXH5147LGD | D1 | 1 |
| 42 | TRANSFORMER & DIODE ARRAY T9021_-BASE | PULSE – T9021 | U1 | 1 |
| 43 | TEST_POINT_2_PAD60CI R36D-BASE | | TP9,TP10 | 2 |
| 44 | TST_PT-BASE | DIGIKEY – S1011-36-ND | TP3-TP8 | 6 |
| 45 | TST_PT_BIG-GROUNDED MOUNTING HA | | TP1,TP2 | 2 |

# 14 APPENDIX B: SCHEMATICS

The COMET-QUAD Evaluator Board schematics were captured using Cadence software Concept Schematics Capture tool.

## 14.1 ROOT DRAWING, Sheet 1

This sheet provides an overview of the major functional blocks of the COMET-QUAD Evaluator board. It shows interconnections between the COMET-QUAD_BLOCK, PCI_INTERFACE_BLOCK, LINE_INTERFACE and POWER blocks.

## 14.2 COMET-QUAD BLOCK, Sheet 2

This sheet shows the COMET-QUAD device and its power circuitry. The power circuitry includes a Schottky diode for powering up the COMET-QUAD device and separate filtering circuitry for the analog and digital power pins. A LED is connected to the INTB pin to allow for visual indication of interrupts being generated by the COMET-QUAD.

## 14.3 LINE INTERFACE, Sheet 3 and 4

This sheet shows the termination, magnetics and protection circuitry for the 4 line interfaces. A single diode array and transformers quad module from Pulse is used to couple all of the 4 sets transmit and receive lines of the COMET-QUAD to the connectors. The P1800SC SIDACtor, P0720SC SIDACtor and the F1250T Telelink Fuse provide over voltage and over-current protection. Connections to RJ48C connectors are provided.

## 14.4 PCI INTERFACE, Sheet 5

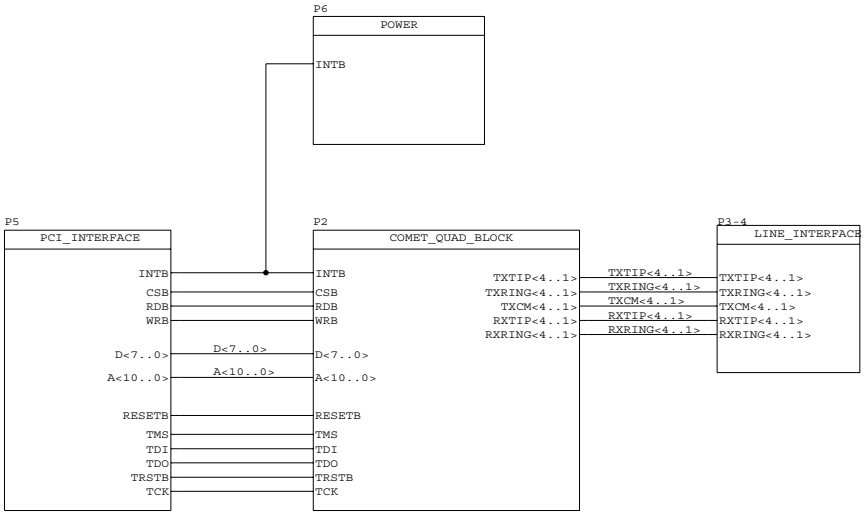
This sheet shows the PCI connector and the PCI bridge chip. The PLX PCI-9050 PCI bridge chip is compliant to PCI Specification 2.1.

## 14.5 POWER, Sheet 6

The LM3940 drop-out voltage regulator supplies 3.3V to the COMET-QUAD device. Three LED's are provided to display the status of power to the COMET-QUAD board, one for 5.0V, one for 3.3V, and one for 2.5V.

NOTE: VCC = +5.0V

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV | DESCRIPTION | DATE | APPR |

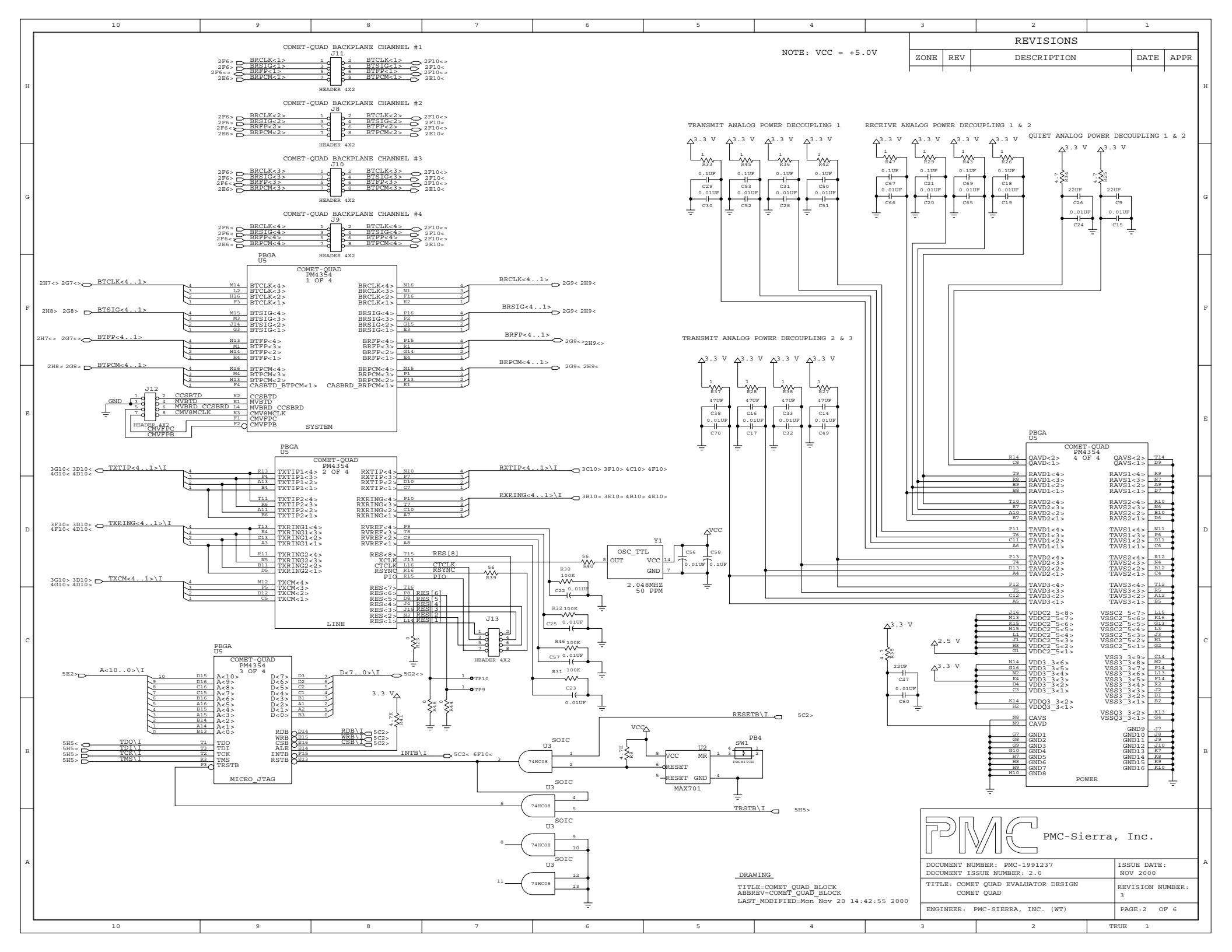



DRAWING

TITLE=COMET_QUAD_KIT_ROOT
ABBREV=COMET_QUAD_KIT_ROOT
LAST_MODIFIED=Wed Nov 15 14:00:44 2000

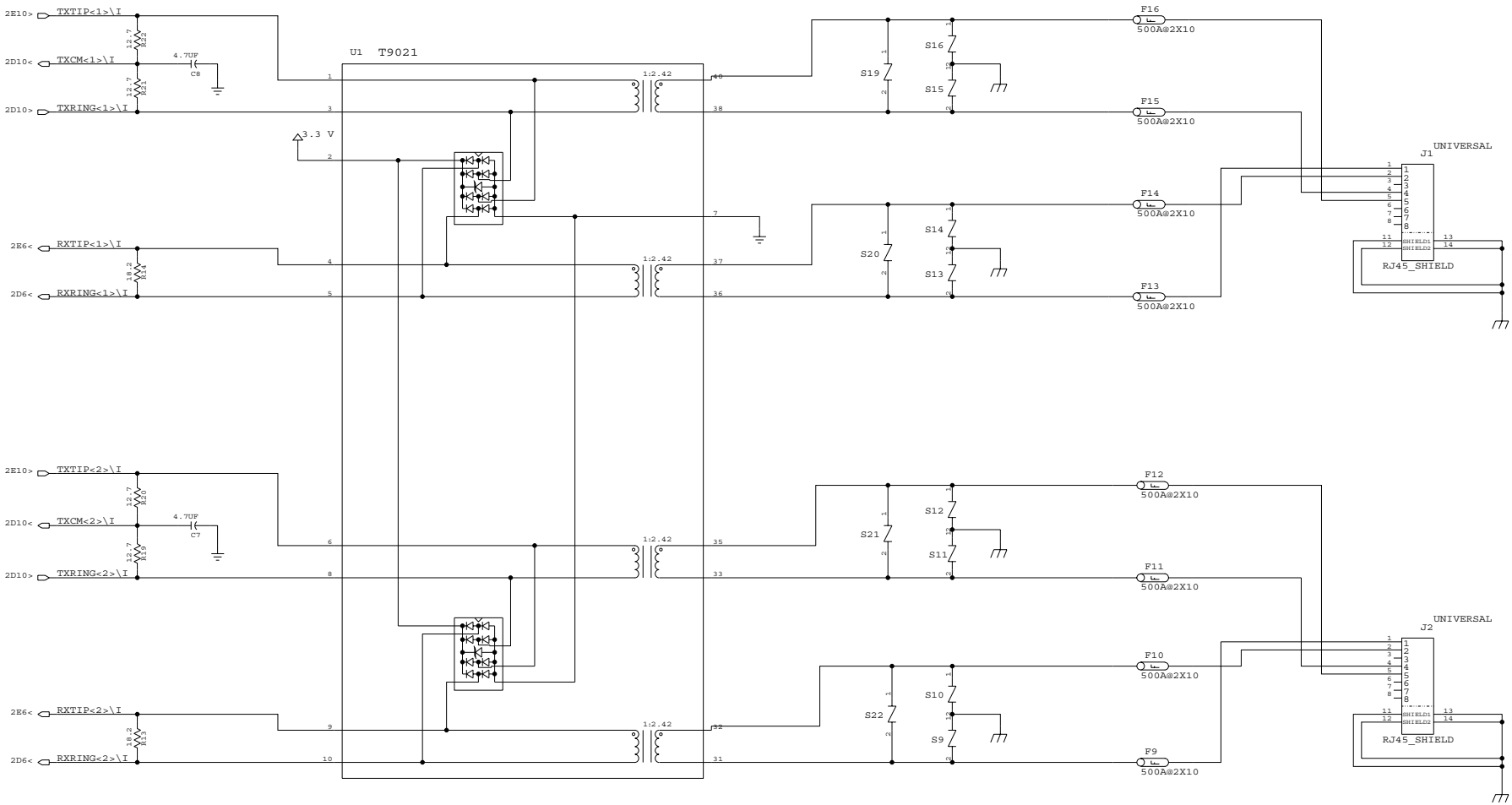
PMC-Sierra, Inc.

| | |
|---|---|
| DOCUMENT NUMBER: PMC-1991237<br>DOCUMENT ISSUE NUMBER: 2.0 | ISSUE DATE:<br>NOV 2000 |
| TITLE: COMET QUAD EVALUATOR DESIGN<br>ROOT DRAWING | REVISION NUMBER:<br>3 |
| ENGINEER: PMC-SIERRA, INC. (WT) | PAGE:1 OF 6 |


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPR
NOTE: VCC = +5.0V
COMET-QUAD BACKPLANE CHANNEL #1
COMET-QUAD BACKPLANE CHANNEL #2
COMET-QUAD BACKPLANE CHANNEL #3
COMET-QUAD BACKPLANE CHANNEL #4
HEADER 4X2
TRANSMIT ANALOG POWER DECOUPLING 1
RECEIVE ANALOG POWER DECOUPLING 1 & 2
QUIET ANALOG POWER DECOUPLING 1 & 2
TRANSMIT ANALOG POWER DECOUPLING 2 & 3
COMET-QUAD PM4354 1 OF 4
COMET-QUAD PM4354 2 OF 4
COMET-QUAD PM4354 3 OF 4
COMET-QUAD PM4354 4 OF 4
SYSTEM
LINE
MICRO_JTAG
POWER
OSC_TTL
2.048MHZ 50 PPM
MAX701
74HC08
SOIC
DRAWING
TITLE=COMET_QUAD_BLOCK
ABBREV=COMET_QUAD_BLOCK
LAST_MODIFIED=Mon Nov 20 14:42:55 2000
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-1991237
DOCUMENT ISSUE NUMBER: 2.0
ISSUE DATE: NOV 2000
TITLE: COMET QUAD EVALUATOR DESIGN
COMET QUAD
REVISION NUMBER: 3
ENGINEER: PMC-SIERRA, INC. (WT)
PAGE:2 OF 6

NOTE: VCC = +5.0V

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV | DESCRIPTION | DATE | APPR |
| | | | | |




DRAWING

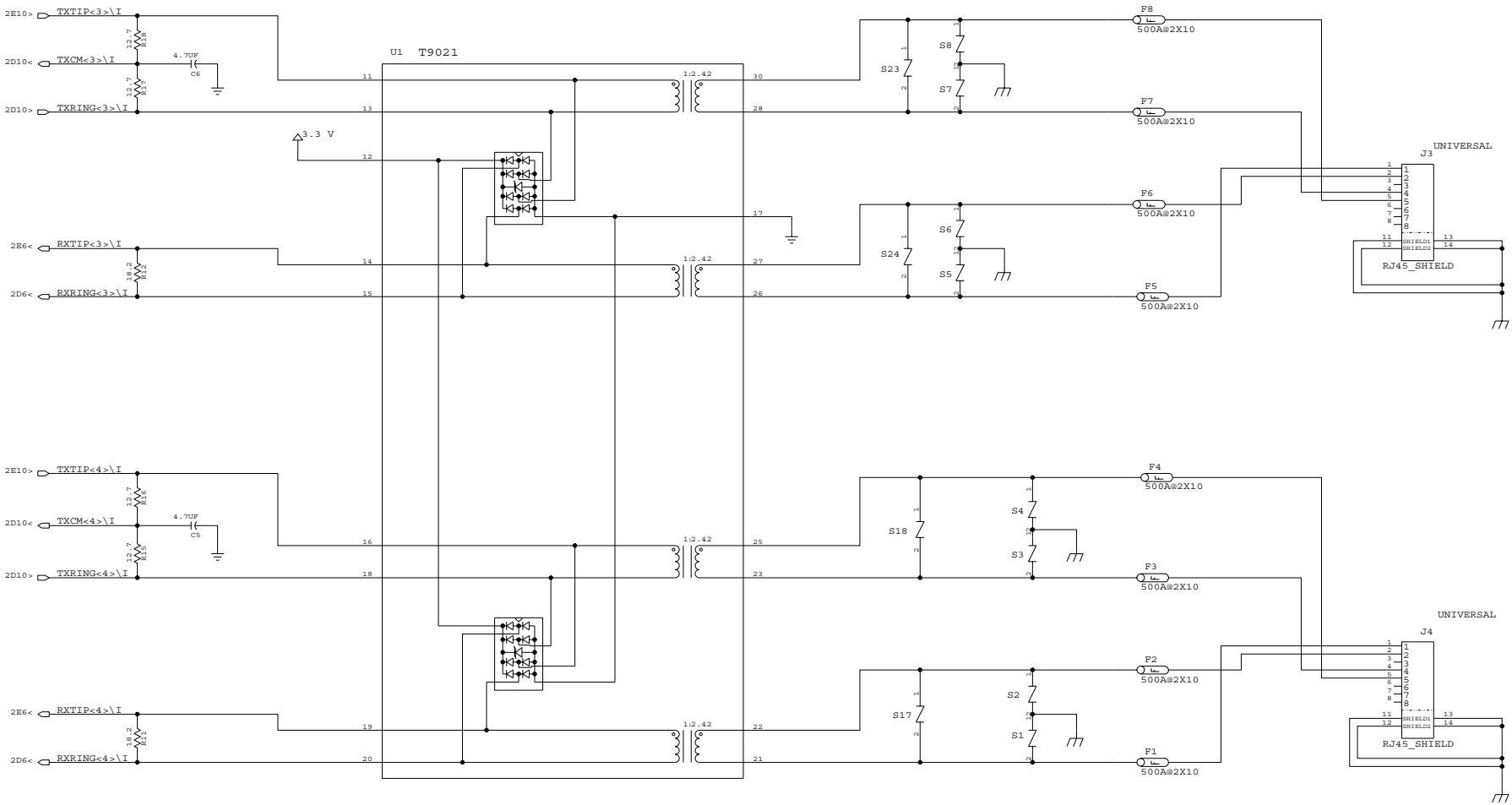
TITLE=LINE_INTERFACE
ABBREV=LINE_INTERFACE
LAST_MODIFIED=Mon Nov 20 14:42:39 2000

PMC-Sierra, Inc.

| | |
|---|---|
| DOCUMENT NUMBER: PMC-1991237<br>DOCUMENT ISSUE NUMBER: 2.0 | ISSUE DATE:<br>NOV 2000 |
| TITLE: COMET QUAD EVALUATOR DESIGN<br>LINE INTERFACE 1/2 | REVISION NUMBER:<br>3 |
| ENGINEER: PMC-SIERRA, INC. (WT) | PAGE:3 OF 6 |

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV | DESCRIPTION | DATE | APPR |

NOTE: VCC = +5.0V




DRAWING

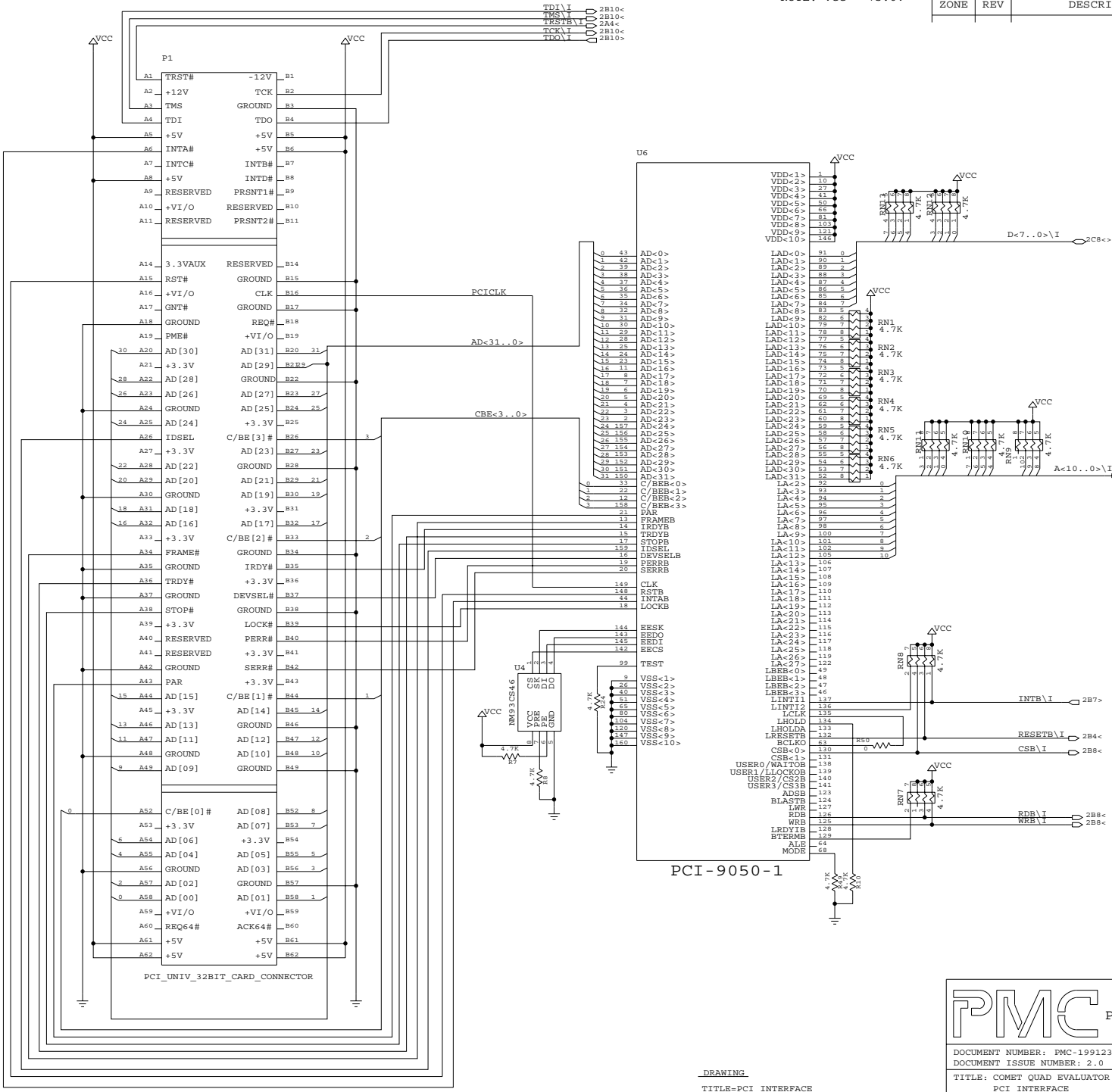
TITLE=LINE_INTERFACE
ABBREV=LINE_INTERFACE
LAST_MODIFIED=Mon Nov 20 14:42:41 2000

PMC-Sierra, Inc.

| | |
|---|---|
| DOCUMENT NUMBER: PMC-1991237<br>DOCUMENT ISSUE NUMBER: 2.0 | ISSUE DATE:<br>NOV 2000 |
| TITLE: COMET QUAD EVALUATOR DESIGN<br>LINE INTERFACE 2/2 | REVISION NUMBER:<br>3 |
| ENGINEER: PMC-SIERRA, INC. (WT) | PAGE:4 OF 6 |

NOTE: VCC = +5.0V

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV | DESCRIPTION | DATE | APPR |
| | | | | |




DRAWING

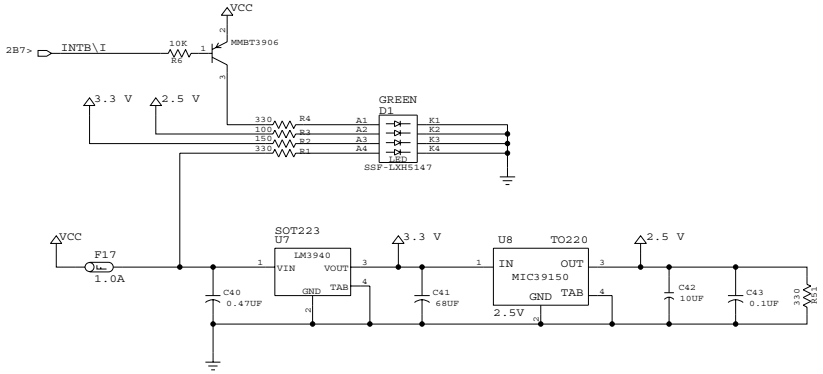
TITLE=PCI_INTERFACE
ABBREV=PCI_INTERFACE
LAST_MODIFIED=Mon Nov 20 14:42:49 2000

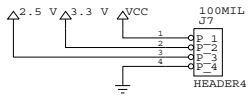
PMC-Sierra, Inc.

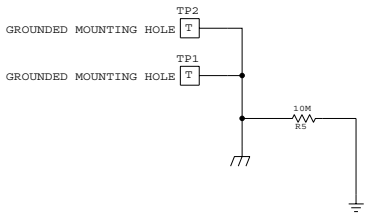
| | |
|---|---|
| DOCUMENT NUMBER: PMC-1991237<br>DOCUMENT ISSUE NUMBER: 2.0 | ISSUE DATE:<br>NOV 2000 |
| TITLE: COMET QUAD EVALUATOR DESIGN<br>PCI INTERFACE | REVISION NUMBER:<br>3 |
| ENGINEER: PMC-SIERRA, INC. (WT) | PAGE:5 OF 6 |

NOTE: VCC = +5.0V

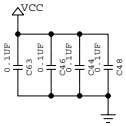
| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV | DESCRIPTION | DATE | APPR |
| | | | | |



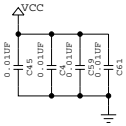








PLACE ONE CAP ON EACH SIDE OF THE PCI9050 DEVICE

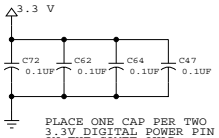



PLACE ONE CAP ON EACH SIDE OF THE PCI9050 DEVICE

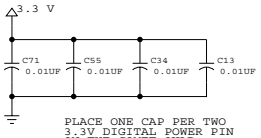
PLACE ONE CAP FOR MAX701 DEVICE


PLACE ONE CAP FOR HC08 DEVICE

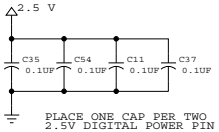

PLACE ONE CAP FOR NM93CS46 DEVICE

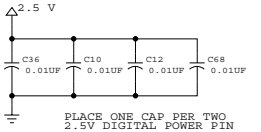

PLACE ONE CAP PER TWO 3.3V DIGITAL POWER PIN ON THE COMET QUAD



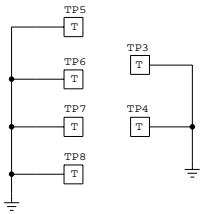

PLACE ONE CAP PER TWO 3.3V DIGITAL POWER PIN ON THE COMET QUAD




PLACE ONE CAP PER TWO 2.5V DIGITAL POWER PIN ON THE COMET QUAD




PLACE ONE CAP PER TWO 2.5V DIGITAL POWER PIN ON THE COMET QUAD




DRAWING

TITLE=POWER
ABBREV=POWER
LAST_MODIFIED=Mon Nov 20 14:42:44 2000

PMC-Sierra, Inc.

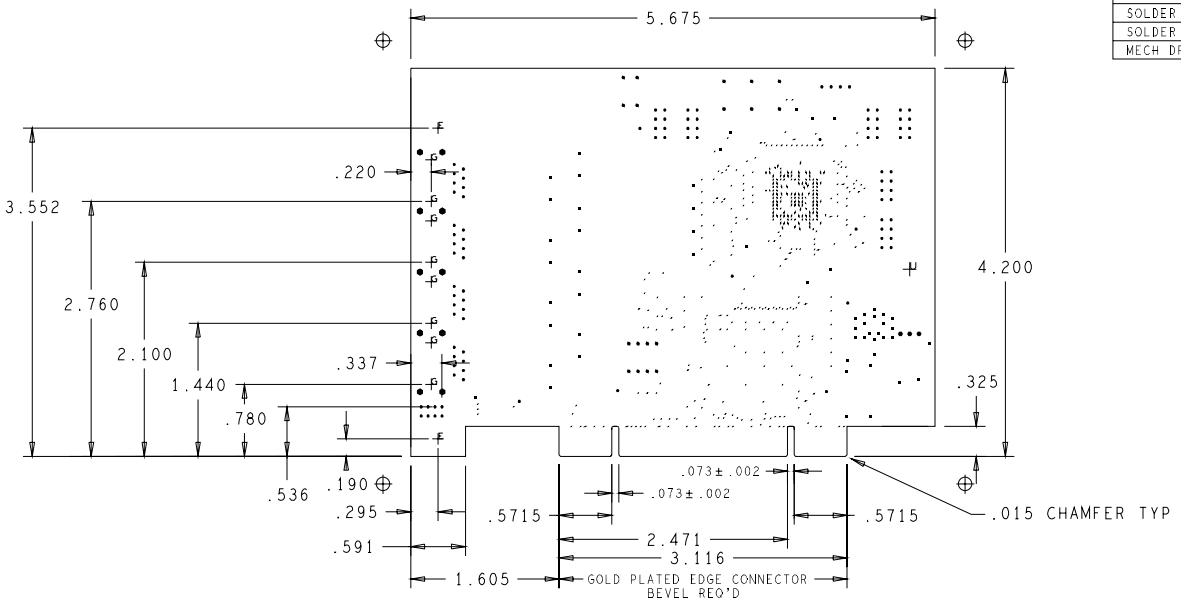
| | |
|---|---|
| DOCUMENT NUMBER: PMC-1991237<br>DOCUMENT ISSUE NUMBER: 2.0 | ISSUE DATE:<br>NOV 2000 |
| TITLE: COMET QUAD EVALUATOR DESIGN<br>POWER | REVISION NUMBER:<br>3 |
| ENGINEER: PMC-SIERRA, INC. (WT) | PAGE:6 OF 6 |

# 15 APPENDIX C: LAYOUT

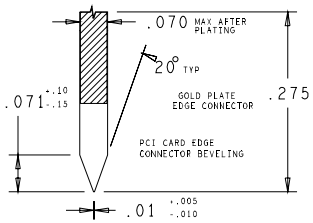
| REVISIONS | | | | | |
|---|---|---|---|---|---|
| REV | DESCRIPTION | DATE YY | MM | DD | APPROVED |
| | | | | | |

| ARTWORK FILM |
|---|
| TOP LAYER |
| GROUND PLANE |
| SIG1_VCC |
| 2V5_PLANE |
| 3V3_PLANE |
| BOTTOM LAYER |
| SILKSCREEN TOP |
| SILKSCREEN BOTTOM |
| SOLDER MASK TOP |
| SOLDER MASK BOTTOM |
| SOLDER PASTE TOP |
| SOLDER PASTE BOTTOM |
| MECH DRAWING |

| Material | Layer Type | Etch Name | Film Type | Thickness | Dielectric Constant |
|---|---|---|---|---|---|
| COPPER | CONDUCTOR | TOP | POSITIVE | 0.72 mil | ------- |
| FR-4 | DIELECTRIC | ------- | ------- | 8.0 mil | 4.2 |
| COPPER | CONDUCTOR | GND_PLANE | POSITIVE | 1.44 mil | ------- |
| FR-4 | DIELECTRIC | ------- | ------- | 8.0 mil | 4.2 |
| COPPER | CONDUCTOR | SIG1_VCC | POSITIVE | 1.44 mil | ------- |
| FR-4 | DIELECTRIC | ------- | ------- | 20.0 mil | 4.2 |
| COPPER | CONDUCTOR | 2V5_PLANE | POSITIVE | 1.44 mil | ------- |
| FR-4 | DIELECTRIC | ------- | ------- | 8.0 mil | 4.2 |
| COPPER | CONDUCTOR | 3V3_PLANE | POSITIVE | 1.44 mil | ------- |
| FR-4 | DIELECTRIC | ------- | ------- | 8.0 mil | 4.2 |
| COPPER | CONDUCTOR | BOTTOM | POSITIVE | 0.72 mil | ------- |




| FINISHED HOLES SIZE | | | |
|---|---|---|---|
| All Units are in mils | | | |
| FIGURE | SIZE | PLATED | QTY |
| · | 12.0 | PLATED | 142 |
| · | 13.0 | PLATED | 269 |
| • | 25.0 | PLATED | 55 |
| • | 36.0 | PLATED | 100 |
| • | 42.0 | PLATED | 18 |
| • | 55.0 | PLATED | 3 |
| • | 76.0 | PLATED | 16 |
| ⊕ | 125.0 | PLATED | 2 |
| ⊕ | 150.0 | PLATED | 1 |
| ⊕ | 128.0 | NOT PLATED | 8 |




PMC-SIERRA COMET QUAD EVALUATOR BOARD REV.3.0 2000

# NOTE: All 6 mils traces are 75 Ohms controlled impedance.

Notes:

1. Copper thickness is 1/2 oz. on outer layers and 1 oz. on internal layers. All track width shown under Gerber files are final trace width.
2. Total thickness of board shall be 58 mil +/- 7 mil. The stackup shown above is the final stackup of this board.
3. The outline dimension are specified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil minimum copper wall thickness. All holes size shown are final hole size.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white base ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in/in per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.

| UNLESS OTHERWISE SPECIFIED | | DATE YY | MM | DD |
|---|---|---|---|---|
| DIMENSIONS ARE IN INCHES | DRAWN | | | |
| TOLERANCES ON: | | | | |
| 2 PL DECIMALS +/- .03 | CHECKED | | | |
| 3 PL DECIMALS +/- .003 | ENGRG | | | |
| ANGLES ° | ISSUED | | | |
| FRACTIONS ° | | | | |

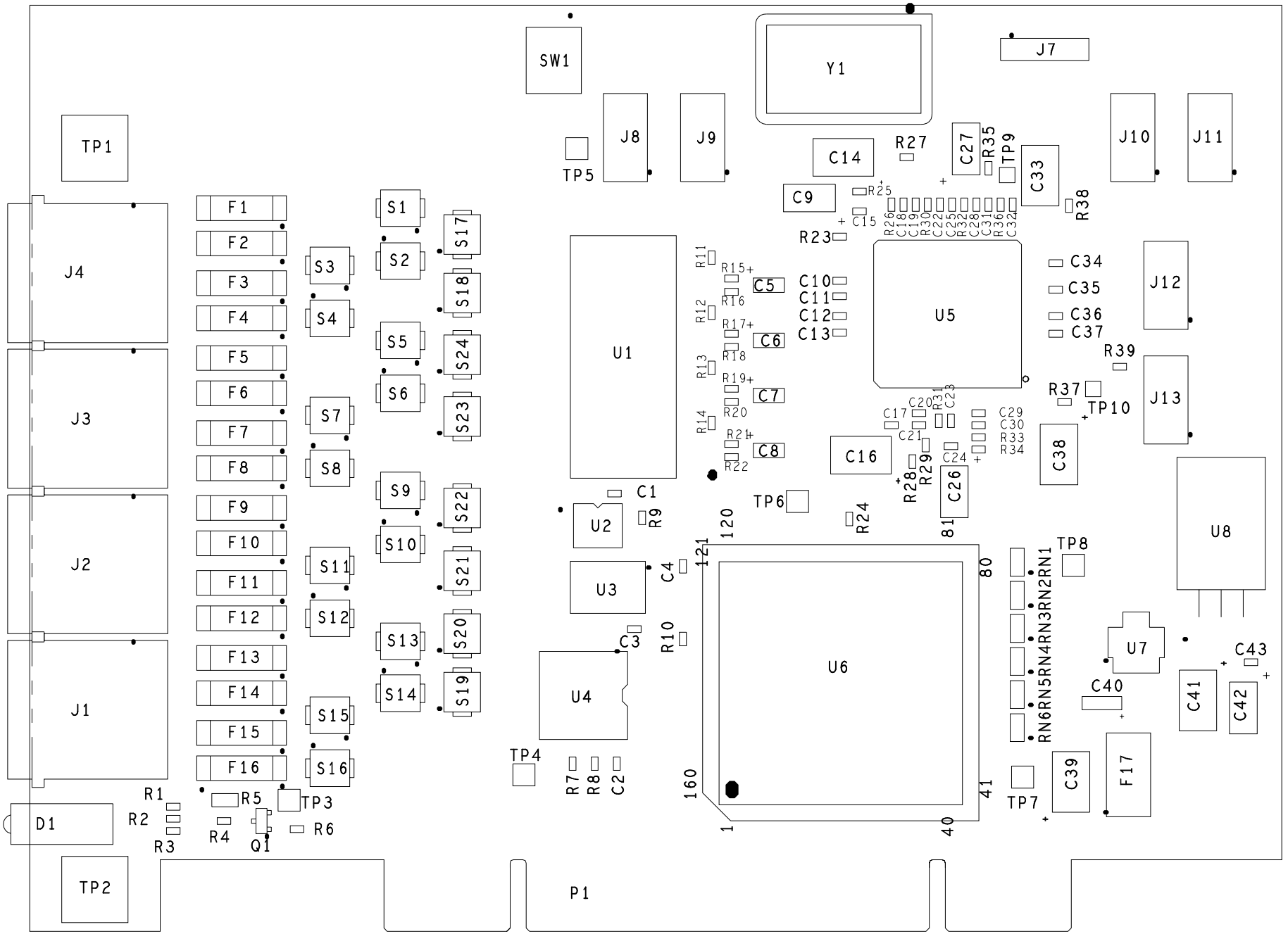

PMC-Sierra, Inc.

105-8555 Baxter Place, Burnaby B.C. Canada, V5A 4V7

Tel: 604 415-6000 Fax: 604 415-6200

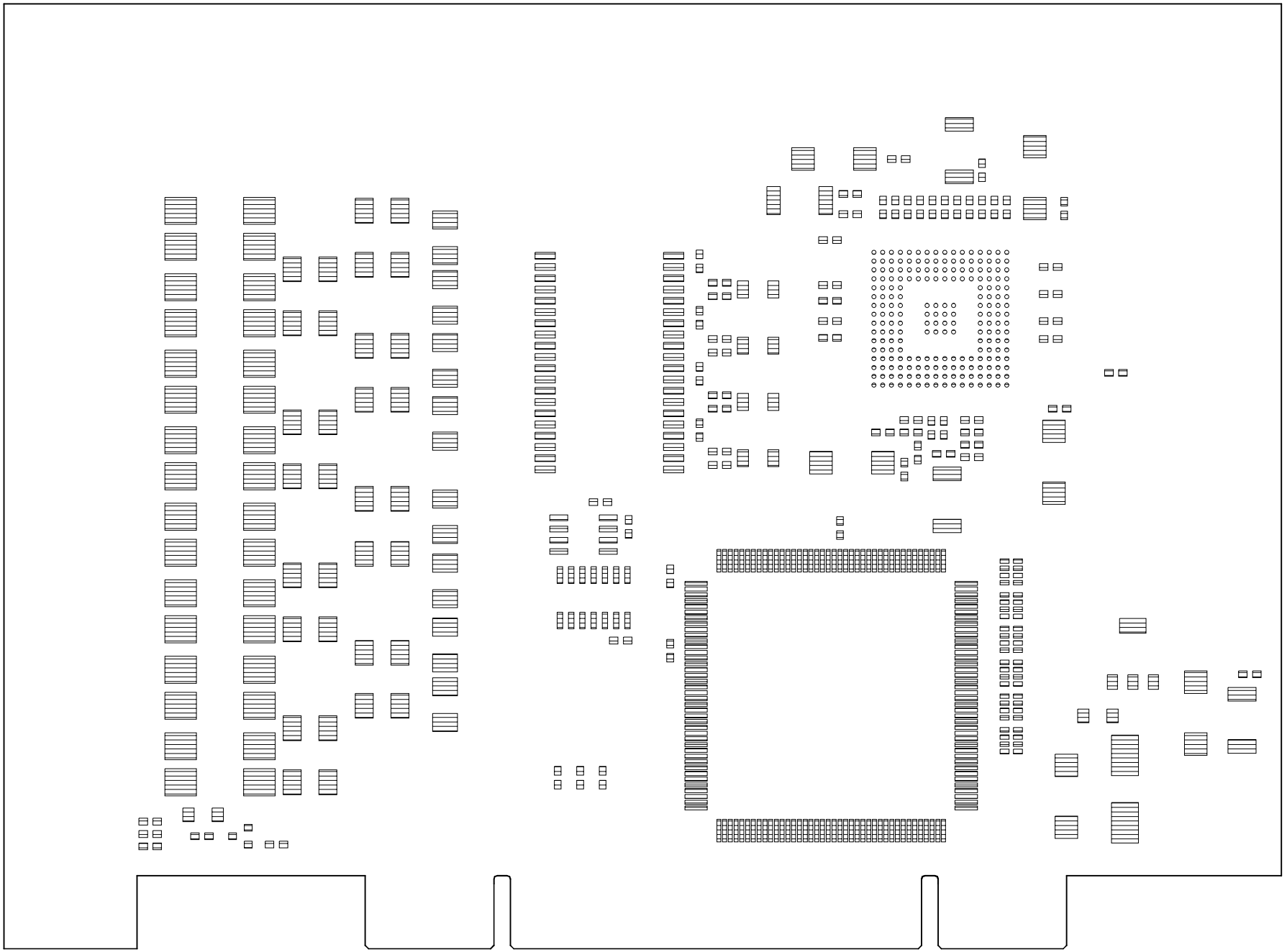

| SIZE | FSCM NO | DWG NO |
|---|---|---|
| B | | |
| SCALE | NTS | SHEET 1 OF 1 |

ASSY TOP



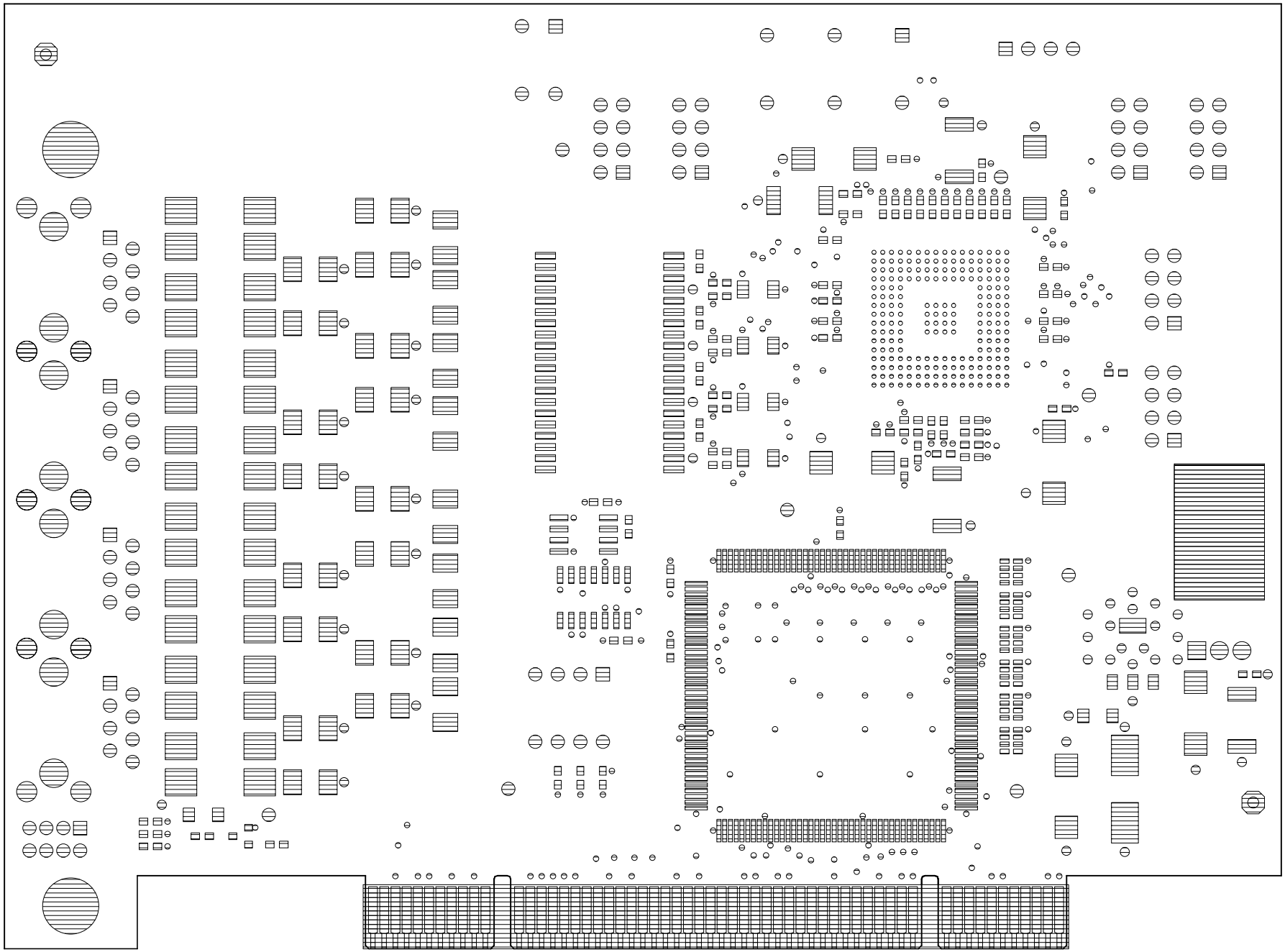

PMC-SIERRA COMET QUAD EVALUATOR BOARD REV.3.0 2000

PASTEMASK TOP



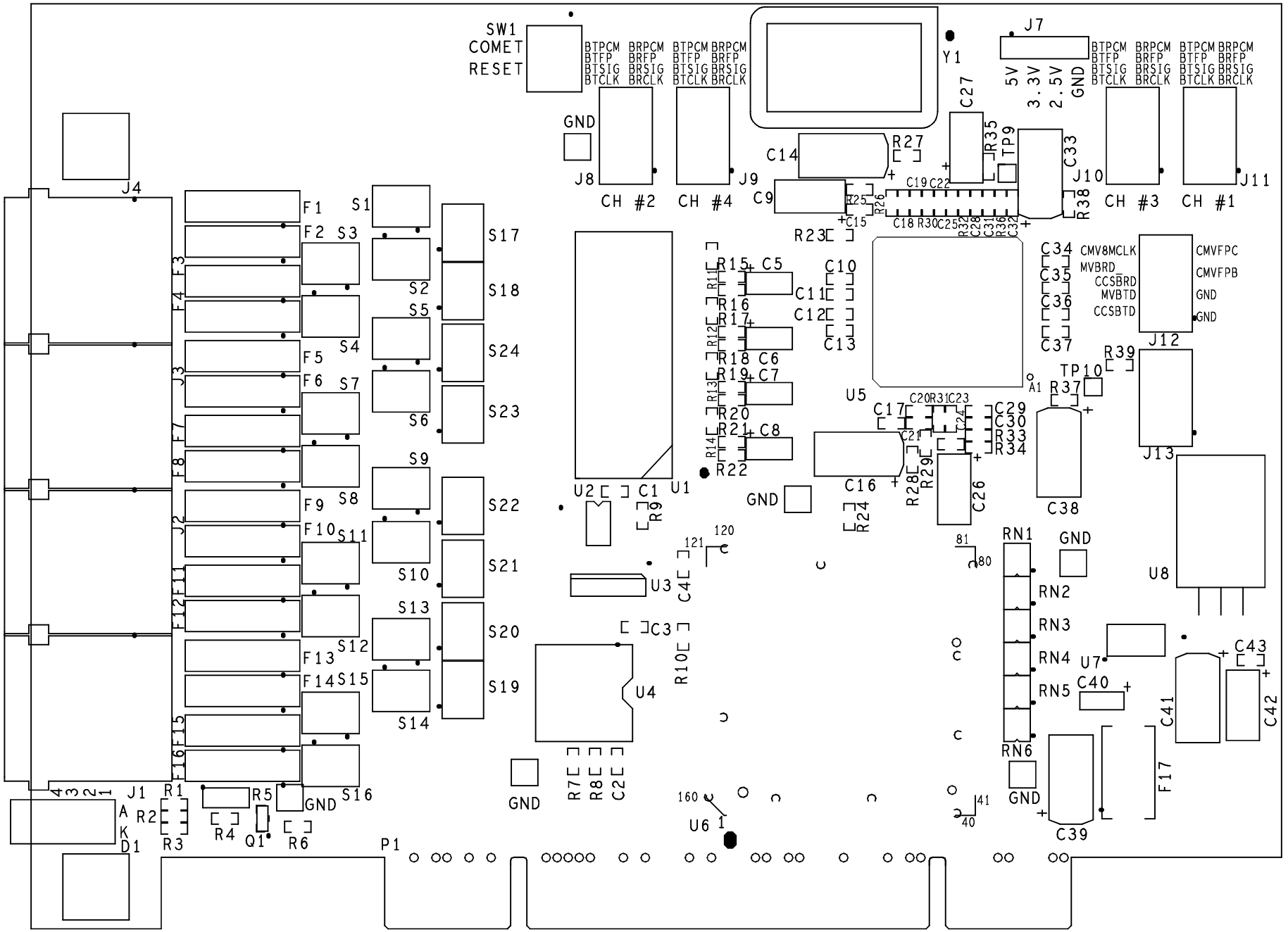
PMC-SIERRA COMET QUAD EVALUATOR BOARD REV.3.0 2000

SOLDERMASK TOP



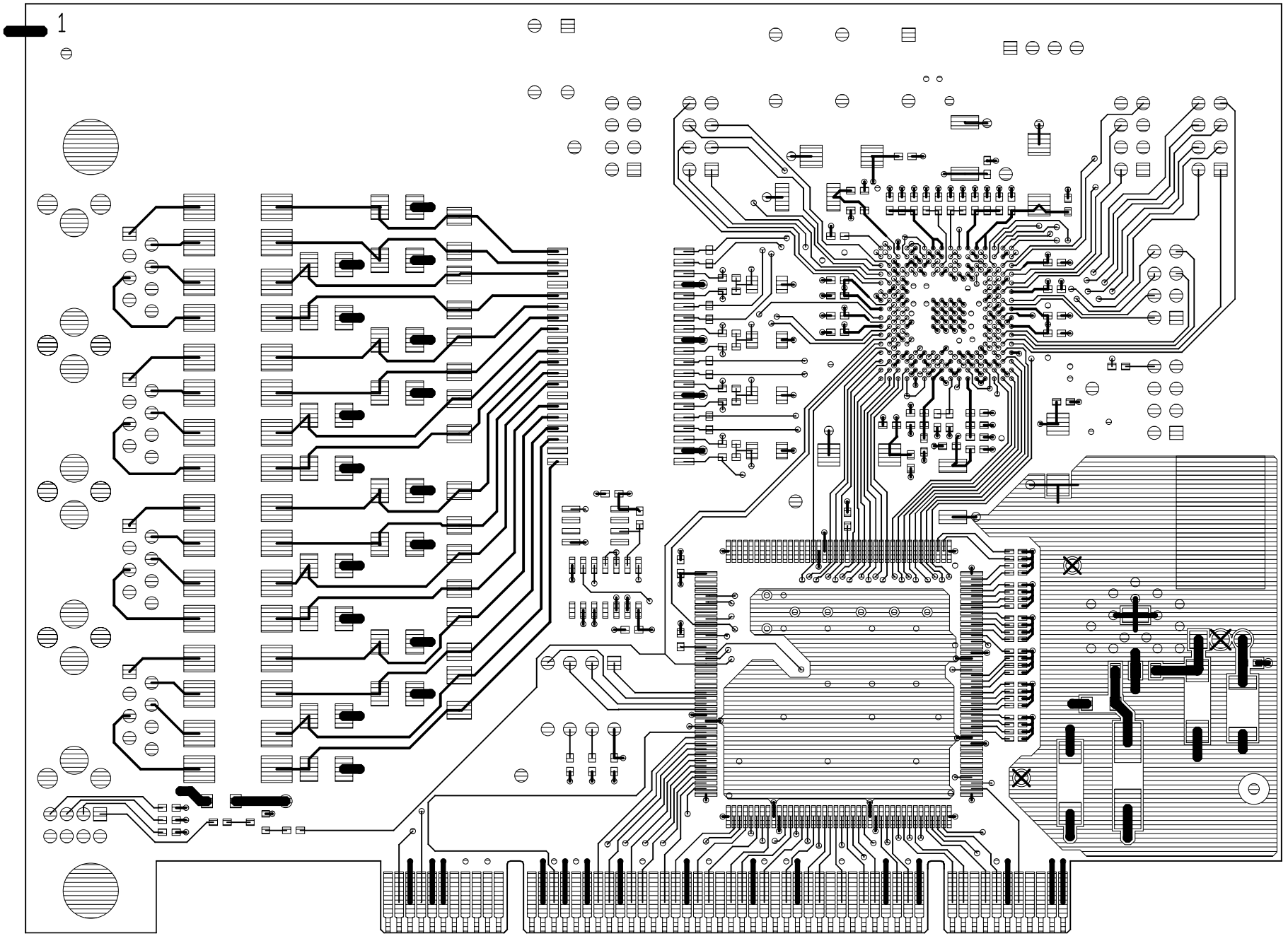
PMC-SIERRA COMET QUAD EVALUATOR BOARD REV.3.0 2000

SILK SCREEN TOP



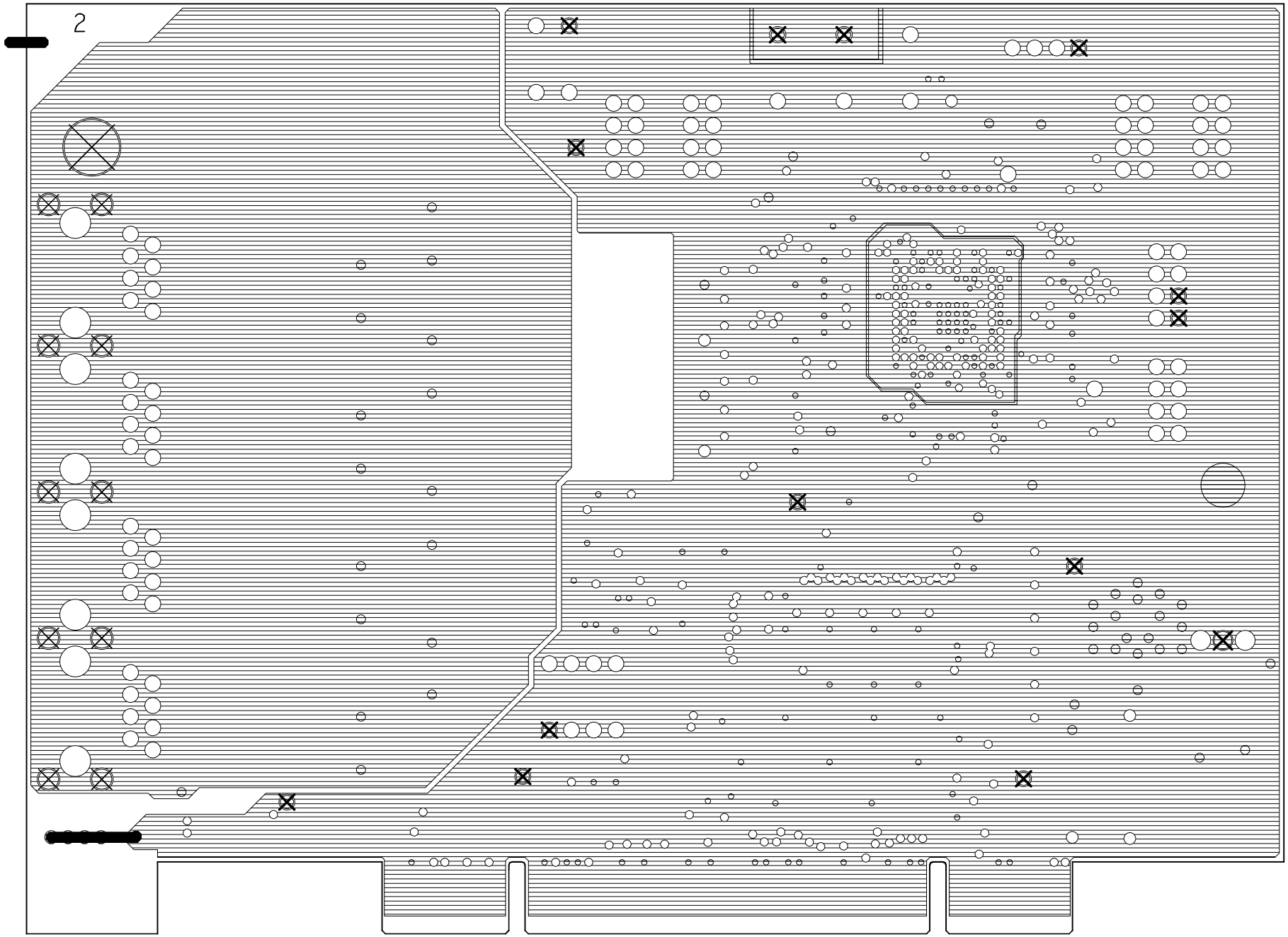

PMC-SIERRA COMET QUAD EVALUATOR BOARD REV.3.0 2000

TOP LAYER



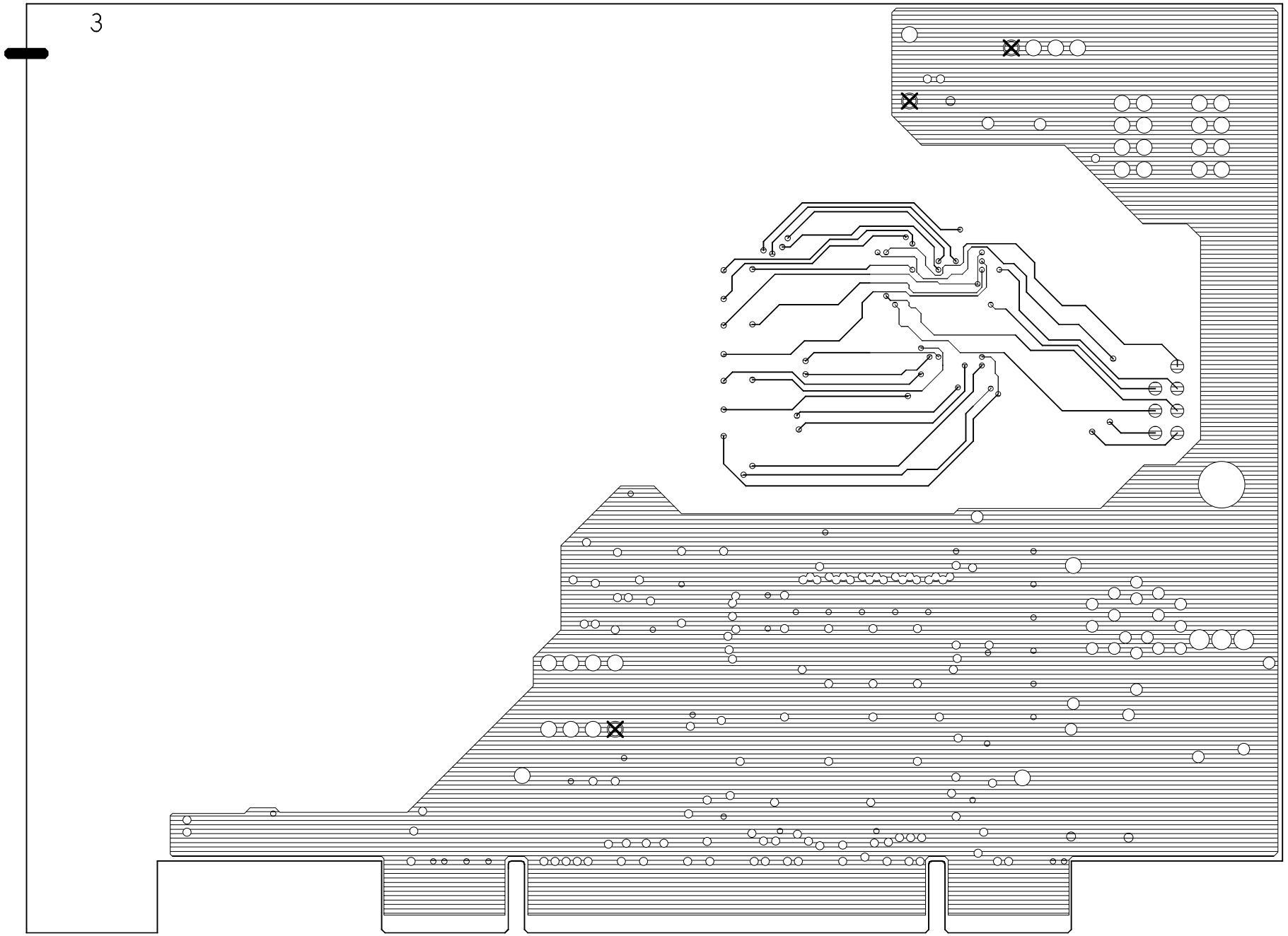

PMC-SIERRA COMET QUAD EVALUATOR BOARD REV.3.0 2000

GND_PLANE

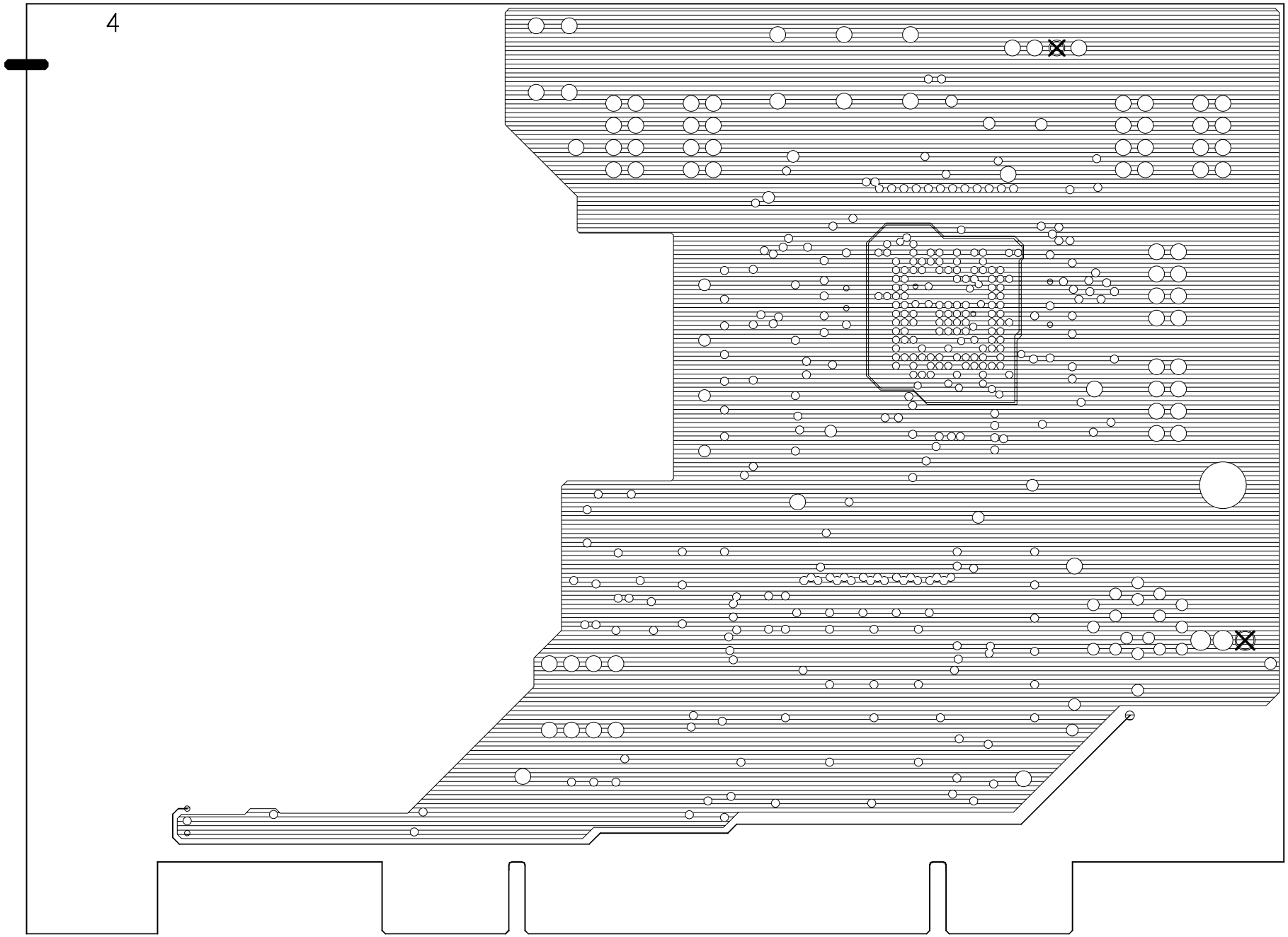


SIG1_VCC

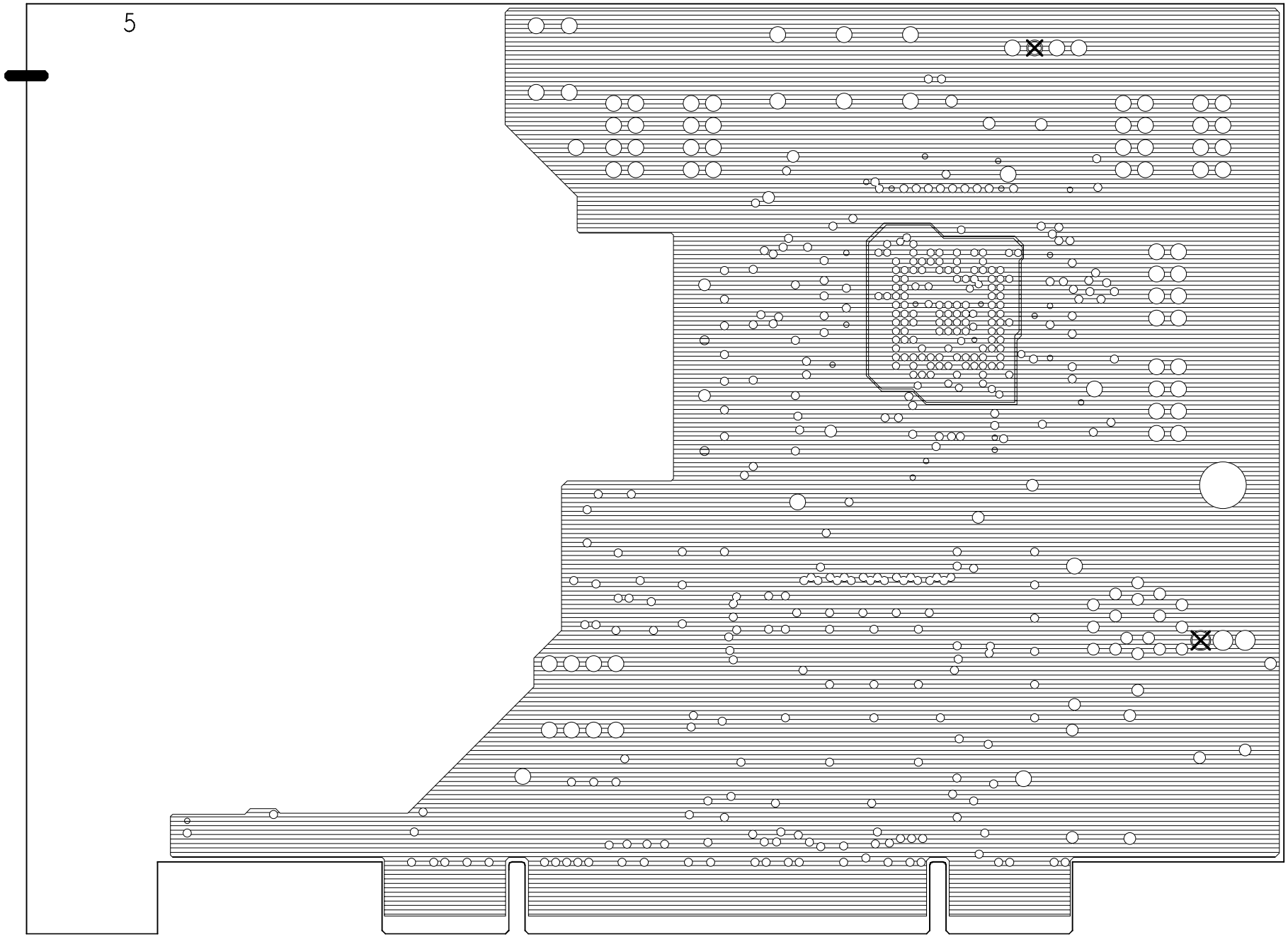
3



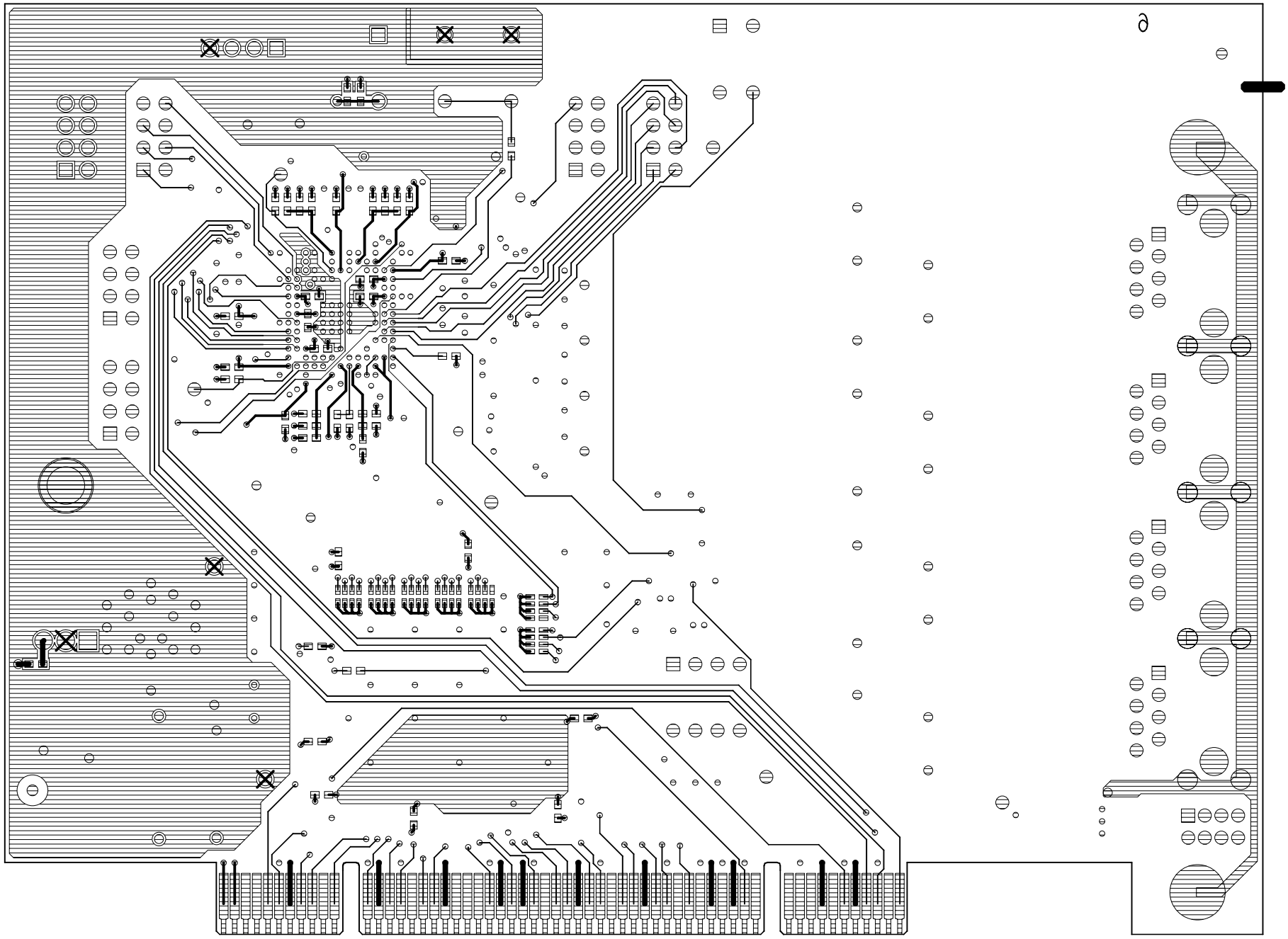
2V5_PLANE



3V3_PLANE



BOTTOM LAYER



PMC-SIERRA COMET QUAD EVALUATOR BOARD REV.3.0 2000

## NOTES

## CONTACTING PMC-SIERRA, INC.

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Canada V5A 4V7

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Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com



PMC-1991237 (P2) Issue date: January 2001