DATA SHEET

TJA1041
High speed CAN transceiver

Product specification
Supersedes data of 2002 Dec 23

2003 Feb 13

Philips
Semiconductors

PHILIPS

High speed CAN transceiver TJA1041

FEATURES

Optimized for in-vehicle high speed communication

- Fully compatible with the ISO 11898 standard
- Communication speed up to 1 Mbit/s
- Very low ElectroMagnetic Emission (EME)
- Differential receiver with wide common-mode range, offering high ElectroMagnetic Immunity (EMI)
- Passive behaviour when supply voltage is off
- Automatic I/O-level adaptation to the host controller supply voltage
- Recessive bus DC voltage stabilization for further improvement of EME behaviour
- Listen-only mode for node diagnosis and failure containment
- Allows implementation of large networks (more than 110 nodes).

Low-power management

- Very low-current in standby and sleep mode, with local and remote wake-up
- Capability to power down the entire node, still allowing local and remote wake-up
- Wake-up source recognition.

Protection and diagnosis (detection and signalling)

- TXD dominant clamping handler with diagnosis
- RXD recessive clamping handler with diagnosis
- TXD-to-RXD short-circuit handler with diagnosis
- Over-temperature protection with diagnosis
- Undervoltage detection on pins V_{CC}, $V_{I/O}$ and V_{BAT}
- Automotive environment transient protected bus pins and pin V_{BAT}
- Short-circuit proof bus pins and pin SPLIT (to battery and to ground)
- Bus line short-circuit diagnosis
- Bus dominant clamping diagnosis
- Cold start diagnosis (first battery connection).

GENERAL DESCRIPTION

The TJA1041 provides an advanced interface between the protocol controller and the physical bus in a Controller Area Network (CAN) node. The TJA1041 is primarily intended for automotive high-speed CAN applications (up to 1 Mbit/s). The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller. The TJA1041 is fully compatible to the ISO 11898 standard, and offers excellent EMC performance, very low power consumption, and passive behaviour when supply voltage is off. The advanced features include:

- Low-power management, supporting local and remote wake-up with wake-up source recognition and the capability to control the power supply in the rest of the node
- Several protection and diagnosis functions including short circuits of the bus lines and first battery connection
- Automatic adaptation of the I/O-levels, in line with the supply voltage of the controller.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TJA1041T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1041U	–	bare die; $1930 \times 3200 \times 380$ μm	–

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC voltage on pin V_{CC}	operating range	4.75	5.25	V
$V_{I/O}$	DC voltage on pin $V_{I/O}$	operating range	2.8	5.25	V
V_{BAT}	DC voltage on pin V_{BAT}	operating range	5	27	V
I_{BAT}	V_{BAT} input current	V_{BAT} = 12 V	10	30	µA
V_{CANH}	DC voltage on pin CANH	0 < V_{CC} < 5.25 V; no time limit	–27	+40	V
V_{CANL}	DC voltage on pin CANL	0 < V_{CC} < 5.25 V; no time limit	–27	+40	V
V_{SPLIT}	DC voltage on pin SPLIT	0 < V_{CC} < 5.25 V; no time limit	–27	+40	V
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM)			
		pins CANH, CANL and SPLIT	–6	+6	kV
		all other pins	–4	+4	kV
$t_{PD(TXD-RXD)}$	propagation delay TXD to RXD	V_{STB} = 0 V	40	255	ns
T_{vj}	virtual junction temperature		–40	+150	°C

BLOCK DIAGRAM

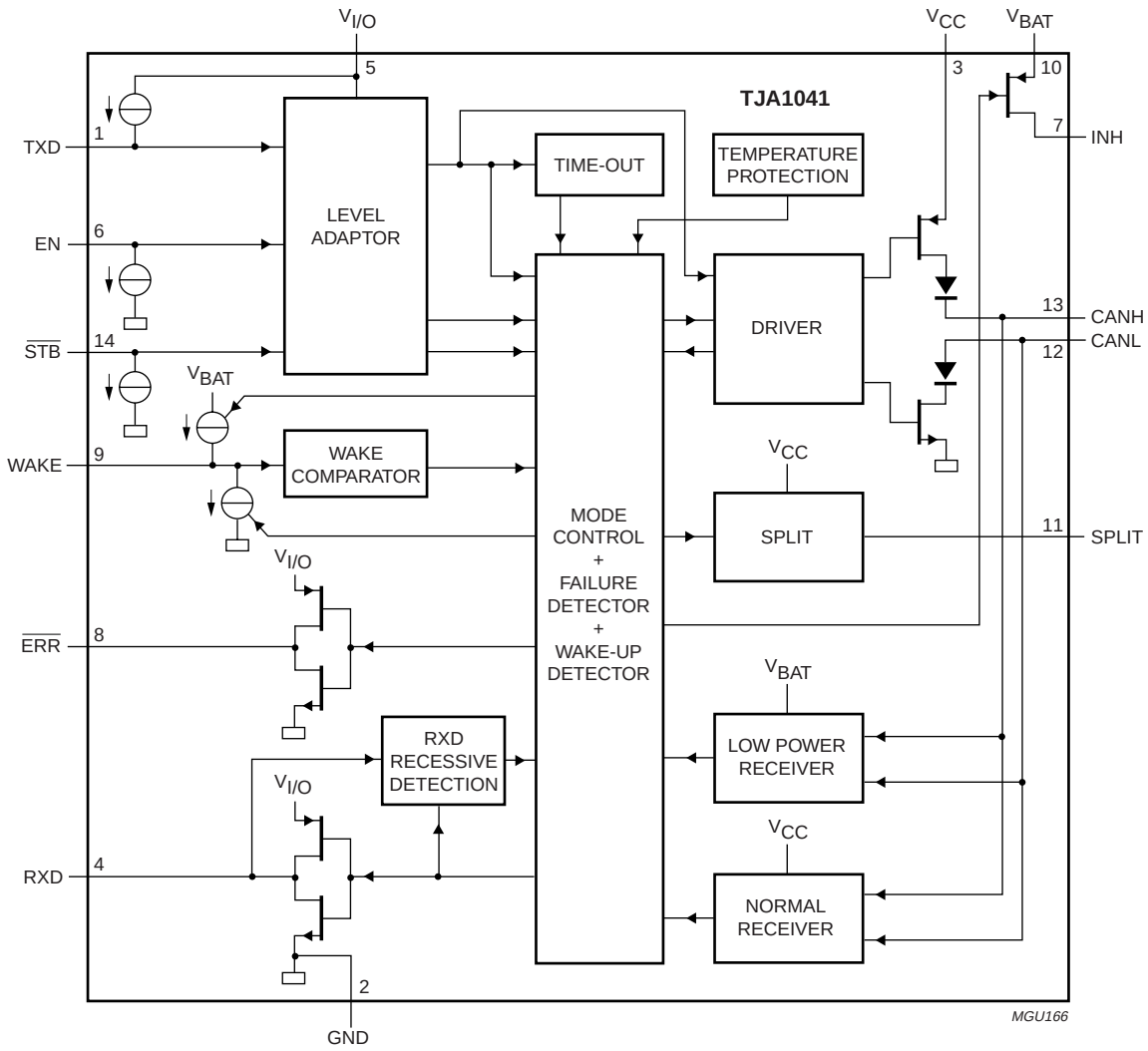


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXD	1	transmit data input
GND	2	ground
V_{CC}	3	transceiver supply voltage input
RXD	4	receive data output; reads out data from the bus lines
$V_{I/O}$	5	I/O-level adapter voltage input
EN	6	enable control input
INH	7	inhibit output for switching external voltage regulators
$\overline{ERR}$	8	error and power-on indication output (active LOW)
WAKE	9	local wake-up input
V_{BAT}	10	battery voltage input
SPLIT	11	common-mode stabilization output
CANL	12	LOW-level CAN bus line
CANH	13	HIGH-level CAN bus line
$\overline{STB}$	14	standby control input (active LOW)

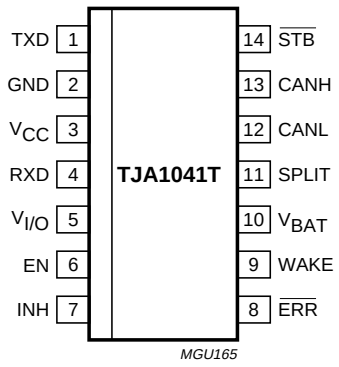


Fig.2 Pinning configuration.

FUNCTIONAL DESCRIPTION

The primary function of a CAN transceiver is to provide the CAN physical layer as described in the ISO 11898 standard. In the TJA1041 this primary function is complemented with a number of operating modes, fail-safe features and diagnosis features, which offer enhanced system reliability and advanced power management functionality.

Operating modes

The TJA1041 can be operated in five modes, each with specific features. Control pins $\overline{STB}$ and EN select the operating mode. Changing between modes also gives access to a number of diagnostics flags, available via pin $\overline{ERR}$. The following sections describe the five operating modes. Table 1 shows the conditions for selecting these modes. Figure 3 illustrates the mode transitions when V_{CC}, $V_{I/O}$ and V_{BAT} are present.

Table 1 Operating mode selection.

CONTROL PINS		INTERNAL FLAGS			OPERATING MODE	PIN INH
$\overline{STB}$	EN	UV_{NOM}	UV_{BAT}	pwon, wake-up		
X	X	set	X	X[1]	sleep mode; note 2	floating
		cleared	set	one or both set	standby mode	H
				both cleared	no change from sleep mode	floating
					standby mode from any other mode	H
L	L	cleared	cleared	one or both set	standby mode	H
				both cleared	no change from sleep mode	floating
					standby mode from any other mode	H
L	H	cleared	cleared	one or both set	standby mode	H
				both cleared	no change from sleep mode	floating
					go-to-sleep command mode from any other mode; note 3	H[3]
H	L	cleared	cleared	X	pwon/listen-only mode	H
H	H	cleared	cleared	X	normal mode; note 4	H

Notes

1. Setting the pwon flag or the wake-up flag will clear the UV_{NOM} flag.
2. The transceiver directly enters sleep mode and pin INH is set floating when the UV_{NOM} flag is set (so after the undervoltage detection time on either V_{CC} or $V_{I/O}$ has elapsed before that voltage level has recovered).
3. When go-to-sleep command mode is selected for longer than the minimum hold time of the go-to-sleep command, the transceiver will enter sleep mode and pin INH is set floating.
4. On entering normal mode the pwon flag and the wake-up flag will be cleared.

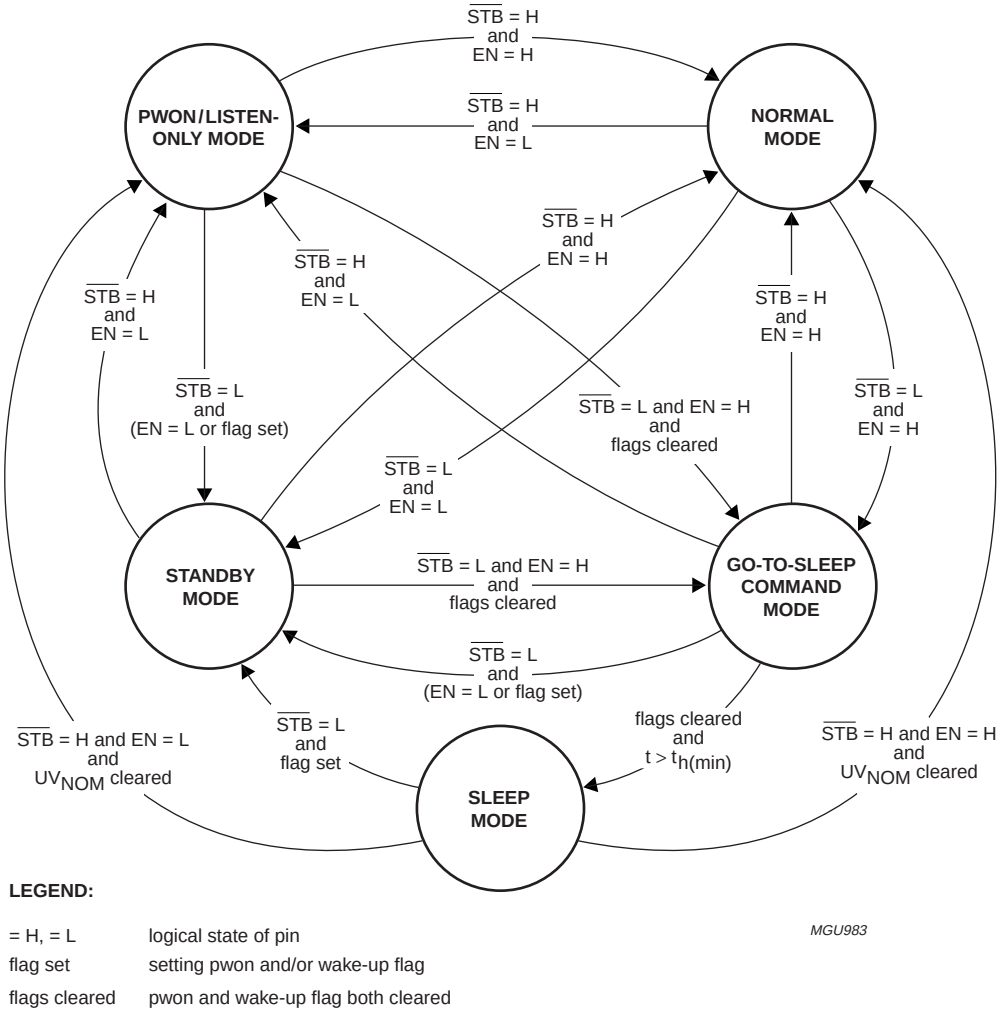


Fig.3 Mode transitions when V_{CC}, $V_{I/O}$ and V_{BAT} are present.

NORMAL MODE

Normal mode is the mode for normal bi-directional CAN communication. The receiver will convert the differential analog bus signal on pins CANH and CANL into digital data, available for output to pin RXD. The transmitter will convert digital data on pin TXD into a differential analog signal, available for output to the bus pins. The bus pins are biased at $0.5V_{CC}$ (via $R_{i(cm)}$). Pin INH is active, so voltage regulators controlled by pin INH (see Fig.4) will be active too.

PWON/LISTEN-ONLY MODE

In pwon/listen-only mode the transmitter of the transceiver is disabled, effectively providing a transceiver listen-only behaviour. The receiver will still convert the analog bus signal on pins CANH and CANL into digital data, available for output to pin RXD. As in normal mode the bus pins are biased at $0.5V_{CC}$, and pin INH remains active.

STANDBY MODE

The standby mode is the first-level power saving mode of the transceiver, offering reduced current consumption. In standby mode the transceiver is not able to transmit or receive data and the low-power receiver is activated to monitor bus activity. The bus pins are biased at ground level (via $R_{i(cm)}$). Pin INH is still active, so voltage regulators controlled by this pin INH will be too.

Pins RXD and $\overline{ERR}$ will reflect any wake-up requests (provided that $V_{I/O}$ is present).

GO-TO-SLEEP COMMAND MODE

The go-to-sleep command mode is the controlled route for entering sleep mode. In go-to-sleep command mode the transceiver behaves as if in standby mode, plus a go-to-sleep command is issued to the transceiver. After remaining in go-to-sleep command mode for the minimum hold time ($t_{h(min)}$), the transceiver will enter sleep mode. The transceiver will not enter the sleep mode if the state of pins $\overline{STB}$ or EN is changed or the UV_{BAT}, pwon or wake-up flag is set before $t_{h(min)}$ has expired.

SLEEP MODE

The sleep mode is the second-level power saving mode of the transceiver. Sleep mode is entered via the go-to-sleep command mode, and also when the undervoltage detection time on either V_{CC} or $V_{I/O}$ elapses before that voltage level has recovered. In sleep mode the transceiver still behaves as described for standby mode, but now pin INH is set floating. Voltage regulators controlled by pin INH will be switched off, and the current into pin V_{BAT} is reduced to a minimum. Waking up a node from sleep mode is possible via the wake-up flag and (as long as the UV_{NOM} flag is not set) via pin $\overline{STB}$.

Internal flags

The TJA1041 makes use of seven internal flags for its fail-safe fallback mode control and system diagnosis support. Table 1 shows the relation between flags and operating modes of the transceiver. Five of the internal flags can be made available to the controller via pin $\overline{ERR}$. Table 2 shows the details on how to access these flags. The following sections describe the seven internal flags.

Table 2 Accessing internal flags via pin $\overline{ERR}$.

Internal flag	Flag is available on pin $\overline{ERR}$ (note 1)	Flag is cleared
UV_{NOM}	no	by setting the pwon or wake-up flag
UV_{BAT}	no	when V_{BAT} has recovered
pwon	in pwon/listen-only mode (coming from standby mode, go-to-sleep command mode, or sleep mode)	on entering normal mode
wake-up	in standby mode, go-to-sleep command mode, and sleep mode (provided that $V_{I/O}$ is present)	on entering normal mode, or by setting the pwon or UV_{NOM} flag
wake-up source	in normal mode (before the fourth dominant to recessive edge on pin TXD; note 2)	on leaving normal mode, or by setting the pwon flag
bus failure	in normal mode (after the fourth dominant to recessive edge on pin TXD; note 2)	on re-entering normal mode
local failure	in pwon/listen-only mode (coming from normal mode)	on entering normal mode or when RXD is dominant while TXD is recessive (provided that all local failures are resolved)

Notes

1. Pin $\overline{ERR}$ is an active-LOW output, so a LOW level indicates a set flag and a HIGH level indicates a cleared flag. Allow pin $\overline{ERR}$ to stabilize for at least 8 μs after changing operating modes.
2. Allow for a TXD dominant time of at least 4 μs per dominant-recessive cycle.

UV_{NOM} FLAG

UV_{NOM} is the V_{CC} and $V_{I/O}$ undervoltage detection flag. The flag is set when the voltage on pin V_{CC} drops below $V_{CC(sleep)}$ for longer than $t_{UV(VCC)}$ or when the voltage on pin $V_{I/O}$ drops below $V_{I/O(sleep)}$ for longer than $t_{UV(VI/O)}$. When the UV_{NOM} flag is set, the transceiver will enter sleep mode to save power and not disturb the bus. In sleep mode the voltage regulators connected to pin INH are disabled, avoiding the extra power consumption in case of a short-circuit condition. After a waiting time (fixed by the same timers used for setting UV_{NOM}) any wake-up request or setting of the pwon flag will clear UV_{NOM} and the timers, allowing the voltage regulators to be reactivated at least until UV_{NOM} is set again.

UV_{BAT} FLAG

UV_{BAT} is the V_{BAT} undervoltage detection flag. The flag is set when the voltage on pin V_{BAT} drops below $V_{BAT(stb)}$. When UV_{BAT} is set, the transceiver will try to enter standby mode to save power and not disturb the bus. UV_{BAT} is cleared when the voltage on pin V_{BAT} has recovered. The transceiver will then return to the operating mode determined by the logic state of pins $\overline{STB}$ and EN.

PWON FLAG

Pwon is the V_{BAT} power-on flag. This flag is set when the voltage on pin V_{BAT} has recovered after it dropped below $V_{BAT(pwon)}$, particularly after the transceiver was disconnected from the battery. By setting the pwon flag, the UV_{NOM} flag and timers are cleared and the transceiver can not enter sleep mode. This ensures that any voltage regulator connected to pin INH is activated when the node is reconnected to the battery. In pwon/listen-only mode the pwon flag can be made available on pin $\overline{ERR}$. The flag is cleared when the transceiver enters normal mode.

WAKE-UP FLAG

The wake-up flag is set when the transceiver detects a local or a remote wake-up request. A local wake-up request is detected when a logic state change on pin WAKE remains stable for at least t_{wake}. A remote wake-up request is detected when the bus remains in dominant state for at least t_{BUS}. The wake-up flag can only be set in standby mode, go-to-sleep command mode or sleep mode. Setting of the flag is blocked during the UV_{NOM} flag waiting time. By setting the wake-up flag, the UV_{NOM} flag and timers are cleared. The wake-up flag is immediately available on pins $\overline{ERR}$ and RXD (provided that $V_{I/O}$ is present). The flag is cleared at power-on, or when the UV_{NOM} flag is set or the transceiver enters normal mode.

WAKE-UP SOURCE FLAG

Wake-up source recognition is provided via the wake-up source flag, which is set when the wake-up flag is set by a local wake-up request via pin WAKE. The wake-up source flag can only be set after the pwon flag is cleared.
In normal mode the wake-up source flag can be made available on pin $\overline{ERR}$. The flag is cleared at power-on or when the transceiver leaves normal mode.

BUS FAILURE FLAG

The bus failure flag is set if the transceiver detects a bus line short-circuit condition to V_{BAT}, V_{CC} or GND during four consecutive dominant-recessive cycles on pin TXD, when trying to drive the bus lines dominant. In normal mode the bus failure flag can be made available on pin $\overline{ERR}$. The flag is cleared when the transceiver re-enters normal mode.

LOCAL FAILURE FLAG

In normal mode or pwon/listen-only mode the transceiver can recognize five different local failures, and will combine them into one local failure flag. The five local failures are: TXD dominant clamping, RXD recessive clamping, a TXD-to-RXD short circuit, bus dominant clamping, and over-temperature. Nature and detection of these local failures is described in Section “Local failures”.
In pwon/listen-only mode the local failure flag can be made available on pin $\overline{ERR}$. The flag is cleared when entering normal mode or when RXD is dominant while TXD is recessive, provided that all local failures are resolved.

Local failures

The TJA1041 can detect five different local failure conditions. Any of these failures will set the local failure flag, and in most cases the transmitter of the transceiver will be disabled. The following sections give the details.

TXD DOMINANT CLAMPING DETECTION

A permanent LOW level on pin TXD (due to a hardware or software application failure) would drive the CAN bus into a permanent dominant state, blocking all network communication. The TXD dominant time-out function prevents such a network lock-up by disabling the transmitter of the transceiver if pin TXD remains at a LOW level for longer than the TXD dominant time-out $t_{dom(TXD)}$. The $t_{dom(TXD)}$ timer defines the minimum possible bit rate

of 40 kbit/s. The transmitter remains disabled until the local failure flag is cleared.

RXD RECESSIVE CLAMPING DETECTION

An RXD pin clamped to HIGH level will prevent the controller connected to this pin from recognizing a bus dominant state. So the controller can start messages at any time, which is likely to disturb all bus communication.. RXD recessive clamping detection prevents this effect by disabling the transmitter when the bus is in dominant state without RXD reflecting this. The transmitter remains disabled until the local failure flag is cleared.

TXD-TO-RXD SHORT-CIRCUIT DETECTION

A short-circuit between pins RXD and TXD would keep the bus in a permanent dominant state once the bus is driven dominant, because the low-side driver of RXD is typically stronger than the high-side driver of the controller connected to TXD. The TXD-to-RXD short-circuit detection prevents such a network lock-up by disabling the transmitter. The transmitter remains disabled until the local failure flag is cleared.

BUS DOMINANT CLAMPING DETECTION

A CAN bus short circuit (to V_{BAT}, V_{CC} or GND) or a failure in one of the other network nodes could result in a differential voltage on the bus high enough to represent a bus dominant state. Because a node will not start transmission if the bus is dominant, the normal bus failure detection will not detect this failure, but the bus dominant clamping detection will. The local failure flag is set if the dominant state on the bus persists for longer than $t_{dom(bus)}$. By checking this flag, the controller can determine if a clamped bus is blocking network communication. There is no need to disable the transmitter. Note that the local failure flag does not retain a bus dominant clamping failure, and is released as soon as the bus returns to recessive state.

OVER-TEMPERATURE DETECTION

To protect the output drivers of the transceiver against overheating, the transmitter will be disabled if the virtual junction temperature exceeds the shutdown junction temperature $T_{j(sd)}$. The transmitter remains disabled until the local failure flag is cleared.

Recessive bus voltage stabilization

In recessive state the output impedance of transceivers is relatively high. In a partially powered network (supply voltage is off in some of the nodes) any deactivated transceiver with a significant leakage current is likely to load the recessive bus to ground. This will cause a common-mode voltage step each time transmission starts, resulting in increased ElectroMagnetic Emission (EME). Using pin SPLIT of the TJA1041 in combination with split termination (see Fig.5) will reduce this step effect. In normal mode and pwon/listen-only mode pin SPLIT provides a stabilized $0.5V_{CC}$ DC voltage. In standby mode, go-to-sleep command mode and sleep mode pin SPLIT is set floating.

I/O level adapter

The TJA1041 is equipped with a built-in I/O-level adapter. By using the supply voltage of the controller (to be supplied at pin $V_{I/O}$) the level adapter ratio-metrically scales the I/O-levels of the transceiver. For pins TXD, $\overline{STB}$ and EN the digital input threshold level is adjusted, and for pins RXD and $\overline{ERR}$ the HIGH-level output voltage is adjusted. This allows the transceiver to be directly interfaced with controllers on supply voltages between 2.8 V and 5.25 V, without the need for glue logic.

Pin WAKE

Pin WAKE of the TJA1041 allows local wake-up triggering by a LOW to HIGH state change as well as a HIGH to LOW state change. This gives maximum flexibility when designing a local wake-up circuit. To keep current consumption at a minimum, after a t_{wake} delay the internal bias voltage of pin WAKE will follow the logic state of this pin. A HIGH level on pin WAKE is followed by an internal pull-up to V_{BAT}. A LOW level on pin WAKE is followed by an internal pull-down towards GND.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC voltage on pin V_{CC}	no time limit	–0.3	+6	V
		operating range	4.75	5.25	V
$V_{I/O}$	DC voltage on pin $V_{I/O}$	no time limit	–0.3	+6	V
		operating range	2.8	5.25	V
V_{BAT}	DC voltage on pin V_{BAT}	no time limit	–0.3	+40	V
		operating range	5	27	V
		load dump	–	40	V
V_{TXD}	DC voltage on pin TXD		–0.3	$V_{I/O}$ + 0.3	V
V_{RXD}	DC voltage on pin RXD		–0.3	$V_{I/O}$ + 0.3	V
V_{STB}	DC voltage on pin $\overline{STB}$		–0.3	$V_{I/O}$ + 0.3	V
V_{EN}	DC voltage on pin EN		–0.3	$V_{I/O}$ + 0.3	V
V_{ERR}	DC voltage on pin $\overline{ERR}$		–0.3	$V_{I/O}$ + 0.3	V
V_{INH}	DC voltage on pin INH		–0.3	V_{BAT} + 0.3	V
V_{WAKE}	DC voltage on pin WAKE		–0.3	V_{BAT} + 0.3	V
I_{WAKE}	DC current on pin WAKE		–	–15	mA
V_{CANH}	DC voltage on pin CANH	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{CANL}	DC voltage on pin CANL	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{SPLIT}	DC voltage on pin SPLIT	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{trt}	transient voltages on pins CANH, CANL, SPLIT and V_{BAT}	according to ISO 7637; see Fig.6	–200	+200	V
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM); note 1			
		pins CANH, CANL and SPLIT	–6	+6	kV
		all other pins	–4	+4	kV
		Machine Model (MM); note 2	–200	+200	V
T_{vj}	virtual junction temperature	note 3	–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C

Notes

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor via a 0.75 μH series inductor and a 10 Ω series resistor.
3. Junction temperature in accordance with IEC 60747-1. An alternative definition is: $T_{vj} = T_{amb} + P \times R_{th(vj\text{-}amb)}$, where $R_{th(vj\text{-}amb)}$ is a fixed value. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient in SO14 package	in free air	120	K/W
$R_{th(j\text{-}s)}$	thermal resistance from junction to substrate of bare die	in free air	40	K/W

CHARACTERISTICS

V_{CC} = 4.75 to 5.25 V; $V_{I/O}$ = 2.8 V to V_{CC}; V_{BAT} = 5 to 27 V; R_L = 60 Ω; T_{vj} = –40 to +150 °C; unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the device; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies (pins V_{BAT}, V_{CC} and $V_{I/O}$)						
$V_{CC(sleep)}$	V_{CC} undervoltage detection level for forced sleep mode	V_{BAT} = 12 V (fail-safe)	2.75	3.3	4.5	V
$V_{I/O(sleep)}$	$V_{I/O}$ undervoltage detection level for forced sleep mode		0.5	1.5	2	V
$V_{BAT(stb)}$	V_{BAT} voltage level for fail-safe fallback mode	V_{CC} = 5 V (fail-safe)	2.75	3.3	4.5	V
$V_{BAT(pwon)}$	V_{BAT} voltage level for setting pwon flag	V_{CC} = 0 V	2.5	3.3	4.1	V
I_{CC}	V_{CC} input current	normal mode; V_{TXD} = 0 V (dominant)	25	55	80	mA
		normal or pwon/listen-only mode; V_{TXD} = $V_{I/O}$ (recessive)	2	6	10	mA
		standby or sleep mode	–	1	10	µA
$I_{I/O}$	$V_{I/O}$ input current	normal mode; V_{TXD} = 0 V (dominant)	100	350	1000	µA
		normal or pwon/listen-only mode; V_{TXD} = $V_{I/O}$ (recessive)	15	80	200	µA
		standby or sleep mode	–	0	5	µA
I_{BAT}	V_{BAT} input current	normal or pwon/listen-only mode	15	30	40	µA
		standby mode; V_{CC} > 4.75 V; $V_{I/O}$ = 2.8 V; V_{INH} = V_{WAKE} = V_{BAT} = 12 V	10	20	30	µA
		sleep mode; V_{INH} = V_{CC} = $V_{I/O}$ = 0 V; V_{WAKE} = V_{BAT} = 12 V	10	20	30	µA
Transmitter data input (pin TXD)						
V_{IH}	HIGH-level input voltage		$0.7V_{I/O}$	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	$0.3V_{I/O}$	V
I_{IH}	HIGH-level input current	normal or pwon/listen-only mode; V_{TXD} = $V_{I/O}$	–5	0	+5	µA
I_{IL}	LOW-level input current	normal or pwon/listen-only mode; V_{TXD} = $0.3V_{I/O}$	–70	–250	–500	µA
C_i	input capacitance	not tested	–	5	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver data output (pin RXD)						
I_{OH}	HIGH-level output current	$V_{RXD} = V_{I/O} - 0.4$ V; $V_{I/O} = V_{CC}$	–1	–3	–6	mA
I_{OL}	LOW-level output current	$V_{RXD} = 0.4$ V; $V_{TXD} = V_{I/O}$; bus dominant	2	5	12	mA
Standby and enable control inputs (pins $\overline{STB}$ and EN)						
V_{IH}	HIGH-level input voltage		$0.7V_{I/O}$	–	$V_{CC} + 0.3$	V
V_{IL}	LOW-level input voltage		–0.3	–	$0.3V_{I/O}$	V
I_{IH}	HIGH-level input current	$V_{STB} = V_{EN} = 0.7V_{I/O}$	1	4	10	µA
I_{IL}	LOW-level input current	$V_{STB} = V_{EN} = 0$ V	–	0	–1	µA
Error and power-on indication output (pin $\overline{ERR}$)						
I_{OH}	HIGH-level output current	$V_{ERR} = V_{I/O} - 0.4$ V; $V_{I/O} = V_{CC}$	–4	–20	–50	µA
I_{OL}	LOW-level output current	$V_{ERR} = 0.4$ V	0.1	0.2	0.35	mA
Local wake-up input (pin WAKE)						
I_{IH}	HIGH-level input current	$V_{WAKE} = V_{BAT} - 1.9$ V	–1	–5	–10	µA
I_{IL}	LOW-level input current	$V_{WAKE} = V_{BAT} - 3.1$ V	1	5	10	µA
V_{th}	threshold voltage	$V_{STB} = 0$ V	$V_{BAT} - 3$	$V_{BAT} - 2.5$	$V_{BAT} - 2$	V
Inhibit output (pin INH)						
ΔV_H	HIGH-level voltage drop	$I_{INH} = -0.18$ mA	0.05	0.2	0.8	V
$\lvert I_L \rvert$	leakage current	sleep mode	–	0	5	µA
Bus lines (pins CANH and CANL)						
$V_{O(dom)}$	dominant output voltage	$V_{TXD} = 0$ V				
		pin CANH	3	3.6	4.25	V
		pin CANL	0.5	1.4	1.75	V
$V_{O(dom)(m)}$	matching of dominant output voltage ($V_{CC} - V_{CANH} - V_{CANL}$)		–0.1	–	+0.15	V
$V_{O(dif)(bus)}$	differential bus output voltage ($V_{CANH} - V_{CANL}$)	$V_{TXD} = 0$ V (dominant); 45 Ω < R_L < 65 Ω	1.5	–	3.0	V
		$V_{TXD} = V_{I/O}$ (recessive); no load	–50	–	+50	mV
$V_{O(reces)}$	recessive output voltage	normal or pwon/listen-only mode; $V_{TXD} = V_{I/O}$; no load	2	$0.5V_{CC}$	3	V
		standby or sleep mode; no load	–0.1	0	+0.1	V
$I_{O(sc)}$	short-circuit output current	$V_{TXD} = 0$ V (dominant)				
		pin CANH; $V_{CANH} = 0$ V	–45	–70	–95	mA
		pin CANL; $V_{CANL} = 40$ V	45	70	95	mA
$I_{O(reces)}$	recessive output current	$-27 \text{ V} < V_{CAN} < 32$ V	–2.5	–	+2.5	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{dif(th)}$	differential receiver threshold voltage	normal or pwon/listen-only mode (see Fig.7); $-12\ V < V_{CANH} < 12\ V$; $-12\ V < V_{CANL} < 12\ V$	0.5	0.7	0.9	V
		standby or sleep mode; $-12\ V < V_{CANH} < 12\ V$; $-12\ V < V_{CANL} < 12\ V$	0.5	0.7	1.15	V
$V_{dif(hys)}$	differential receiver hysteresis	normal or pwon/listen-only mode (see Fig.7); $-12\ V < V_{CANH} < 12\ V$; $-12\ V < V_{CANL} < 12\ V$	50	70	100	mV
I_{LI}	input leakage current	$V_{CC} = 0\ V$; $V_{CANH} = V_{CANL} = 5\ V$	100	170	250	μA
$R_{i(cm)}$	common-mode input resistance		15	25	35	kΩ
$R_{i(cm)(m)}$	common-mode input resistance matching	$V_{CANH} = V_{CANL}$	−3	0	+3	%
$R_{i(dif)}$	differential input resistance		25	50	75	kΩ
$C_{i(cm)}$	common-mode input capacitance	$V_{TXD} = V_{CC}$; not tested	–	–	20	pF
$C_{i(dif)}$	differential input capacitance	$V_{TXD} = V_{CC}$; not tested	–	–	10	pF
$R_{sc(bus)}$	detectable short-circuit resistance between bus lines and V_{BAT}, V_{CC} and GND	normal mode	0	–	50	Ω
Common-mode stabilization output (pin SPLIT)						
V_o	output voltage	normal or pwon/listen-only mode; $-500\ \mu A < I_{SPLIT} < 500\ \mu A$	$0.3V_{CC}$	$0.5V_{CC}$	$0.7V_{CC}$	V
$\lvert I_L \rvert$	leakage current	standby or sleep mode; $-22\ V < V_{SPLIT} < 35\ V$	–	0	5	μA
Timing characteristics; see Figs 8 and 9						
$t_{d(TXD-BUSon)}$	delay TXD to bus active	normal mode	25	70	110	ns
$t_{d(TXD-BUSoff)}$	delay TXD to bus inactive	normal mode	10	50	95	ns
$t_{d(BUSon-RXD)}$	delay bus active to RXD	normal or pwon/listen-only mode	15	65	115	ns
$t_{d(BUSoff-RXD)}$	delay bus inactive to RXD	normal or pwon/listen-only mode	35	100	160	ns
$t_{PD(TXD-RXD)}$	propagation delay TXD to RXD	$V_{STB} = 0\ V$	40	–	255	ns
$t_{UV(VCC)}$, $t_{UV(VI/O)}$	undervoltage detection time on V_{CC} and $V_{I/O}$		5	10	12.5	ms
$t_{dom(TXD)}$	TXD dominant time-out	$V_{TXD} = 0\ V$	300	600	1000	μs
$t_{dom(bus)}$	bus dominant time-out	$V_{dif} > 0.9\ V$	300	600	1000	μs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{h(min)}$	minimum hold time of go-to-sleep command		20	35	50	µs
t_{BUS}	dominant time for wake-up via bus	standby or sleep mode; V_{BAT} = 12 V	0.75	1.75	5	µs
t_{wake}	minimum wake-up time after receiving a falling or rising edge	standby or sleep mode; V_{BAT} = 12 V	5	25	50	µs
Thermal shutdown						
$T_{j(sd)}$	shutdown junction temperature		155	165	180	°C

Note

1. All parameters are guaranteed over the virtual junction temperature range by design, but only 100% tested at T_{amb} = 125 °C for dies on wafer level and in addition to this, 100% tested at T_{amb} = 125 °C for cased products, unless specified otherwise. For bare dies, all parameters are only guaranteed with the reverse side of the die connected to ground.

TEST AND APPLICATION INFORMATION

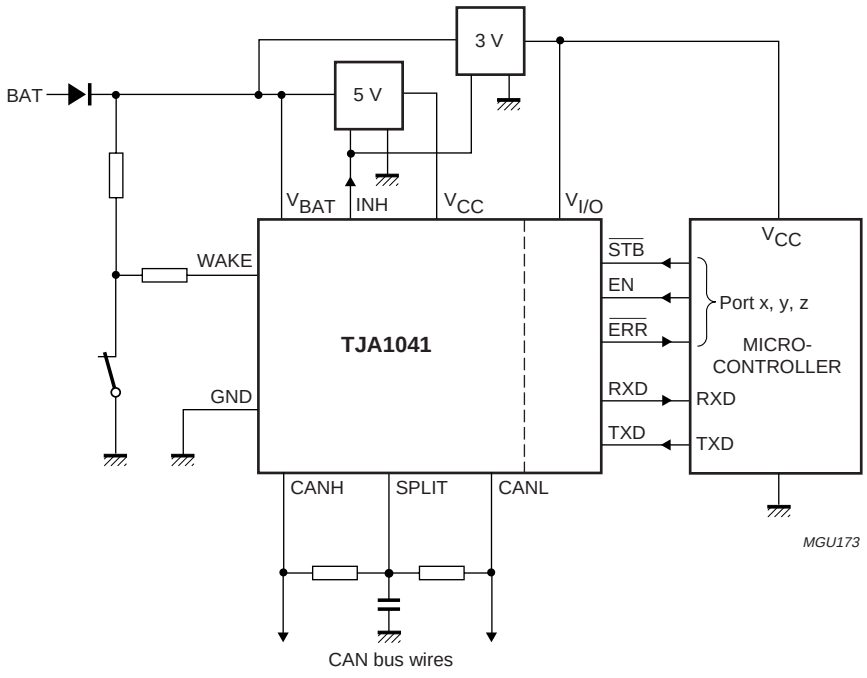


Fig.4 Typical application with 3 V microcontroller.

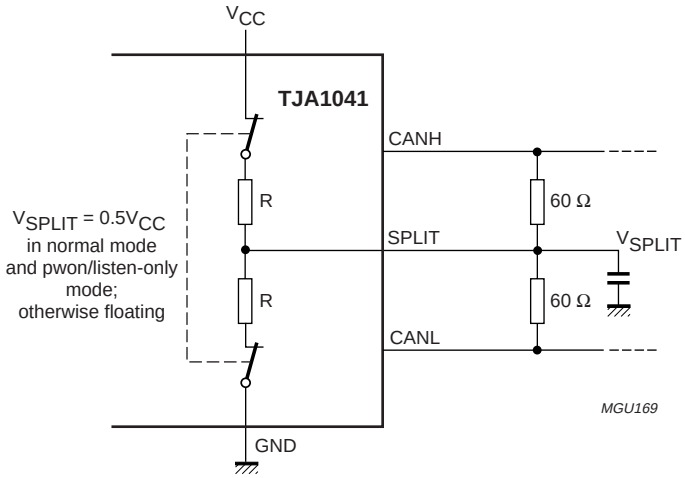
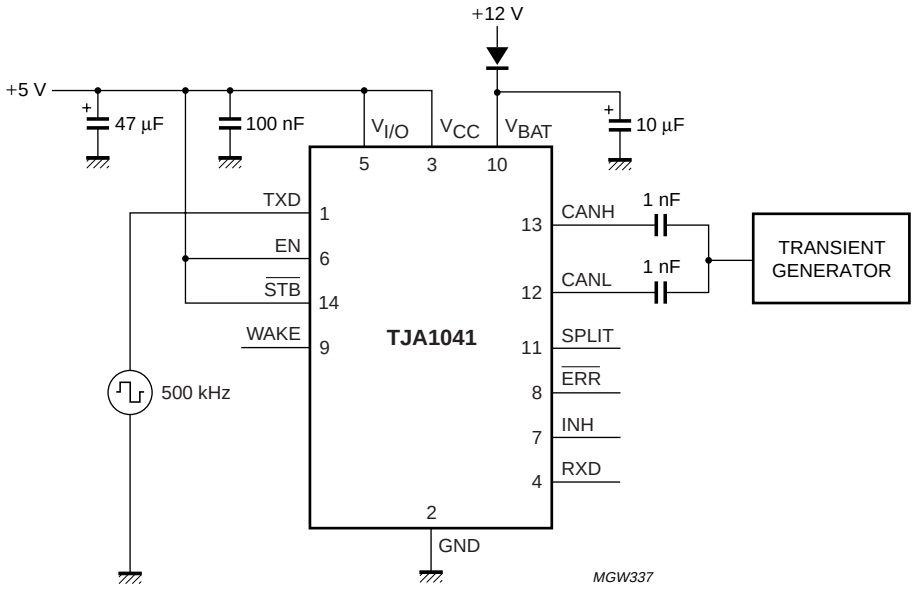


Fig.5 Stabilization circuitry and application.



The waveforms of the applied transients will be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, 3b, 5, 6 and 7.

Fig.6 Test circuit for automotive transients.

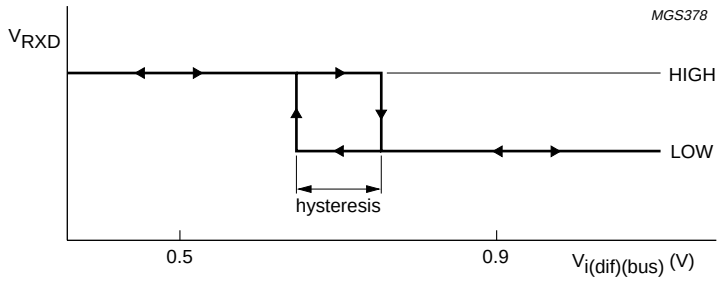


Fig.7 Hysteresis of the receiver.

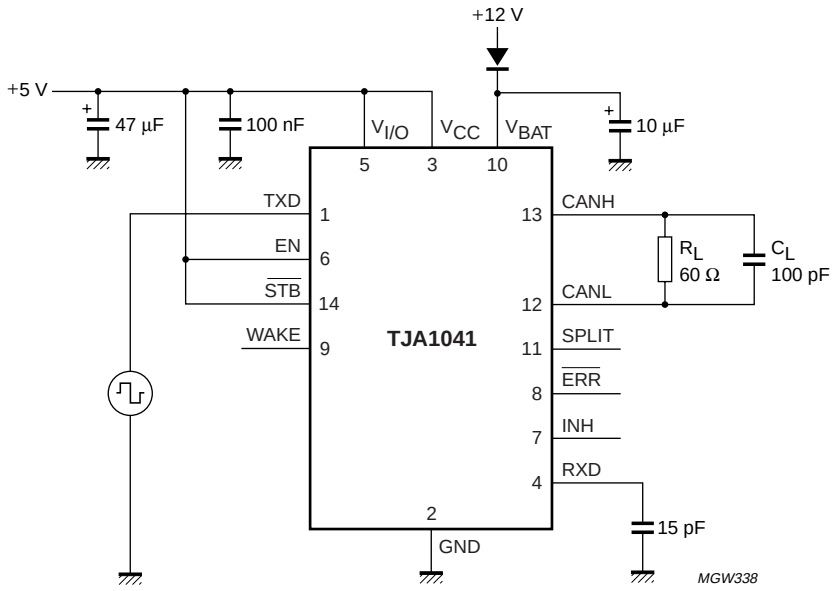
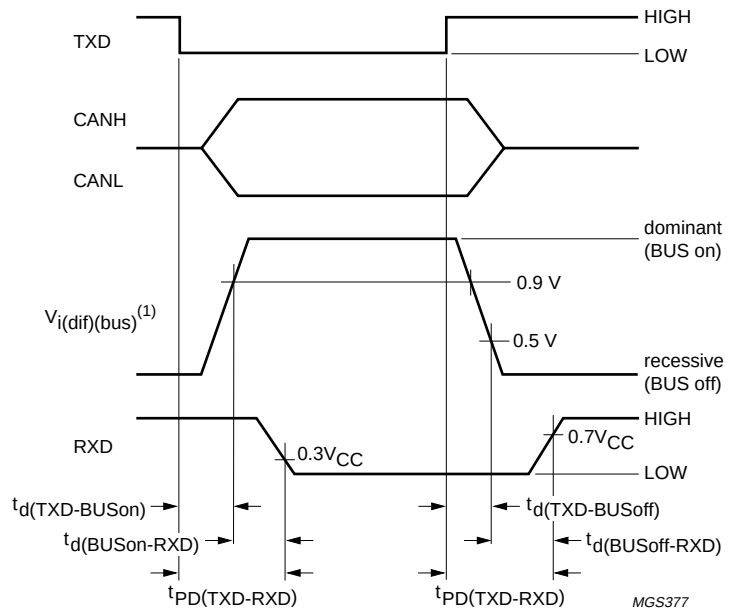


Fig.8 Test circuit for timing characteristics.



(1) $V_{i(dif)(bus)} = V_{CANH} - V_{CANL}$.

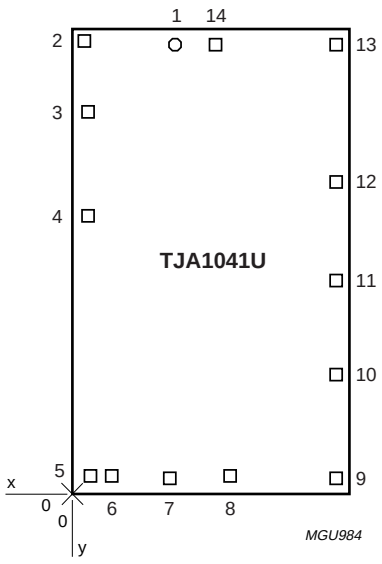
Fig.9 Timing diagram.

BONDING PAD LOCATIONS

SYMBOL	PAD	COORDINATES(1)	
		x	y
TXD	1	664.25	3004.5
GND	2	75.75	3044.25
V_{CC}	3	115.5	2573
RXD	4	115.5	1862.75
$V_{I/O}$	5	115.5	115.5
EN	6	264.5	114
INH	7	667.75	85
$\overline{ERR}$	8	1076.75	115.5
WAKE	9	1765	85
V_{BAT}	10	1765	792.5
SPLIT	11	1765	1442.25
CANL	12	1765	2115
CANH	13	1751	3002.5
$\overline{STB}$	14	940.75	3004.5

Note

1. All x/y coordinates represent the position of the centre of each pad (in μm) with respect to the left hand bottom corner of the top aluminium layer.

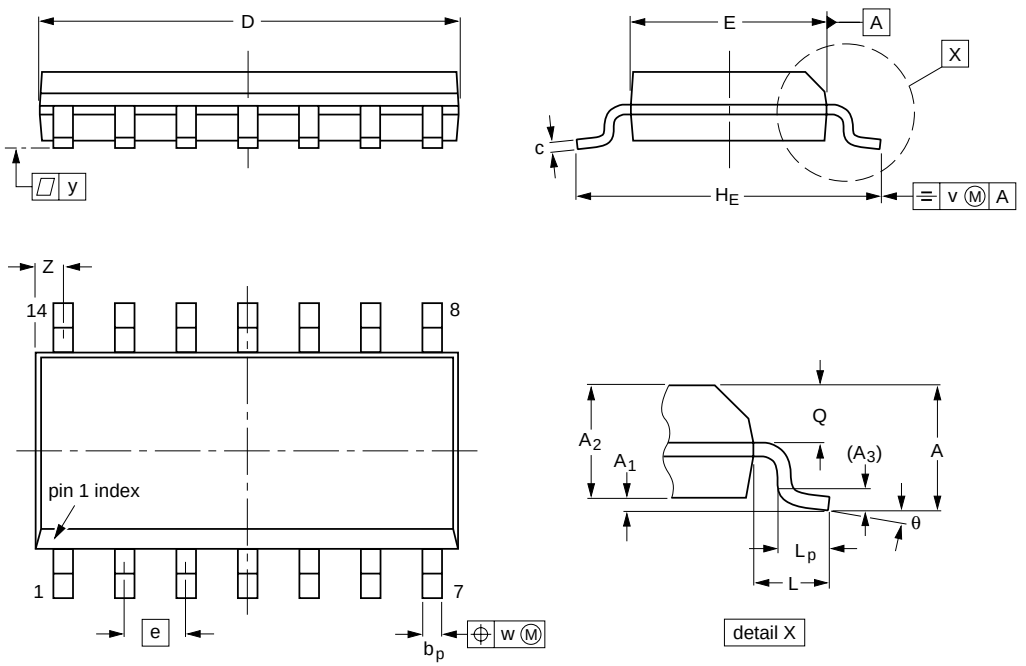


The reverse side of the bare die must be connected to ground.

Fig.10 Bonding pad locations.

PACKAGE OUTLINE

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept:

- below 220 °C for all the BGA packages and packages with a thickness ≥ 2.5mm and packages with a thickness <2.5 mm and a volume ≥350 mm^3 so called thick/large packages
- below 235 °C for packages with a thickness <2.5 mm and a volume <350 mm^3 so called small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Bare die — All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of Philips' delivery. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post packing tests performed on individual die or wafer. Philips Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

Printed in The Netherlands 03/pp24 Date of release: 2003 Feb 13 Document order number: 9397 750 10785

Let's make things better.

Philips
Semiconductors

PHILIPS